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NON-PLANAR SURFACE FOR SEMICONDUCTOR CHIPS AND METHOD OF FORMING THE NON-PLANAR SEMICONDUCTOR CHIP

BACKGROUND OF THE INVENTION

Technical Field

The present invention relates generally to semiconductor chip packaging. More particularly, the present invention relates to a non-planar semiconductor chip, and a method of forming the non-planar semiconductor chip.

Related Art

In the manufacture of semiconductor chip packages, such as laminate chip carriers, differences in the coefficients of thermal expansion, in combination with thermal cycling, tend to produce high stresses in locations of abrupt geometric change within the chip. During thermal cycling the chip may bend creating a stress concentration between the outer edges of the chip and the package cover plate, heat sink, or other device mounted thereon, as well as the adhesive materials therebetween. In addition, high localized stresses tend to occur at the edges of organic chip carrier packages, having heat spreaders or coupled caps, due to the differences in curvature of the various layers. Further, flaws, such as voids, cracks, etc., within the edges or corners of the chip may lead to crack propagation,



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particularly in locations of abrupt geometric change. As a result, chips may become cracked and/or delamination may occur between the chip, cover plate, and the adhesive material therebetween.

Attempts have been made in the industry to minimize the amount of stress concentrations within the chip packages. For instance, the thickness of the chip has been reduced in an attempt to make the chip more flexible, thereby minimizing the stress concentrations. The thickness of the cover plate or heat sink has been reduced near the edges of the cover plate or heat sink in an attempt to increase flexibility as well. Additionally, attempts have been made to minimize the amount of thermal mismatch between the chip, cover plate or heat sink and the adhesives in contact with the chip.

Accordingly, there currently exists a need in the industry for a semiconductor chip package having reduced stress concentrations therein.

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SUMMARY OF THE INVENTION

According to an aspect of the present invention, there is provided an electronic package comprising an electronic component having a first surface electrically mounted to a substrate and a second arcuate surface opposing the first surface and having a contour

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such that the distance between the first surface and the second arcuate surface continuously increases from a periphery of the electronic component to near the center of the electronic component and a planar element mounted to the second arcuate surface of the electronic component by an adhesive.

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BRIEF DESCRIPTION OF THE DRAWINGS

The preferred embodiments of this invention will be described in detail, with reference to the following figures, wherein like designations denote like elements, and wherein:

FIG. 1 depicts a cross-sectional view of a related art semiconductor chip package;

FIG. 2 depicts a cross-sectional view of a semiconductor chip package in accordance with a preferred embodiment of the present invention;

FIG. 3 depicts a semiconductor wafer in accordance with a first embodiment of the present invention;

FIG. 4 depicts a chip and a profiling tool in accordance with the first embodiment of the present invention;

FIG. 5 depicts a profiled chip in accordance with a preferred embodiment of the present invention;

FIG. 6 depicts a semiconductor wafer and profiling tool in accordance with a second embodiment of the present invention;

FIG. 7 depicts a profiled semiconductor wafer in accordance

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with the second embodiment of the present invention;

FIG. 8 depicts a chip in accordance with a third embodiment of the present invention; and

FIG. 9 depicts a modified chip in accordance with the third embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Although certain preferred embodiments of the present invention will be shown and described in detail, it should be understood that various changes and modifications may be made without departing from the scope of the appended claims. The scope of the present invention will in no way be limited to the number of constituting components, the materials thereof, the shapes thereof, the relative arrangement thereof, etc., and are disclosed simply as an example of the preferred embodiment. Although the drawings are intended to illustrate the present invention, the drawings are not necessarily drawn to scale.

Referring to the drawings, FIG. 1 shows a cross-sectional view of a related art semiconductor chip package 10. A carrier 12 is connected to a card or substrate 14 by a plurality of connectors 16. The carrier includes an opening 13 to house a semiconductor chip 18. The chip 18 is electrically connected to the carrier 12 by a plurality of connectors 20. A cover plate 22 is mounted on the carrier 12 and the chip 18 by an adhesive 24.

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Unfortunately, due to differences in the coefficients of thermal expansion between the chip 18, the cover plate 22 and the adhesive 24, in conjunction with thermal cycling, etc., stress concentrations occur within the chip 18 as a result of geometric changes that take place within the chip package 10. As a result, the chip 18 may begin to pull away from the cover plate 22 at the edges 26, as well as the adhesive 24 therebetween, resulting in delamination of the chip 18.

FIG. 2 illustrates a cross-sectional view of a semiconductor chip package 50 in accordance with the present invention. The semiconductor chip package 50 generally includes a carrier 52 having an opening 53 therein. The carrier 52 is electrically connected to a card or substrate 54, such as a circuit board, by a plurality of connectors 56, e.g., ball grid array (BGA), column grid array, grid array, etc. A circuitized or featurized surface 59 of a semiconductor chip 58 is electrically connected to the carrier 52 within the opening 53 by a plurality of connectors 60, e.g., controlled collapse chip connectors (C4). The chip 58 includes a non-planar arcuate or domed back surface 64. A planar element 62, such as a cap, cover plate, heat sink, etc., is mounted on the carrier 52 and the chip 58 by an adhesive 66. The adhesive is preferably a thermally conductive reflowable bonding material known and used in the industry. Due to the configuration of the chip 58, namely, the non-planar or "domed"

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shape, the thickness of the adhesive 66 is greatest near the edges 68 of the chip 58. This allows for bending of the chip 58, that occurs during thermal cycling, without causing the chip 58 to pull away from, or curl towards the planar element 62 at the edges resulting in delamination and/or stress concentrations at the edges of the chip 58. Therefore, the life of the chip and the electronic package is significantly increased, with little or no added expense in manufacture.

Despite the use of a non-planar chip, the finished semiconductor chip package 50 illustrated in FIG. 2, remains substantially planar. The use of a non-planar chip 58 does not alter the shape of the finished semiconductor package 50. This is helpful because it is desirable for the planar element 62 (depicted in FIG. 2) to be flat for the subsequent mounting of heat sinks, heat spreaders, etc., which require a planar mounting surface.

In a first embodiment of the present invention, FIG. 3 depicts a wafer 70 having a first circuitized or featurized surface 59 and a planar second or back surface 73. The featurized surface 59 is circuitized in sections 82 of the wafer 70, such that each section 82 corresponds to the location of a chip 58 (depicted in Fig. 2). The wafer is scored and diced, using a process known in the art, to form individual chips 58, as shown in FIG. 4. Each chip 58 is securely held by a part holder

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61, i.e., a chuck, vice, etc., as known in the art, and back side ground using a profiling tool 74, e.g., a cup grinding wheel, an abrasive impregnated convex surface, etc. Specifically, the concave grinding surface 76 of the profiling tool 74, rotating in the direction indicted by arrow 78, descends (in the direction indicted by arrow 80) upon the back surface 73 of the chip 58, thereby removing a portion of the back surface 73 of the chip 58. A profiled chip 58 is produced having a domed back surface 64, as depicted in FIG. 5. The thickness T of the chip 58 is preferably greatest near the center or midpoint M of the chip 58. The featurized surface 59 of the chip 58 remains undefiled and ready for electrical connection. The modified chip 58 may then be electrically mounted within the chip package 50, as described above and illustrated in FIG. 2.

In the alternative, the wafer 70 may be scored and each section 82 of the wafer 70 may be profiled using the profiling tool 74 before the wafer 70 is diced into individual chips 58. Further, the wafer 70 may be ground, scored and profiled using a profiling tool 74 having an inner grinding surface 76 that only accommodates the profiling of one section 82 of the wafer 70 at a time, as described above. A single profiling tool 74 may also be used having an inner grinding surface 76 capable of grinding, scoring and profiling the entire wafer 70, or a plurality of sections 82 at once.

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In a second embodiment of the present invention, the wafer 70 as a whole may be profiled using a profiling tool 90, as illustrated in FIG. 6. The profiling tool 90, having a concave inner grinding surface 92, rotating in the direction indicated by arrow 94, passes over each section 82 of the wafer 70 in two directions. First the profiling tool 90 passes over each section 82 of the wafer 70 from the back 96 of the wafer 70 to the front 98 of the wafer 70, as indicated by arrow 100. The profiling tool 90 then passes over each section 82 of the wafer 70 from the right side 102 of the wafer 70 to the left side 104 of the wafer 70, as indicated by arrow 106. FIG. 7 shows the wafer 70 produced, wherein each section 82 of the wafer 70 has a non-planar domed back surface 64. The wafer 70 is then diced along score lines 84, using techniques well known in the art, forming individual chips 58 having domed back surfaces 64, as shown in FIG. 5. The individual chips 58 may then be mounted in a chip package 50, as depicted in FIG. 2.

The second embodiment is not limited by the above description. For instance, multiple profiling tools 90 may be used having different concave inner grinding surfaces 92. In particular, the first pass over sections 82 of the wafer 70, in the direction indicated by arrow 100, may be performed using a profiling tool 90 having a first concave inner grinding surface 92, while the second pass, in the direction indicated by arrow

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106, may use a profiling tool 90 having a second concave inner grinding surface 92.

It should be appreciated that the first and second embodiments described above may be modified by those skilled in the art, without departing from the scope of the present invention. For instance, one or more sides of the chip 58 or wafer 70 may be profiled to form a domed surface 64, in addition to, or in place of forming the domed back surface 64. In other words, the present invention is not limited to forming a domed surface 64 on the back surface 73, opposite the featurized surface 59.

A third embodiment of the present invention provides for the optional profiling of one or more edges 110, 111 of the chip 58. As illustrated in FIG. 8, the edges 110 in this example refer to the location where the sides 114 of the chip 58 meet. Likewise, the edges 111 refer to the location where the surfaces 59, 64, or 73 meet the sides 114 cf the chip 58. Each chip 58 is held by a part holder 61, i.e., a chuck, vice, etc., as known in the art. A profiling tool 120, (similar to the profiling tool 90 shown in FIG. 6), having a concave inner grinding surface 122, rotating in the direction indicated by arrow 124, descends in the direction indicated by arrow 126 along one or more of the edges 110 of the chip 58. In a similar manner, the profiling tool 120 may then optionally be used to profile the edges 111 if so desired or

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needed.

FIG. 9 shows the chip 58 having radiused edges 112 produced as a result of profiling the edges 110. The rounded or radiused edges 112 help to eliminate flaws and stress concentrations often found at the edges 110, 111 of the chip 58. In particular, radiusing the edges 110 of the chip 58 will remove voids, chips and other small defects created at the edges 110, 111 of the chip 58 during scoring and dicing operations.

The third embodiment was illustrated in FIG. 8 using the chip 58, having a domed back surface 64, preferably formed using one of the techniques described above. However, it should be understood that this is only an example. This embodiment may be used in conjunction with, or completely independent of, the first and/or second embodiments. In other words, the technique described herein for forming radiused edges 112 may be used in conjunction with any type of chip, and is not restricted to use with the chip 58 having a domed surface 64.

It should be noted that the shape of the chip 58 used as an illustration dictates the location of the edges 110, 111. Since the present invention may be used for any variety of chip configurations, e.g., cylinders, discs, hemispheres, polygons, etc., the number and location of the edges 110, 111 will also vary accordingly, and are not limited by this disclosure.

While this invention has been described in conjunction with

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the specific embodiments outlined above, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the preferred embodiments of the invention as set forth above are intended to be illustrative, not limiting. Various changes may be made without departing from the spirit and scope of the invention as defined in the following claims.

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CLAIMS

We claim:

1. An electronic package comprising:

an electronic component having a first surface electrically mounted to a substrate and a second arcuate surface opposing the first surface and having a contour such that the distance between the first surface and the second arcuate surface continuously increases from a periphery of the electronic component to near the center of the electronic component; and

a planar element mounted to the second arcuate surface of the electronic component by an adhesive;

wherein localized stresses at the edge of the electronic component are minimized.

2. The electronic package of claim 1, wherein a planar element is mounted to the second arcuate surface of the electronic component is a cover plate.

3. The electronic package of claim 1, wherein a planar element is mounted to the second arcuate surface of the electronic component is a heat sink.

4. The electronic package of claim 1, wherein the second arcuate surface of the electronic component is contoured using a profiling tool having a concave profiling surface.

5. The electronic package of claim 1, wherein the adhesive is a thermally conductive reflowable adhesive.

6. The electronic package of claim 1, wherein the substrate has an opening within which the electronic component is mounted.