

Description

The invention relates to a hybrid circuit comprising an input, an output and an in/output, at least one signal transistor, at least one auxiliary transistor incorporated as a current multiplier in a circuit with an associated signal transistor and an impedance circuit incorporated in a circuit with associated signal transistor, a junction point of this impedance circuit being connected to the output of the hybrid circuit, the impedance circuit as a whole having such impedance related to the coefficient of the auxiliary transistor that the hybrid circuit fulfills the line matching condition.

A hybrid circuit of the type mentioned hereinbefore is known from the German "Auslegeschrift" 2 829 392.

The active hybrid circuit known from the above-mentioned publication can be designed to be symmetrical, or and in that case to comprise two axially symmetrical half sections. This known active hybrid circuit can further be designed to comprise only NPN-transistors in the signal path, as a result of which in accordance with the then state of the art higher limit frequencies could be obtained than in case PNP-transistors would have been inserted in the signal path.

In case the known hybrid circuit is of a symmetrical configuration, each half section comprises two signal transistors, one of which being connected to the input and in/output of the hybrid circuit and a negative supply line and being inserted in a circuit comprising an auxiliary transistor switched as a current multiplier, the auxiliary transistor coefficient being smaller than 1, the other signal transistor being connected between the output and in/output of the hybrid circuit and a positive supply line and being incorporated in a circuit comprising an impedance circuit, in the simplest case composed of a series arrangement of two resistors, with more specifically a first resistor, being inserted between the collector of the aforesaid signal transistor, and the positive supply line and having a value amounting to half the line resistance, for example 300 Ohms and the other resistor being connected between the collector and the base of this signal transistor and having a value equal to the inverse decreased by 1 of the aforesaid coefficient times half the line resistance, in order to meet the requirement of line matching. However, to avoid cross-talk of the input signal at the output of the hybrid circuit the aforesaid resistors of the impedance circuit are not interlinked directly, but by means of a base emitter transistor of an additional transistor of the impedance circuit, whose collector is connected to the positive supply line.

The object aimed at with the known hybrid circuit is transmitting onto the line the whole signal current at the input of the hybrid circuit, this object being achieved through the measures of current amplification (division) and impedance transformation, at least as regards transmitting onto the line. Further advantages of the known hybrid circuit are that it is readily integrated relatively simple to construct and that it has a small current consumption.

In addition to the advantage of high limit frequencies, the aforementioned advantages are of importance when such a hybrid circuit has to be inserted in an integrated modem circuit for example, for a viewdata system.

For such use, however, not only the current consumption or the dissipation should be lowest possible, but especially for direct supply from the line the required supply voltage should be lowest possible, with for example a total available power of approximately 20 mW and a total available supply voltage of approximately 4.5-8 V.

Unfortunately, with the known hybrid circuit, specially in practical embodiments thereof, this is not quite well possible owing to the required transistors connected in series and in a totem pole configuration between the supply lines, each requiring a diode voltage (base/emitter voltage) of approximately 0.7 Volt.

The object of the invention is to provide a new concept for a hybrid circuit in which the least possible supply voltage is lost on required diode voltages.

The invention hereto provides a hybrid circuit of the type mentioned in the preamble, characterized in that the impedance circuit is connected between the in/output and at least one virtual earth point of the hybrid circuit and has a further junction point connected to the input of the hybrid circuit, in that the signal transistor(s) is(are) connected between an associated virtual earth point and an associated supply line and in that two auxiliary transistors having the same multiplication coefficient are connected between a respective supply line and the in/output of the hybrid circuit and are incorporated in a current mirror circuit having at least one signal transistor, with junction points in the impedance circuit determining partial impedances being selected such that the hybrid balance condition is fulfilled.

Worded differently, the invention provides an active symmetrical balance hybrid circuit, which need not necessarily be axially symmetrical, but which can also have a universal coupling and which comprises in each half section an in/output for connection to a two-way transmission line, an input for connection to a transmitter and an output for connection to a receiver, an impedance circuit connected between the

in/output of the hybrid circuit and preferably one virtual earth point, for example a resistor circuit, whose respective branches are connected to the input and the output of the hybrid circuit, preferably one signal transistor connected between the virtual earth point and a respective supply line and two auxiliary transistors each connected between the in/output of the hybrid circuit and a respective supply line as a current amplifier having a multiplication coefficient larger than 1 and inserted in a current mirror circuit preferably comprising the one signal transistor of the relevant half section, the auxiliary transistors in the latter case being complementary, the resistor circuit being dimensioned such that both the condition of line matching and the condition of hybrid balance are fulfilled, implying that the overall impedance of the resistor-circuit, that is to say on the one side the resistance value of a series arrangement of resistors between the in/output of the hybrid circuit and the virtual earth point and on the other side the coefficient of the auxiliary transistors and the line impedance, more specifically, the line resistance of the transmission line to be connected to the in/output of the hybrid circuit are assimilated such that the in/output resistance of the hybrid circuit as seen from the transmission line is equal to the line resistance, worded more generally, that the impedance of the in/output of the hybrid circuit is the complex conjugate of the line impedance and that the partial resistance-values of the resistor circuit between in/output, output input and the virtual earth point of the hybrid circuit are determined such that a signal on the input of the hybrid circuit does not appear on the output of the hybrid circuit.

A balanced current multiplier circuit is described in the International Patent Application WO 83/01163. This multiplier circuit is intended for use in a subscriber line interface circuit (SLIC) in a telephone exchange. This circuit is intended for supplying signals and DC-current to the subscriber line; it does not address itself to the problem of operating with a current consumption and a dissipation being as low as possible, nor does it offer a solution of the problem how to operate at a very low available power or a very low supply voltage. Moreover, it is not provided with a virtual earth point to which an impedance circuit is connected.

In the United States Patent No. 4,300,023 a hybrid circuit (SLIC) is described for use in a telephone exchange. This document also does not address itself to the aforementioned problems, nor does it show the characterizing features of the invention.

As stated hereinbefore, in a preferred embodiment of the hybrid circuit in accordance with the invention, the auxiliary transistors are complementary, implying PNP transistors to be present in the signal path, whose limit frequency can come close to that of NPN transistors in accordance with the present state of the art, whereas, which is more important, in that case the least supply voltage is required because with a drive to full voltage swing both auxiliary transistors in the half sections can assume a negligibly small collector-emitter voltage.

In a further preferred embodiment only NPN-transistors are used in the signal path and the coupling of the half sections is axially symmetrical like in the known hybrid circuit. Per half section, however, exactly one signal transistor is used, this single signal transistor being incorporated in a current mirror circuit with both auxiliary transistors of the same section.

As the resistance value of the resistor between the in/output and output of the hybrid circuit is proportional to the coefficient of the auxiliary transistors, this resistor is preferably designed to be an external resistor among others to fulfill the condition that the resistance value on the in/output of the hybrid circuit may have a maximum tolerance of for example 5 %.

In addition to the advantages of low dissipation by simply designing the matching resistor as a virtual resistor, high cut-off frequencies and simplicity of the circuit, further advantageous features of the suggested hybrid circuit are that the circuit is designed to be balanced and to be driven in class A, making the overall current consumption time-invariant and avoiding thus cross-talk via the supply lines and that the hybrid circuit is extremely linear. The supply voltage and supply current can also be used rather well by piling the bipolar hybrid circuit with one or more layers of PL. The maximum supply current of 2-4 mA (V.23) can be set or limited by an external resistor.

The invention will now be further explained by way of example with reference to the attached drawing, wherein:

Fig. 1 shows the circuit diagram of an embodiment of the hybrid circuit for explaining the principles of the relevant invention;

Fig. 2 shows a preferred embodiment of a total hybrid circuit in accordance with the present invention based on the example of fig. 1;

Fig. 3 shows a half section of a further preferred hybrid circuit; and

Figs. 4A-C show examples for realising a virtual earth point in the case of the hybrid circuit section of fig. 3.

In fig. 1 a half section of an axial symmetrical hybrid circuit in accordance with the present invention is

shown. The half section comprises two complementary signal transistors T_{s1}, T_{s2} and two complementary auxiliary transistors T_{h1}, T_{h2} , the bases of the PNP-transistors T_{s1} and T_{h1} being jointly connected to the output of an operational amplifier A1, the emitters of these transistors being connected to a positive supply line V_1 . The bases of the NPN-transistors T_{s2} and T_{h2} are similarly jointly connected to the output of an operational amplifier A2, their emitters being connected to a negative supply line V_2 .

The collectors of the auxiliary transistors T_{h1}, T_{h2} are jointly connected to the in/output I/O of this half section of the hybrid circuit, which can be connected to the in/output of the other section by means of a winding of a line transformer (not shown) whilst the other winding of the line transformer can be connected to a transmission line.

The collector of the signal transistor T_{s1} is connected to the non-inverting input of the operational amplifier A1, the inverting input of the operational amplifier A1 having a slight positive DC bias $+dE$ and this inverting input being earthed for signals, the collector of the signal transistor T_{s2} is connected to the non-inverting input of the operational amplifier A2, the inverting input of the operational amplifier A2 having a slight negative DC bias $-dE$ and this inverting input being earthed for signals, which is indicated in the figure by respectively "O" $+ dE$ and "O" $- dE$. as a result of the functioning of operational amplifiers A1, A2 the collectors of the signal transistors T_{s1}, T_{s2} are virtually earthed, that is the voltage is earth, but the current cannot flow to earth.

Worded differently, the signal transistors T_{s1} and T_{s2} are virtually switched as diodes and form current mirror circuits with the associated auxiliary transistors T_{h1} and T_{h2} , causing the collector currents of the signal transistors T_{s1} and T_{s2} to be identical. The auxiliary transistors T_{h1} and T_{h2} are switched as current amplifiers, for example as a result of the presence of an emitter resistor (not shown) in the emitter lines of the auxiliary transistors T_{h1} and T_{h2} , this resistor being n times smaller than the emitter resistors (not shown) in the emitter lines of the signal transistors T_{s1} and T_{s2} , causing the current coefficient to be n , which in the figure is indicated by 1^x and n^x with the respective signal transistors T_{s1}, T_{s2} and the auxiliary transistors T_{h1} and T_{h2} . In practice this can be done more accurately by providing correspondingly different emitter surfaces for the integrated signal transistors T_{s1}, T_{s2} as the only measure, or in combination with the aforesaid measure.

Between the junction point of the in/output I/O of the half hybrid circuit section and the collectors of the auxiliary transistors T_{h1}, T_{h2} and the associated junction points of the collector of the signal transistor T_{s1} and the non-inverting input of the operational amplifier A1 on the one side and of the collector of the signal transistor T_{s2} and the non-inverting input of the operational amplifier A2 on the other an impedance circuit is inserted comprising in the shown embodiment a resistor circuit R_1, R_2 and R_3 as well as a T-section of three small resistors with two small resistors $2dR$ being inserted in the parallel branch and one small resistor $-dR$ being inserted in the series branch and the unused end of the latter small resistor being connected to the resistor circuit, more specifically R_3 , the unused ends of the small resistors $2dR$ being connected to respective junction points of signal transistors T_{s1}, T_{s2} and the non-inverting inputs of respective operational amplifiers A1, A2. The junction point of resistor $-dR$ and resistor R_3 is indicated by B, the input I of the half hybrid circuit being connected to the junction point of resistor R_2 and R_3 and its output O being connected to the junction point of resistors R_1 and R_2 . For practical reasons preference is given to $R_3 - dR > 0$.

In a state of equilibrium a small direct voltage $+dE$ will be applied to the collector of signal transistor T_{s1} due to the operation of operational amplifier A1. Similarly a small direct voltage $-dE$ will be applied to the collector of signal transistor T_{s2} . Consequently, a quiescent current $J = 2dE/4dR$ will flow from the collector of signal transistor T_{s2} , and as a result of the coefficient n of the auxiliary transistors T_{h1}, T_{h2} a quiescent current nJ will flow from the collector of the auxiliary transistor T_{h1} to the collector of the auxiliary transistor T_{h2} .

If $n \gg 1$ the largest current consumption will take place in the auxiliary transistors T_{h1}, T_{h2} . Assuming a signal current i_i flowing into the in/output I/O, a current flowing into auxiliary transistor T_{h1} will be approximately $nJ - i_i/2$, whilst the current flowing into auxiliary transistor T_{h2} will be $nJ + i_i/2$.

Because it was assumed for the half hybrid circuit section shown in fig. 1 that the line current i_i flowed into the in/output I/O, this current i_i will flow from the in/out of the other half section, so that for this other half section the condition holds that for the auxiliary transistor in the other half section corresponding to auxiliary transistor T_{h1} the current flowing through this auxiliary transistor will be $nJ + i_i/2$, and will be analogously $nJ - i_i/2$ through the auxiliary transistor in the other half section corresponding to the auxiliary transistor T_{h2} .

Consequently, the overall current consumption of the whole hybrid circuit will be $2(n + 1)J$, irrespective of the signal current i_i . In view of the fact that the supply lines in an integrated circuit can cause considerable resistance, a time-invariant current dissipation will avoid in the entire hybrid circuit cross-talk to

further circuits fed by the same supply lines.

The transistors T_{h1} and T_{h2} cannot handle negative current. So the supply current of these transistors nJ has to be larger than the peak value of $ni/2$. For a large n the condition holds that ni is about equal to the line current i_l . The line current i_l consists of a part i_{lr} coming from a transmitter and a part i_{lt} intended for a receiver. The following condition should hold: $2nJ > \text{peak value of } (i_{lr} + i_{lt})$. The supply voltage between the supply lines V_1 and V_2 should further be larger than twice the peak value of the line voltage v_l . If the said supply voltage is E , the following condition should hold:

$$E > \text{peak value of } (v_{lr} - v_{lt})$$

In the worst case with an overall maximum signal level on a transmission line of 600 Ohms in accordance with the V.23 standard of 1 milliwatt there is a transmitter power of 0.5 milliwatt and a receiver power of 0.5 milliwatt, so that the peak value of $i_{lr} + i_{lt}$ is the root of 20/3 milliampere and the peak value of $V_{lr} - v_{lt}$ is the square root of 2.4 Volts, leading to the theoretical minimum power consumption for the entire hybrid circuit of :

$$(\text{voltage difference between supply lines } V_1, V_2) \times 2nJ = \sqrt{2.4} \times \sqrt{20/3} \text{ milliwatts} = 4 \text{ milliwatts.}$$

Hereinbelow the line matching condition for the embodiment of the hybrid circuit in accordance with fig. 1 will be calculated.

Let it be assumed that $i_t = i_r = 0$, a signal current i_l flowing into in/output I/O of the half section shown in fig. 1 will result in a current i in the resistor circuit R_1, R_2, R_3 , branching into currents $i/2$ through signal transistors T_{s1}, T_{s2} , causing currents $ni/2$ to flow into auxiliary transistors T_{h1}, T_{h2} . Applying the appropriate Kirchoff's law to the in/output I/O will yield $i_l = ni/2 + ni/2 + i = (n+1)i$. As the collectors of the signal transistors T_{s1}, T_{s2} are virtually earthed, the resistors $2dR$ are connected in parallel with each other and this parallel circuit is connected in series with the resistor $-dR$, resulting in 0 Ohm net. Let the resistance value of the series arrangement of resistors $R_1 + R_2 + R_3 = R_{tot}$ be the signal voltage on the in/output I/O, V_l and let the connection to the line transformer of the in/output I/O be translated into a virtually earthed half line resistance $R_l/2$, the following condition will hold:

$$V_l = iR_{tot} = R_l/2 \cdot i = R_l/2(n+1)i,$$

from which it follows that:

$$R_{tot} = (n+1)R_l/2 \text{ (line matching condition).}$$

As a result of a virtual impedance in the place of the balance in the hybrid circuit in accordance with the invention forming a correct terminating impedance use of feedback, an electronic measure is taken to minimise dissipation loss in the balance on transmitting.

Subsequently, the hybrid balance condition will be calculated, assuming for convenience that a signal current i_t in the input I results in a signal voltage 0 at the output O, the signal current i_t in the input I branching into partial signal currents i_2 and i_3 because of the resistors R_2 and R_3 , as represented in fig. 1, with the following conditions holding for these partial signal currents:

$$i_2 = \frac{R_3 \cdot i_t}{R_2 + R_3} ; i_3 = \frac{R_2 \cdot i_t}{R_2 + R_3}$$

It is likewise assumed that the in/output I/O is virtually earthed via the half line resistor $R_l/2$. As it is assumed that the transmit current i_t in the input I results in a signal current i_r from the output equalling 0, the total partial signal current i_2 will flow through R_2 and through R_1 . This will result in the following equation:

$$i_t R_l/2 = i_2 R_1$$

As the partial signal current i_3 equally branches over signal transistors T_{s1}, T_{s2} through R_3 , these equally branched partial currents multiplied by the coefficient n will occur in the auxiliary transistors T_{h1}, T_{h2} .

12, so that the following condition will hold :

$$i_1 = ni_3/2 + ni_3/2 - i_2$$

5 Now the following condition holds :

$$R_1/2 \cdot (ni_3 - i_2) = R_1 \cdot i_2$$

or:

$$R_1/2 \cdot \left[n \cdot \frac{R_2 \cdot i_t}{R_2 + R_3} \cdot \frac{R_3 \cdot i_t}{R_2 + R_3} \right] = R_1 \cdot \frac{R_3 \cdot i_t}{R_2 + R_3}$$

or:

$$(n R_2 - R_3) \cdot R_1/2 = R_1 \cdot R_3 \text{ (hybrid balance condition).}$$

If $R_2 = R_3$ it will follow that :

$$(n-1) \cdot R_1/2 = R_1.$$

If, in addition, $R_2 = R_3 = R_1/2$ the line matching condition is fulfilled at the same time.

If we take $R_2 = R_3 = R_1/2 = 300$ Ohms as a numerical example, it will hold that $R_1 = (n-1) \cdot 300$ ohms.

25 If, for example, we take 12 for n , R_1 will be 3.3 kilohms. As observed before this resistor R_1 can be designed to be an external resistor.

Owing to the use of complementary auxiliary transistors T_{h1} , T_{h2} a design in accordance with fig. 1 of the hybrid circuit according to the invention will need at least supply voltage, this is the difference in voltages of supply lines V_1 and V_2 , which difference has to exceed the peak value of the signal voltage v_1 incremented by two times the saturation voltage of the collector-emitter path of the auxiliary transistors T_{h1} , T_{h2} , which saturation voltage can amount to approximately 100 millivolts.

A more practical embodiment of the hybrid circuit with complementary transistors in accordance with the present invention based on the circuit of fig. 1 will now be further described with reference to fig. 2.

35 In fig. 2 is shown a complete hybrid circuit to clearly show that the half sections are not axially symmetrical but form a universal coupling. Elements corresponding with those in fig. 1 are indicated by the same reference characters. By providing a direct current source S in each half section the resistors $-dR$ and $2dR$ in fig. 1 can be omitted and there will be no need of the small direct voltages $+dE$ and $-dE$ at the inverting inputs of the operational amplifiers $A1$ and $A2$. Corresponding elements in the upper half section have identical reference characters but are extended by an accent. Respective coupling transistors T_k and T'_k have been extended to the half sections of the complete hybrid circuit in fig. 2.

The half section of the hybrid circuit shown in fig. 2 corresponding to the half section shown in fig. 1 will henceforth be called the left section, the other half obviously being called the right section.

Let it be assumed that $i_i = i_r = 0$, a signal current i_1 into the in/output I/O of the left section will result in a current i through the resistor circuit R_1 , R_2 , R_3 to the junction point with the current source S , supplying a current J , to the collector of signal transistor T_{s2} and the non-inverting input of the operational amplifier A_2 , whose output is connected to the base of signal transistor T_{s2} and whose inverting input is connected to a reference voltage (earth point) to which also the inverting input of operational amplifier $A1$ is connected, whose non-inverting input is connected to the collector of signal transistor T_{s1} and whose output is connected to the base of signal transistor T_{s1} . By means of the operational amplifiers $A1$, $A2$ connected thus, the signal transistors T_{s1} , T_{s2} are virtually switched as diodes. The base of signal transistor T_{s2} is connected to the base of auxiliary transistor T_{h2} and likewise to the base of coupling transistor T_k . Due to this current mirror circuit the collector currents of the signal transistor T_{s2} , auxiliary transistor T_{h2} and coupling transistor T_k are interrelated in a ratio of 1:n:1. In a like manner the collector currents of signal transistor T'_{s2} , auxiliary transistor T'_{h2} and coupling transistor T'_k of the right section are also interrelated in a ratio of 1:n:1. The collector current of signal transistor T_{s1} of the left section is further equal to the collector current of coupling transistor T'_k , due to the universal coupling with coupling transistor T'_k of the right section as the operational amplifier $A1$ substantially draws no current. The signal transistor T_{s1} being virtually connected as a diode and its base being connected to the auxiliary transistor T_{h1} a current mirror

circuit will be formed causing the collector current of the auxiliary transistor T_{h1} to be n times the collector current of signal transistor T_{s1} . The circuit formed by the auxiliary transistor T_{h1} and signal transistor T_{s1} in the left section and the coupling transistor T_k the signal transistor T_{s2} and the auxiliary transistor T_{h2} in the right section can therefore be called a current mirror circuit. The same applies to the signal transistor T_{s2} , auxiliary transistor T_{h2} and coupling transistor T_k of the left section and the signal transistor T_{s1} and auxiliary transistor T_{h1} in the right section.

The hybrid circuit of fig. 2 can possibly be designed to be complementary, that is to say that PNP-transistors are replaced by NPN-transistors and vice versa.

Analogous to fig. 1 the line matching condition can be calculated as follows:

$$R_{tot} = R_1 + R_2 + R_3 = (2n + 1) \cdot R/2$$

and the hybrid balance condition:

$$R/2 \cdot (2nR_2 - R_3) = R_1 R_3.$$

Let R_2 and R_3 be equal, the two conditions are fulfilled if:

$$R_1 = (2n-1) \cdot R/2 \text{ and } R_2 = R_3 = R/2$$

A preferred embodiment of an axially symmetrical hybrid circuit will now be described with reference to fig. 3 showing a half section only using NPN-transistors in the signal paths and with a possibly higher limit frequency having a detrimental effect on the supply voltage requiring a supply voltage which is one base-emitter voltage higher. Elements in fig. 3 corresponding to those in fig. 1 are again indicated by identical reference characters. In the half section of fig. 3 there is a single signal transistor T_s whose collector is virtually earthed through the operational amplifier A having its inverting input connected to a reference voltage (earth), the signal transistor T_s being virtually switched as a diode by connecting the non-inverting input of the operational amplifier A to its collector and by connecting the output of the operational amplifier A to its base. The signal transistor T_s together with auxiliary transistor T_{h2} forms a current mirror circuit causing the collector current of the auxiliary transistor T_{h2} to be n times the collector current of the signal transistor T_s . The signal transistor T_s does not only form a current mirror circuit with auxiliary transistor T_{h2} , but with coupling transistor T_k as well. The collector current of coupling transistor T_k is equal to the collector current of the signal transistor T_s . The respective transistors T_{c1} and T_{c2} are connected in parallel with the auxiliary transistors T_{h1} and T_{h2} , transistor T_{c1} being connected as a diode. The collector of coupling transistor T_k is connected to the collector of transistor T_{c1} , a direct current source S_2 being connected to the junction point of the collectors and supplying a current $2J$. A current source S_1 supplying a current J is connected to the junction point of the resistor circuit R_1, R_2, R_3 , the collector of the signal transistor T_s and the non-inverting input of the operational amplifier A.

Let it be assumed that a line signal current i , supplied to the in/output I/O of the half hybrid circuit of fig. 3 results in a current i through the resistor circuit R_1, R_2, R_3 and that $i_r = i_t = 0$, the current i will then flow through the signal transistor T_s and also through the coupling transistor T_k and the transistor T_{c2} and the current ni will flow through the auxiliary transistor T_{h2} . The current i through the coupling transistor T_k will entail a current i through the transistor T_{c1} and this current will result in a current ni through the auxiliary transistor T_{h1} . In other words auxiliary transistors T_{h1} and T_{h2} are connected to the signal transistor T_s in a current mirror circuit.

Analogous to the aforedescribed embodiments the following condition holds for line matching :

$$R_{tot} = (2n + 3) \cdot R/2$$

As regards the hybrid balance condition the following holds:

$$((2n+2)R_2 - R_3) \cdot R/2 = R_1 \cdot R_3.$$

If again it is assumed that $R_2 = R_3$ these two conditions are fulfilled if:

$$R_1 = (2n + 1) \cdot R/2 \text{ and } R_2 = R_3 = R/2.$$

Although hereinbefore a 1:1 line output transformer ratio was assumed, with a different line output

transformer ratio the maximum line signal voltage can be accommodated to the supply voltage. By implementing this measure the other transformer ratio can act as a parameter in the line matching and hybrid balance condition. At a ratio of 1:m the following condition will hold for fig. 3:

$$5 \quad R_1 = m^2(2n + 1) \cdot R_1/2 \text{ and } R_2 = R_3 = m^2 R_1/2.$$

In fig. 3 the current source S_2 forces transistor T_{c1} to supply a current which is complementary to the current through coupling transistor T_k and therefore the current through signal transistor T_s .

Also in fig. 3 the current coefficient n provides a virtual input resistance of for example 300 ohms on the in/output I/O.

In fig. 3 a transmitter current i_t in the input I with $i_r = 0$ results in a line current i_l in the in/output I/O which equals:

$$15 \quad i_l = (2ni_3 + 2i_3) - i_2 = (2n+2) \cdot \frac{R_2 \cdot i_t}{R_2 + R_3} - \frac{R_3 \cdot i_t}{R_2 + R_3}$$

and if $R_2 = R_3$ the condition holds that :

$$i_l = (n + 0.5) \cdot i_t.$$

The signal voltage v_r , scanned by a receiver on the output O equals:

$$25 \quad v_r = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \cdot v_1$$

30 With $R_1 = (2n + 1) \cdot R_1/2$ and $R_2 = R_3 = R_1/2$ the following condition holds:

$$35 \quad v_r = \frac{v_1}{n+1,5}.$$

In the embodiments of the integratable symmetrical balance hybrid circuit in accordance with the invention discussed and shown hereinbefore, for clarity's sake it was assumed to use operational amplifiers for virtually earthing collectors of signal transistors and virtually switching these transistors as diodes to result in an according current mirror circuit. Such a use of operational amplifiers is not necessary, though, as will be explained hereinafter with reference to figs. 4A-C, likewise indicating how simply a virtual earth point can be provided, which is a rather obvious matter for those skilled in the art.

Figs. 4A-C correspond to fig. 3 and identical reference characters are used. The differences between fig. 3 and fig. 4a are that the signal transistor T_s is switched as a diode and the operational amplifier A is substituted for a PNP-transistor T_v , whose base is connected to a reference voltage "O" (earth), its collector being connected to the junction point of the bases of the transistors T_s , T_k , T_{c2} and T_{h2} , and its emitter being connected to the junction point of direct current source S_1 and resistor R_3 , the collector of T_s not being connected to the latter junction point. A disadvantage of the circuit of fig. 4A could be that the virtual earth point between resistor R_3 , direct current source S_1 and the emitter of the PNP-transistor T_v is a virtual earth point only by approximation due to the base emitter voltage of this transistor T_v . Figs. 4B and 4C give solutions to this problem, the PNP-transistor T_v being simulated (T_v) with the aid of a number of transistors and possibly a diode. Figs. 4B and 4C show the base-emitter and collector connections b, e, c of the simulated PNP-transistor T_v .

The operation of the circuits shown in figs. 4A-C will be clear for those skilled in the art and a further explanation thereof will not be given, whilst it should be observed that there are and that there can be designed a great many more of these circuits.

The direct current sources S , S' , S_1 and S_2 as well as direct current sources which are not shown are preferably PNP-transistors.

Claims

1. A hybrid circuit comprising an input (I), an output (O) and an in/output (I/O), at least one signal transistor (T_{s1}), at least one auxiliary transistor (T_{h1}) incorporated as a current multiplier in a circuit with an associated signal transistor (T_{s2}) and an impedance circuit (R_1, R_2, R_3) incorporated in a circuit with an associated signal transistor (T_{s2}), a junction point of the impedance circuit being connected to the output (O) of the hybrid circuit, the impedance circuit as a whole having such impedance related to the multiplication coefficient of the auxiliary transistor (T_{h1}) that the hybrid circuit fulfils the line matching condition, characterized in that the impedance circuit (R_1, R_2, R_3) is connected between the in/output (I/O) and at least one virtual earth point of the hybrid circuit and has a further junction point connected to the input (I) of the hybrid circuit, in that the signal transistor(s) (T_{s1}, T_{s2}) is (are) connected between an associated virtual earth point and an associated supply line (V_1, V_2) and in that two auxiliary transistors (T_{h1}, T_{h2}) having the same multiplication coefficient are connected between a respective supply line (V_1, V_2) and the in/ output (I/O) of the hybrid circuit and are incorporated in a current mirror circuit having at least one signal transistor (T_{s1}, T_{s2}), with junction points in the impedance circuit determining partial impedances being selected such that the hybrid balance condition is fulfilled.
2. A hybrid circuit as claimed in Claim 1, comprising a single signal transistor (T_s), characterized in that the impedance circuit (R_1, R_2, R_3) is connected between the in/output (I/O) and a single virtual earth point of the hybrid circuit, in that the one signal transistor (T_s) is connected between the one virtual earth point and a first supply line (V_2) and in that the two auxiliary transistors (T_{h1}, T_{h2}) having the same current coefficient through the one signal transistor (T_s) are connected between respectively the first and a second supply line (V_1, V_2) and the in/output (I/O) of the hybrid circuit and are incorporated in a current mirror circuit comprising one signal transistor (T_s).
3. A hybrid circuit as claimed in Claim 1, characterized in that the auxiliary transistors (T_{h1}, T_{h2}) are complementary.
4. A hybrid circuit as claimed in Claim 3, comprising a first signal transistor (T_{s1}) and a second signal transistor (T_{s2}) complementary to the first, characterized in that the impedance circuit ($R_1, R_2, R_3, -dR, 2dR, 2dR$) is connected between the in/output (I/O) and a first and a second virtual earth point (A_1, A_2) of the hybrid circuit, in that the first and second signal transistors (T_{s1}, T_{s2}) are connected between the first and second earth points (A_1, A_2) and a first and a second supply line (V_1, V_2), respectively, and in that a first and a second auxiliary transistor (T_{h1}, T_{h2}) having the same coefficient and this second transistor (T_{h2}) being complementary to the first one (T_{h1}) are connected between the first and the second supply line (V_1, V_2) and the in/output (I/O) of the hybrid circuit, respectively, for the current through the first and second signal transistor (T_{s1}, T_{s2}), respectively, and being incorporated in a current mirror circuit with the respective first and second signal transistors (T_{s1}, T_{s2}), the first signal transistor (T_{s1}) and auxiliary transistor (T_{h1}) being of the same polarity i.e. conductivity type.
5. A hybrid circuit as claimed in Claim 3, which is of a symmetrical configuration, characterized in that each half section comprises a signal transistor (T_{s1}) incorporated in a current mirror circuit with one of the auxiliary transistors (T_{h1}) of this half section, the other auxiliary transistor (T_{h2}) of this half section being incorporated in a current mirror circuit with the associated signal transistor (T'_{s1}) of the other half section.
6. A hybrid circuit as claimed in Claim 5, comprising a first and a second half section, each comprising a single signal transistor (T_s), characterized in that in each half section the impedance circuit (R_1, R_2, R_3) is connected between the in/output (I/O) and a virtual earth point (A) of the half section, in that the single signal transistor (T_s) is connected between the virtual earth point (A) and a first supply line (V_2) and in that the two auxiliary transistors (T_{h1}, T_{h2}) having the same coefficient for the current through the single signal transistor (T_s) are connected between the first and a second supply line (V_1, V_2) and the in/output (I/O) respectively, of the half section and are incorporated in a current mirror circuit with the single signal transistor, the single signal transistor (T_2) of the first half section being incorporated in a current mirror circuit comprising a first auxiliary transistor (T_{h2}) of this half section and the second auxiliary transistor of the second half section, the single signal transistor of the second half section being incorporated in a current mirror circuit comprising a first auxiliary transistor of this half section and the second auxiliary transistor of the first half section (T_{h2}).



Revendications

1. Circuit hybride comprenant une entrée (I), une sortie (O) et une entrée/sortie (I/O), au moins un transistor d'acheminement de signaux (T_{s1}), au moins un transistor auxiliaire (T_{h1}) incorporé en tant que multiplicateur de courant dans un circuit avec un transistor d'acheminement de signaux (T_{s2}) associé et un circuit d'impédance (R_1, R_2, R_3) incorporé dans un circuit avec un transistor d'acheminement de signaux (T_{s2}) associé, un point de jonction du circuit d'impédance étant connecté à la sortie (O) du circuit hybride, le circuit d'impédance, dans sa totalité, présentant une impédance en rapport avec le coefficient de multiplication du transistor auxiliaire (T_{h1}) qui est telle que le circuit hybride satisfait à la condition d'adaptation de ligne, caractérisé en ce que le circuit d'impédance (R_1, R_2, R_3) est connecté entre l'entrée/sortie (I/O) et au moins un point de mise à la terre virtuel du circuit hybride et comporte un autre point de jonction connecté à l'entrée (I) du circuit hybride, en ce que le ou les transistors d'acheminement de signaux (T_{s1}, T_{s2}) est ou sont connectés entre un point de mise à la terre virtuel associé et une ligne d'alimentation (V_1, V_2) associée et en ce que deux transistors auxiliaires (T_{h1}, T_{h2}) présentant le même coefficient de multiplication sont connectés entre une ligne d'alimentation (V_1, V_2) respective et l'entrée/sortie (I/O) du circuit hybride et sont incorporés dans un circuit formant miroir de courant qui comporte au moins un transistor d'acheminement de signaux (T_{s1}, T_{s2}), des points de jonction dans le circuit d'impédance déterminant des impédances partielles étant sélectionnés de façon telle que les conditions d'équilibre du circuit hybride soient remplies.
2. Circuit hybride suivant la revendication 1, comprenant un seul transistor d'acheminement de signaux (T_s), caractérisé en ce que le circuit d'impédance (R_1, R_2, R_3) est connecté entre l'entrée/sortie (I/O) et un point de mise à la terre virtuel unique du circuit hybride, en ce que le transistor d'acheminement de signaux (T_s) est connecté entre ledit point de mise à la terre virtuel et une première ligne d'alimentation (V_2) et en ce que les deux transistors auxiliaires (T_{h1}, T_{h2}) présentant le même coefficient de courant à travers ledit transistor d'acheminement de signaux (T_s) sont connectés entre respectivement la première et la seconde ligne d'alimentation (V_1, V_2) et l'entrée/sortie (I/O) du circuit hybride et sont incorporés dans un circuit formant miroir de courant comprenant un transistor d'acheminement de signaux (T_s).
3. Circuit hybride suivant la revendication 1, caractérisé en ce que les transistors auxiliaires (T_{h1}, T_{h2}) sont complémentaires.
4. Circuit hybride suivant la revendication 3, comprenant un premier transistor d'acheminement de signaux (T_{s1}) et un second transistor d'acheminement de signaux (T_{s2}) complémentaire du premier, caractérisé en ce que le circuit d'impédance ($R_1, R_2, R_3, -dR, 2dR, 2dR$) est connecté entre l'entrée/sortie (I/O) et un premier ainsi qu'un second point de mise à la terre virtuel (A_1, A_2) du circuit hybride, en ce que le premier et le second transistor d'acheminement de signaux (T_{s1}, T_{s2}) sont connectés entre le premier et le second point de mise à la terre (A_1, A_2) et une première ainsi qu'une seconde ligne d'alimentation (V_1, V_2) respectivement, et en ce qu'un premier et un second transistor auxiliaire (T_{h1}, T_{h2}) présentant le même coefficient et dont le second transistor (T_{h2}) est complémentaire du premier (T_{h1}) sont connectés entre la première et la seconde ligne d'alimentation (V_1, V_2) et l'entrée/sortie (I/O) du circuit hybride, respectivement, pour le courant traversant le premier et le second transistor d'acheminement de signaux (T_{s1}, T_{s2}) respectivement, et étant incorporés dans un circuit formant miroir de courant avec le premier et le second transistor d'acheminement de signaux respectifs (T_{s1}, T_{s2}), le premier transistor d'acheminement de signaux (T_{s1}) et le transistor auxiliaire (T_{h1}) étant de la même polarité, c'est-à-dire du même type de conductivité.
5. Circuit hybride suivant la revendication 3, qui est d'une configuration symétrique, caractérisé en ce que chaque demi-section comprend un transistor d'acheminement de signaux (T_{s1}) incorporé dans un circuit formant miroir de courant avec un des transistors auxiliaires (T_{h1}) de cette demi-section, l'autre transistor auxiliaire (T_{h2}) de cette demi-section étant incorporé dans un circuit formant miroir de courant avec le transistor d'acheminement de signaux (T_{s1}) associé de l'autre demi-section.
6. Circuit hybride suivant la revendication 5, comprenant une première et une seconde demi-section, comprenant chacune un seul transistor d'acheminement de signaux, caractérisé en ce que dans chaque demi-section, le circuit d'impédance (R_1, R_2, R_3) est connecté entre l'entrée/sortie (I/O) et un point de mise à la terre virtuel (A) de la demi-section, en ce que le transistor d'acheminement de



signaux unique (T_s) est connecté entre le point de mise à la terre virtuel (A) et une première ligne d'alimentation (V_2) et en ce que les deux transistors auxiliaires (T_{h1} , T_{h2}) présentant le même coefficient pour le courant traversant le transistor d'acheminement de signaux unique (T_2) sont connectés entre la première et une seconde ligne d'alimentation (V_1 , V_2) et l'entrée/sortie (I/O) respectivement de la demi-section et sont incorporés dans un circuit formant miroir de courant avec le transistor d'acheminement de signaux unique, le transistor d'acheminement de signaux (T_2) de la première demi-section étant incorporé dans un circuit formant miroir de courant comprenant un premier transistor auxiliaire (T_{h2}) de cette demi-section et le second transistor auxiliaire de la seconde demi-section, le transistor d'acheminement de signaux unique de la deuxième demi-section étant incorporé dans un circuit formant miroir de courant comprenant un premier transistor auxiliaire de cette demi-section et le second transistor auxiliaire de la première demi-section (T_{h2}).

Patentansprüche

1. Gabelschaltung mit einem Eingang (I), einem Ausgang (O) und einem Ein-/Ausgang (I/O), mindestens einem Signaltransistor (T_{s1}), mindestens einem Hilfstransistor (T_{h1}), ausgebildet als Stromvervielfacher in einer Schaltungsanordnung mit einem zugeordneten Signaltransistor (T_{s2}) und mit einer Impedanzschaltung (R_1 , R_2 , R_3) in einer Schaltungsanordnung mit einem zugeordneten Signaltransistor (T_{s2}), wobei ein Knotenpunkt der Impedanzschaltung mit dem Ausgang (O) der Gabelschaltung gekoppelt ist, wobei die Impedanzschaltung als Ganze eine derartige auf den Multiplikationsfaktor des Hilfstransistors (T_{h1}) bezogene Impedanz aufweist, daß die Gabelschaltung die Leitungsanpassungsbedingung erfüllt, dadurch gekennzeichnet, daß die Impedanzschaltung (R_1 , R_2 , R_3) zwischen dem Ein-/Ausgang (I/O) und mindestens einem virtuellen Erdungspunkt der Gabelschaltung vorgesehen ist und einen mit dem Eingang (I) der Gabelschaltung verbundenen weiteren Knotenpunkt hat, daß der (die) Signaltransistor(en) (T_{s1} , T_{s2}) zwischen einem zugeordneten virtuellen Erdungspunkt und einer zugeordneten Speiseleitung (V_1 , V_2) vorgesehen ist (sind) und daß zwei Hilfstransistoren (T_{h1} , T_{h2}) mit demselben Multiplikationsfaktor zwischen einer betreffenden Speiseleitung (V_1 , V_2) und dem Ein-/Ausgang (I/O) der Gabelschaltung vorgesehen und in eine Stromspiegelschaltung mit mindestens einem Signaltransistor (T_{s1} , T_{s2}) aufgenommen sind, wobei Teilimpedanzen bestimmende Knotenpunkte in der Impedanzschaltung derart gewählt worden sind, daß die Ausgleichsbedingung der Gabelschaltung erfüllt ist.
2. Gabelschaltung nach Anspruch 1 mit einem einzigen Signaltransistor (T_s), dadurch gekennzeichnet, daß die Impedanzschaltung (R_1 , R_2 , R_3) zwischen dem Ein-/Ausgang (I/O) und einem einzigen virtuellen Erdungspunkt der Gabelschaltung vorgesehen ist, daß der einzige Signaltransistor (T_s) zwischen dem einen virtuellen Erdungspunkt und einer ersten Speiseleitung (V_2) vorgesehen ist und daß die beiden Hilfstransistoren (T_{h1} , T_{h2}) mit demselben Stromkoeffizienten durch den einen Signaltransistor (T_s) zwischen einerseits der ersten und zweiten Speiseleitung (V_1 , V_2) und andererseits dem Ein-/Ausgang (I/O) der Gabelschaltung vorgesehen und in eine Stromspiegelschaltung mit einem Signaltransistor (T_s) aufgenommen sind.
3. Gabelschaltung nach Anspruch 1, dadurch gekennzeichnet, daß die Hilfstransistoren (T_{h1} , T_{h2}) komplementär sind.
4. Gabelschaltung nach Anspruch 3 mit einem ersten Signaltransistor (T_{s1}) und einem zweiten zu dem ersten komplementären Signaltransistor (T_{s2}), dadurch gekennzeichnet, daß die Impedanzschaltung (R_1 , R_2 , R_3 , $-dR$, $2dR$, $2dR$) zwischen dem Ein-/Ausgang (I/O) und einem ersten und zweiten virtuellen Erdungspunkt (A_1 , A_2) der Gabelschaltung vorgesehen ist, daß der erste und zweite Signaltransistor (T_{s1} , T_{s2}) zwischen dem ersten und zweiten Erdungspunkt (A_1 , A_2) und einer ersten bzw. zweiten Speiseleitung (V_1 , V_2) vorgesehen sind, und daß ein erster und zweiter Hilfstransistor (T_{h1} , T_{h2}), die denselben Koeffizienten haben und wobei der zweite Transistor (T_{h2}) zu dem ersten (T_{h1}) komplementär ist, zwischen der ersten bzw. zweiten Speiseleitung (V_1 , V_2) und dem Ein-/Ausgang (I/O) der Gabelschaltung für den Strom durch den ersten bzw. zweiten Signaltransistor (T_{s1} , T_{s2}) vorgesehen und in eine Stromspiegelschaltung mit dem betreffenden ersten und zweiten Signaltransistor (T_{s1} , T_{s2}) aufgenommen sind, wobei der erste Signaltransistor (T_{s1}) und der erste Hilfstransistor (T_{h1}) dieselbe Polarität haben, d.h. vom leitenden Typ sind.
5. Gabelschaltung nach Anspruch 3, die symmetrisch ist, dadurch gekennzeichnet, daß jede Hälfte einen Signaltransistor (T_{s1}) aufweist, der zusammen mit einem der Hilfstransistoren (T_{h1}) dieser Hälfte in eine



Stromspiegelschaltung aufgenommen ist, wobei der andere Hilfstransistor (T_{h2}) dieser Hälfte zusammen mit dem zugeordneten Signaltransistor (T_{s1}) der anderen Hälfte in eine Stromspiegelschaltung aufgenommen ist.

- 5 6. Gabelschaltung nach Anspruch 5 mit einer ersten und einer zweiten Hälfte, die je einen einzigen Signaltransistor (T_s) aufweisen, dadurch gekennzeichnet, daß in jeder Hälfte die Impedanzschaltung (R_1 , R_2 , R_3) zwischen dem Ein-/Ausgang (I/O) und einem virtuellen Erdungspunkt (A) der Hälfte vorgesehen ist, daß der einzige Signaltransistor (T_s) zwischen dem virtuellen Erdungspunkt (A) und einer ersten Speiseleitung (V_2) vorgesehen ist und daß die beiden Hilfstransistoren (T_{h1} , T_{h2}) mit demselben Koeffizienten für den Strom durch den einzigen Signaltransistor (T_s) zwischen der ersten bzw. einer zweiten Speiseleitung (V_1 , V_2) und dem Ein-/Ausgang (I/O) der Hälfte vorgesehen und in eine Stromspiegelschaltung mit dem einzigen Signaltransistor aufgenommen sind, wobei der einzige Signaltransistor (T_s) der ersten Hälfte in eine Stromspiegelschaltung mit einem ersten Hilfstransistor (T_{h2}) dieser Hälfte und dem zweiten Hilfstransistor der zweiten Hälfte aufgenommen ist, wobei der einzige Signaltransistor der zweiten Hälfte in eine Stromspiegelschaltung mit einem ersten Hilfstransistor dieser Hälfte und dem zweiten Hilfstransistor (T_{h1}) der ersten Hälfte aufgenommen ist.

