

**TITLE: POLYCRYSTALLINE SILICON CARBIDE SUPPORT FOR A
SUBSTRATE INTENDED TO RECEIVE POWER SEMICONDUCTOR DEVICES
AND SUBSTRATE COMPRISING SUCH A SUPPORT**

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FIELD OF THE INVENTION

The present invention relates to substrates intended to receive semiconductor devices, notably devices for applications requiring high electrical power. This can involve devices based on III-N materials, such as gallium nitride. The invention also relates to a support particularly adapted to form such a substrate.

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TECHNOLOGICAL BACKGROUND OF THE INVENTION

Some of the applications of transistors based on III-N materials, of the HEMT ("High Electron Mobility Transistor") type are in the field of managing high electrical power, for example, such as switches in power converters.

As schematically shown in figure 1, such a component 1 conventionally uses:

- a substrate 2, which typically can be a silicon, sapphire or silicon carbide wafer;
- a buffer layer 3, generally doped in order to be semi-insulating, formed on the substrate 2;
- a heterojunction made up of a GaN channel layer 5 and an AlGaN barrier layer 6 successively formed on the buffer layer;

- source S, drain D and gate G electrode structures on/in the heterojunction;
- a metal sheet M in ohmic contact with the rear face of the support 2. The sheet M can be the copper lead frame of a housing for a semiconductor chip. An adhesion layer B, for example, a silver sintering paste, can be used to make the rear face of the support 2 reliably adhere to the metal sheet M.

10 The metal sheet M helps to promote the discharge of the heat generated at the heterojunction when the device is operating. Generally, the source electrode S is electrically connected to the substrate 2, so as to prevent the potential of this substrate from remaining floating. The electrically

15 conducting state of the transistor between the source S and the drain D is controlled by the voltage applied to the gate G. In the case of power applications, the voltage V_{DS} applied across the terminals of the source S and drain D electrodes can then reach a few hundred volts to several thousand volts

20 when the transistor is turned off. The leakage current flowing between the source S and the drain D in the off state is low, of the order of a few nanoamperes. On the contrary, in the on state, several amperes can flow between the source S and the drain D. Furthermore, switching between the on

25 state and the off state is very fast, of the order of a few nanoseconds.

However, several problems limit the dissemination of this technology.

As has been seen, in the off state, a high voltage is applied across the terminals of the source S and drain D electrodes. This leads to the formation of an electric field, the lines of which penetrate very deeply into the buffer layer 3 and the substrate 2. An electric field then develops between the drain electrode D and the substrate 2, notably in the thickness of the buffer layer 3, and between the source S and the drain D. In order to prevent the intensity of this field from exceeding the critical value (called breakdown field) beyond which it can no longer be supported by the material, provision must be made for the drain D and the source S to be separated by a sufficient distance d so that, for a given voltage V_{DS} , the field intensity $E = V_{DS}/d$ is less than the breakdown field. Similarly, provision can be made to provide a buffer layer 3 that is thick enough so that the value of the electric field at the interface between the buffer layer 3 and the substrate 2 is less than the permissible limit for the relevant materials.

It is relatively easy to select the distance d separating the drain electrode D from the source S when designing the transistor. Thus, for a voltage V_{DS} of the order of 400 V to 2,000 V, a distance d of the order of 5 to 20 microns can be selected. However, there are limits to increasing this distance, as it tends to increase the size of the HEMT device and therefore make it more expensive and less compact.

Providing a device 1 with a thick enough buffer layer 3 of III-N materials (of the order of 3 or more microns) is, however, much more difficult, notably when the substrate 2 is selected from large-scale silicon (200 mm diameter) rather

than sapphire, for availability and cost reasons. This is notably due to the difference between the thermal expansion coefficient of silicon and that of the III-N material that forms the buffer layer. This layer is produced by high temperature deposition onto the silicon substrate, and returning to room temperature subjects this layer to very high stresses, which can lead to cracking, or even breakage, of the substrate if the stresses are too great. It is generally difficult to provide a buffer layer that is more than 3 microns thick on a silicon substrate in the form of a 200 mm wafer.

Naturally, an attempt could be made to replace the silicon substrate with a substrate with a thermal expansion coefficient closer to that of the buffer layer material in order to overcome this constraint. This could involve using a silicon carbide substrate, for example. However, apart from the fact that this material in its crystalline form is particularly scarce and expensive, it also must be metallised and treated in order to form an ohmic contact with the metal sheet M. The document entitled, "Ohmic contacts to SiC", in the International Journal of High Speed Electronics and Systems, Vol. 15, No. 04, pp. 781-820 (2005), states that metal layer-SiC contact is generally non-ohmic immediately after the metal layer has been deposited. This interface then needs to be thermally treated, for example, using a laser, in order to promote the formation of silicides, carbides or ternary phases, making the contact effectively ohmic. Simplifying how the device is housed would be beneficial.

Documents US 2013/0112997, EP 3351660 and US 2005/0269671 propose substrates comprising polycrystalline silicon carbide supports.

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SUBJECT MATTER OF THE INVENTION

An aim of the invention is to propose a support for a substrate intended to receive a power semiconductor device that at least partly addresses these problems. More specifically, an aim of the invention is to propose a support for a substrate capable of receiving a relatively thick buffer layer, preferably having a thickness that is greater than or equal to 5 microns, and which can be simply integrated into a housing, without having to apply heat treatment to the face that receives the adhesion layer. An aim of the invention is to provide a substrate that uses such a support and a semiconductor device formed on/in such a substrate.

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BRIEF DESCRIPTION OF THE INVENTION

In order to achieve one of these aims, the subject matter of the invention proposes a polycrystalline silicon carbide support for a substrate intended to receive a power semiconductor device. The support comprises a first face, denoted "front face", and a second face opposite the first and denoted "rear face". The support comprises:

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- a first surface layer disposed directly under the front face and having resistivity that is greater than or equal to 1 ohm.cm; and
- a second surface layer disposed directly under the rear face and having resistivity that is strictly less than 1 ohm.cm.

According to other advantageous and non-limiting features of the invention, taken individually or according to any technically feasible combination:

- the minimum thickness of the second layer is 10 or more micrometres;
- the second layer has a concentration of n-type dopants, such as nitrogen, that is greater than 10^{20} at/cm³;
- the concentration of n-type dopants monotonically increases from the front face to the second surface layer;
- the first layer is not intentionally doped or has a vanadium concentration that is greater than 10^{15} at/cm³;
- the total thickness of the support, between the first face and the second face, ranges between 200 micrometres and 1 mm;
- the support is in the form of a circular wafer, advantageously with a 200 mm diameter.

According to another aspect, the subject matter of the invention proposes a substrate intended to receive a semiconductor device comprising a support as described above
5 and a seed layer, transferred onto the front face of the support.

According to other advantageous and non-limiting features of this aspect of the invention, taken alone or according to
10 any technically feasible combination:

- the seed layer is made up of gallium nitride, silicon carbide, sapphire or silicon (1,1,1);
- 15 - the substrate comprises a dielectric bonding layer disposed between, and in contact with, the support and the seed layer, preferably a dielectric bonding layer made of silicon nitride;
- 20 - the seed layer is in direct contact with the substrate;
- a gallium nitride-based buffer layer, which preferably is semi-insulating, is disposed on the seed layer;
- 25 - the buffer layer is more than 3 microns thick, preferably more than 5 micrometres thick and even more preferably ranges between 5 micrometres and 10 micrometres thick;
- 30 - the substrate comprises a heterojunction disposed on the buffer layer, the heterojunction comprising a

channel layer and a barrier layer and being capable of forming a 2D electron gas.

5 According to yet another aspect, the invention proposes a semiconductor component comprising a substrate as described above and a source structure, a drain structure and a gate structure disposed on the heterojunction.

10 Advantageously, a metal sheet is disposed under the rear face of the substrate, in ohmic contact with a metal layer deposited onto the second surface layer. An adhesion layer, such as a silver sintering paste layer, can be disposed between the metal sheet and the metal layer deposited onto the second surface layer.

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BRIEF DESCRIPTION OF THE DRAWINGS

20 Further features and advantages of the invention will become apparent from the following detailed description of the invention, with reference to the appended figures, in which:

[Fig. 1]

25 Figure 1 shows a substrate provided with an HEMT transistor according to the prior art;

[Fig. 2a] [Fig. 2b]

30 Figures 2a, 2b show two substrates intended to receive semiconductor devices according to the invention;

[Fig. 3]

Figure 3 shows a semiconductor component formed from a substrate according to the invention.

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DETAILED DESCRIPTION OF THE INVENTION

In order to simplify the following description, the same reference signs are used for elements that are identical or that provide the same function in the various embodiments of the invention or in the disclosure of the prior art.

Figures 2a, 2b show two embodiments of a substrate 2 intended to receive a power semiconductor device and which is the subject matter of the present description. As briefly disclosed in the introduction to this application, this substrate 2 is intended to receive at least one device comprising a buffer layer made of III-N material that is several microns thick, a heterojunction comprising a channel layer and a barrier layer on the buffer layer and source, drain and gate structures disposed on the heterojunction.

The substrate 2, when it is still devoid of devices, is advantageously in the form of a circular wafer, the diameter of which is standardised so that it can be handled by standard equipment in the semiconductor industry. Advantageously, a 200 mm diameter is selected.

After the steps of forming the devices and the singularisation thereof, as is well known per se, chips are formed that are intended to integrate housings for forming

a semiconductor component. The substrate 2, when it is incorporated into a chip, then assumes the form of a rectangular parallelepiped with sides of the order of mm or cm.

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General presentation of the substrate 2

Irrespective of the shape adopted by the substrate 2, in very general terms it comprises a support 2a and a seed layer 2c transferred onto the support 2a. In the embodiment of figure 2a, a dielectric bonding layer 2b is disposed between, and in contact with, the support 2a and the seed layer 2c. In the embodiment of figure 2b, the substrate 2 is devoid of a dielectric bonding layer and the seed layer 2c is directly transferred onto the support 2a, in contact with this support 2a.

The support 2a is entirely made up of polycrystalline silicon carbide. It comprises a first face, denoted "front face", and a second face opposite the first and denoted "rear face". The seed layer is transferred onto the front face of the substrate, either directly or via the dielectric bonding layer 2c. The main function of the support 2a is to mechanically support the remainder of the stack leading to the formation of a functional semiconductor component, as will be disclosed in a subsequent section of this detailed description. To this end, the thickness thereof, measured between its front face and its rear face, is relatively high, typically ranging between 200 micrometres and 1 mm.

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The function of the seed layer 2c, for its part, is to provide an exposed surface of the substrate 2 that is capable of receiving the buffer layer 3 of the device. The nature of this layer is therefore selected so as to provide a lattice parameter adapted to that of the III-N material forming the buffer layer 3, typically gallium nitride, in order to facilitate its epitaxial growth on the substrate 2. This therefore can involve gallium nitride, silicon carbide, sapphire or silicon (1,1,1), in all cases in their monocrystalline form. This seed layer 2c does not need to be thick, as only its surface properties are exploited, and a relatively low thickness of less than 2 micrometres is therefore selected.

The purpose of the dielectric bonding layer 2c is to facilitate the manufacture of the substrate 2, as will be disclosed hereafter. It is preferable for a dielectric material with a good thermal diffusion coefficient to be selected, such as silicon nitride, and for its thickness to be minimised, preferably less than 1 micrometre, so as not to affect the thermal properties of the substrate 2, as will be explained hereafter.

It should be noted that the seed layer 2c is much thinner than the thickness of the support 2a. As a result, and due to the compliance effect, it undergoes the deformations imposed thereon by the support 2a, when, for example, the substrate 2 is exposed to significant temperature variations of several hundred degrees, as is the case during the epitaxial formation of the buffer layer 3. In other words, the deformation of the substrate 2 generated by its exposure

to a significant temperature variation is dictated by the behaviour of the substrate 2a. The thickness of the seed layer is preferably selected so as to be relatively low, less than 2 micrometres as already stated, in order to
5 promote this compliance effect.

It also should be noted that the polycrystalline silicon carbide from which the support 2a is formed has a thermal expansion coefficient close to that of the III-N material
10 forming the buffer layer 3, notably when this buffer layer 3 is made of gallium nitride. Also, after the high-temperature epitaxial formation of the buffer layer 3, and when the substrate 2 provided with this layer is brought back to room temperature, minimal stresses develop in the
15 structure. It is therefore possible to form a buffer layer 3 that is much thicker than that which can be formed on a silicon substrate of the prior art. Notably, a buffer layer 3 can be formed that is at least 3 micrometres thick, preferably that is more than 5 micrometres thick and even
20 more preferably that ranges between 5 micrometres and 10 micrometres thick.

Finally, the polycrystalline silicon carbide from which the support 2a is formed (which represents most of the substrate
25 2), has thermal diffusion properties that allow the heat produced in the device to be dissipated efficiently. By way of a reminder, since this device is preferably designed to deal with a significant amount of electrical power, it tends to heat up, and the heat that is produced needs to be
30 discharged to avoid affecting the correct operation thereof. Thus, the thermal diffusion coefficient of polycrystalline

silicon carbide is approximately three times greater than that of the silicon forming a substrate of the prior art. By improving the thermal conductivity of the substrate 2 compared with a substrate of the prior art, it is also possible to increase the power density processed by the device.

According to an important feature of the substrate 2a, it comprises a first surface layer C1, disposed directly under the front face, which has resistivity that is greater than or equal to 1 ohm.cm, and advantageously that is greater than 10^3 ohms.cm. In the presence of a high intensity electric field with lines that extend into the depth of the substrate 2, and notably into this first surface layer C1 of the support, the resistive nature of this first surface layer C1 allows the breakdown voltage to be removed. The device can therefore withstand high drain-source voltages, in excess of 1,000 V, without risking any damage to the device.

In order to obtain these resistivity values, the first layer C1 is intrinsic, i.e., it is not intentionally doped. Alternatively, it can be doped with vanadium at a concentration of more than 10^{15} at/cm³, in order to further increase its resistivity.

The substrate 2a also comprises a second surface layer C2, this time disposed directly under the rear face. This second surface layer C2 has resistivity of strictly less than 1 ohm.cm, and can be less than 50 milliohm.cm or 10 milliohm.cm. This low resistivity, which can be obtained by n-type doping in a concentration of dopants (for example,

nitrogen) that is greater than 10^{20} at/cm³, allows the rear face of the substrate to be provided with almost metallic behaviour, and therefore allows a layer of metal or metal alloys to be received, by deposition, without requiring heat treatment before applying a method for assembling this face on a metal sheet, during the encasing step.

This second surface layer C2 does not need to be very thick, but it nevertheless is more than 10 micrometres thick.

Preferably, the first layer C1 extends into the depth of the substrate 2 as far as the second highly doped layer C2. Of course, a transition zone can exist between these two layers C1, C2, in order to control the doping gradient required for this transition. Notably, it is possible to contemplate that the concentration of n-type dopant in the substrate 2a monotonically increases from the front face to the second surface layer C2.

However, in all cases, and irrespective of the way in which the dopants are distributed in the thickness of the support 2a, the support has a first surface layer C1 disposed directly under the front face, as close as possible to the device, which is resistive or highly resistive in order to counter the effects of the electric fields that can develop therein. The support 2a also has a second surface layer C2, disposed directly under the rear face, with very low resistivity in order to provide it with metallic behaviour that promotes the reliable assembly thereof on a metal sheet when encasing the device.

Manufacturing the polycrystalline silicon carbide substrate

- Manufacturing a polycrystalline silicon carbide substrate according to the invention, and therefore having the first and second surface layers C1, C2, uses a chemical vapour deposition (CVD) technique. This technique uses a gas mixture comprising at least one silicon precursor gas (such as a silane or a chlorosilane) and/or at least one carbon precursor gas (such as an alkane or an alkene), and/or at least one silicon and carbon precursor gas (such as methyltrichlorosilane, abbreviated to MTCS) in order to form the bulk part of the support 2a.
- It also uses at least one n-type doping gas to form at least the second surface layer C2. In the case of nitrogen doping of this second surface layer C2, the doping gas can be NH_3 , N_2H_4 , N_2 , for example.
- For vanadium doping of the first surface layer C1, if such doping is provided, a vanadium chloride doping gas (VCl_2 , for example) can be used.
- These gases can be diluted in a carrier gas, which can be a reducing gas such as hydrogen and/or an inert gas such as argon. The polycrystalline silicon carbide layer is formed from this gas mixture on a substrate, called "growth" substrate.
- The gaseous mixture is admitted into a reactor at high temperature where the precursor gases are decomposed and

react on the surface of the growth substrate, preferably made of purified fine-grained isostatic graphite, in order to form a layer of polycrystalline silicon carbide, for example, of 3C polytype, the mechanical and thermal resistance properties, the thermal expansion coefficient and the purity of which are perfectly adapted to its use as a support 2a for the substrate 2. 3C polytype also can be doped with nitrogen at very high levels, of the order of 10^{20} atoms/cm³, and thus can have resistivity of less than 10mOhm.cm.

The reactor temperature during the CVD deposition of the silicon carbide must be between approximately 1,000°C and approximately 1,600°C, preferably between approximately 1,100°C and approximately 1,400°C, or even between 1,200°C and approximately 1,400°C. Within this temperature range, the deposition rates can vary over fairly wide ranges, from a micron/hr to more than 100 micron/hr. Advantageously, the total pressure in the reactor does not exceed 350 mbar, or even 300 mbar.

In order to form a substrate 2a according to the invention, the flow of n-type doping gas is controlled so as to form, at the start of the growth process, optionally after the formation of a seed thickness on the graphite surface, a layer of doped polycrystalline silicon carbide that is thick enough to eventually form, after all the finishing steps described hereafter, the second surface layer C2 of the support 2a. This can involve forming an n-type doped layer during this growth process, which is 2 to 10 times thicker than the thickness expected in this support, which by way of

a remainder is typically greater than 10 micrometres after any thinning of the substrate.

During this deposition phase, after forming the highly n-doped thickness, the flow of n-type doping gas can be interrupted in order to form the remainder of the thickness of intrinsic polycrystalline silicon carbide, which is not intentionally doped. Alternatively, a flow of vanadium-based doping gas can be circulated in order to further increase the resistivity of the material intended to form the first surface layer C1.

On completion of this deposition phase, the graphite growth substrate, coated with a polycrystalline silicon carbide deposition layer, is machined and then oxidised in air, typically at 900 °C, in order to remove any graphite residue and to provide a rough disc of polycrystalline silicon carbide. It should be noted that the graphite also could be removed using purely mechanical machining techniques or even basically by burning/oxidation.

It should be noted that it is possible, during the deposition phase, for a very thick polycrystalline silicon carbide to be formed in order to form an ingot of material. Slices then can be cut from this ingot, with each slice forming a rough silicon carbide disc. In this approach, heavily n-doped interlayers (which will be used to form second surface layers C2) will be carefully inserted between intrinsic or vanadium-based doped layers (which will be used to form first surface layers C1) when growing the ingot. The ingot will be cut at positions that allow, after all the finishing steps described

hereafter, supports to be formed in accordance with the invention.

5 In any case, a rough polycrystalline silicon carbide disc resulting from the deposition phase is then mechanically and thermally treated in order to form the support 2a with the selected dimensions. This can involve thinning steps using coarse and then fine grinding. These steps can be followed by a polishing step in order to provide a satisfactory
10 surface finish in terms of roughness. These grinding or polishing steps, which are known in the prior art, are notably intended for removing enough thickness from the side of the disc face that was in contact with the graphite, in order to remove the initial crystal growth zone, which
15 generates high stresses. They also allow, by removing material from both sides of the rough disc, a polycrystalline silicon carbide support 2a to be obtained in the form of a wafer, for example, a wafer with a diameter of 200 mm and a thickness typically ranging between 350 micrometres and 500
20 micrometres, but which can extend, for example, between 200 nm and 1 mm.

Manufacturing the substrate 2

25 In very general terms, the substrate 2 can be produced using a manufacturing method by transferring a seed layer onto the support 2a, the preparation of which has been described above. Such a transfer method comprises:

- assembling, optionally via a dielectric bonding layer 2b,
30 the first face of the support 2a and a main face of a donor substrate in order to form an intermediate structure;

- removing part of the donor substrate from the intermediate structure in order to define the seed layer 2c, transferred onto the support 2a.

5 The dielectric bonding layer 2b can be formed, by deposition and prior to the assembly step, on the donor substrate or on the front face of the support 2a or partly on either of these elements. The dielectric bonding layer 2b thus can be produced using an LPCVD (Low Pressure Chemical Vapour
10 Deposition) or PECVD (Plasma Enhanced Chemical Vapour Deposition) technique. As already stated, this layer is advantageously made of silicon nitride, for thermal diffusivity reasons.

15 The term "donor substrate" is understood to mean a substrate made of the material of the seed layer 2c, or comprising a surface thickness of this material. Thus, the donor substrate can be formed, by way of an example, from a solid substrate of monocrystalline gallium nitride, of monocrystalline
20 silicon (1,1,1), of sapphire or (1,1,1) of monocrystalline silicon carbide. By way of an additional example, it can assume the form of a composite substrate formed by a first substrate that supports a thickness (at least equal to that of the seed layer 2c) of the material intended to form the
25 seed layer. This notably can be a thickness of a III-N material such as gallium nitride formed on a silicon substrate (1,1,1).

The assembly step of the layer transfer manufacturing method
30 is advantageously implemented by molecular adhesion. As is well known per se, during a molecular adhesion method, the

first face of the support 2a and a face of the donor substrate (optionally both covered with a dielectric layer intended to form the dielectric bonding layer 2b), which are perfectly clean, flat and smooth, are brought into close contact in order to promote the development of molecular bonds, for example, of the Van der Waals or covalent type. The assembly of the two bodies is then achieved without using an adhesive. These bonds can be strengthened by applying heat treatment to the intermediate structure thus formed. When the intention is to form a substrate 2 devoid of a dielectric bonding layer, the first face of the support 2a and the face of the donor substrate are not provided with a dielectric layer, and are brought into close contact directly with each other.

The step of removing part of the donor substrate can be carried out by chemical-mechanical thinning of this substrate.

Preferably, however, the substrate 2 is manufactured by applying Smart Cut™ technology, according to which a layer intended to form the seed layer 2c is delimited via a weakened plane formed by implanting "light" species (typically hydrogen and/or helium) in the donor substrate. After the assembly step, this layer is removed from the donor substrate by fracturing in the vicinity of the weakened plane and is thus transferred onto the substrate 2a.

Whether the removal of a portion of the thickness of the donor substrate is carried out by thinning or by fracturing, it is possible to apply any type of finishing treatment to the substrate thus formed in order to adapt the seed layer

2c to thickness, thickness uniformity or roughness specifications or to any other type of specifications.

5 In the substrate 2 thus formed, the rear face of the support 2, under which the second surface layer C2 is disposed, also forms the rear face of the substrate. The first surface layer C1, for its part, is disposed directly under the seed layer 2c (or directly under the dielectric bonding layer 2b, when this layer is present).

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It should be noted that when the material of the donor substrate is a polar material, then a dual transfer of the seed layer 2c taken therefrom needs to be carried out, initially by transferring this seed layer 2c to an intermediate substrate and then, during a second transfer phase, transferring it to the polycrystalline silicon carbide support 2a. In this way, the seed layer 2c has its initial polarity on this support 2a. This is notably the case when the donor substrate comprises gallium nitride, with this material having, in its most widely available form, a gallium face, the exposure of which is generally desired, and a nitrogen face.

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Manufacturing the semiconductor component

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The substrate 2, in the form of a wafer, is used to form at least one semiconductor component. Thus, and as disclosed in a previous section and illustrated in figure 3, a buffer layer 3 based on III-N material is formed by epitaxy on the exposed face of the seed layer 2c of the substrate 2. Preferably, the main layer 3 is doped in order to make it

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semi-insulating. This can involve, for example, carbon doping, the concentration of which in the main layer can range between $5 \cdot 10^{18}$ and $5 \cdot 10^{19}$ at/cm³. It also can be another form of p-type doping, for example, iron or
5 magnesium.

Provision can be made to place one or more interlayers, for example, made of AlGa_N or, more generally, of AlInGa_N, in the buffer layer 3, which is mainly made of gallium nitride.
10 In any case, the lattice parameter of the seed layer 2c and the thermal expansion coefficient of the polycrystalline silicon carbide support 2a are particularly adapted to the nature of the material of the buffer layer 3 made of III-N material. It is therefore possible to form a relatively high
15 thickness of this buffer layer 3 on the substrate 2, for example, a thickness of more than 3 micrometres, preferably of more than 5 micrometres and even more preferably ranging between 5 micrometres and 10 micrometres.

20 In a subsequent step of preparing the semiconductor component 1, a heterojunction is formed on the buffer layer 3. As is well known, such a heterojunction combines at least one channel layer 5 (for example, made of Ga_N) and a barrier layer 6 (for example, made of AlGa_N). A 2D electron gas is
25 likely to develop at the interface of these two layers. A source structure S, a drain structure D and a gate structure G are then disposed on the heterojunction 5.

It is possible to electrically connect the source structure
30 S to the second surface layer C2 in order to use said layer as a ground plane for the semiconductor component 1.

In some cases, provision can be made to thin the substrate 2, by removing a thickness from the support 2a on the side of the second surface layer C2. However, care must be taken
5 to maintain a sufficient thickness for this layer C2 that is greater than or equal to 10 microns.

In a subsequent step, a metal layer is formed on the rear face of the substrate 2a, in contact with the second surface
10 layer C2. This metal layer can be of any suitable type, for example, titanium, aluminium, nickel, gold or a stack formed by these materials. Due to the high doping of the second surface layer C2 and its low resistivity, the contact with the metal layer is ohmic, without having to thermally treat
15 this interface, which is a particularly advantageous feature of a support according to the invention.

A large number of devices is usually collectively formed on the substrate 2 in the form of wafers. These devices are
20 then singulated by cutting the wafer they are resting on in order to form semiconductor chips. These chips are encased in order to form semiconductor components 1, assembled on a metal sheet M using an adhesive, such as a silver sintering paste, forming an adhesion layer B that is particularly
25 reliable for a power component.

Of course, the invention is not limited to the embodiments described, and alternative embodiments can be used without departing from the scope of the invention as defined by the
30 claims.

CLAIMS

1. Polycrystalline silicon carbide support (2a) for a substrate (2) intended to receive a power semiconductor device, the support comprising a first face, denoted "front face", and a second face opposite the first and denoted "rear face", the support comprising:
- a first surface layer (C1) disposed directly under the front face and having resistivity that is greater than or equal to 1 ohm.cm; and
 - a second surface layer (C2) disposed directly under the rear face and having resistivity that is strictly less than 1 ohm.cm.
2. Polycrystalline silicon carbide support (2a) according to the preceding claim, wherein the second surface layer (C2) is 10 or more micrometres thick.
3. Polycrystalline silicon carbide support (2a) according to any of the preceding claims, wherein the second surface layer (C2) has a concentration of n-type dopants, such as nitrogen, that is greater than 10^{20} at/cm³.
4. Polycrystalline silicon carbide support (2a) according to the preceding claim, wherein the concentration of n-type dopants monotonically increases from the front face to the second surface layer (C2).

5. Polycrystalline silicon carbide support (2a) according to any of the preceding claims, wherein the first surface layer (C1) is not intentionally doped or has a vanadium concentration that is greater than 10^{15} at/cm³.
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6. Polycrystalline silicon carbide support (2a) according to any of the preceding claims, having a total thickness, between the first face and the second face, ranging between 200 micrometres and 1 mm.
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7. Polycrystalline silicon carbide support (2a) according to any of the preceding claims, in the form of a circular wafer, advantageously with a diameter of 200 mm.
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8. Substrate (2) intended to receive a semiconductor device, comprising a support (2a) according to any of the preceding claims and a seed layer (2c) transferred onto the front face of the support (2a).
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9. Substrate (2) according to the preceding claim, wherein the seed layer (2c) is made up of gallium nitride, silicon carbide, sapphire or silicon (1,1,1).
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10. Substrate (2) according to any of the two preceding claims, comprising a dielectric bonding layer (2b) disposed between, and in contact with, the support (2a) and the seed layer (2c), preferably a dielectric bonding layer (2b) made of silicon nitride.
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11. Substrate (2) according to Claim 8 or 9, wherein the seed layer (2c) is in direct contact with the support (2a).
- 5 12. Substrate (2) according to any of claims 8 to 11, comprising a gallium nitride-based buffer layer (3), which preferably is semi-insulating, disposed on the seed layer (2c).
- 10 13. Substrate (2) according to the preceding claim, wherein the buffer layer (3) is more than 3 microns thick, preferably more than 5 micrometres thick and even more preferably ranges between 5 micrometres and 10 micrometres thick.
- 15 14. Substrate (2) according to any of claims 12 and 13, comprising a heterojunction disposed on the buffer layer (3), the heterojunction comprising a channel layer (5) and a barrier layer (6) and being capable of forming a 2D electron gas.
- 20 15. Semiconductor component (1), comprising a substrate (2) according to the preceding claim and a source structure (S), a drain structure (D) and a gate structure (G) disposed on the heterojunction.
- 25 16. Semiconductor component (1) according to the preceding claim, comprising a metal sheet (M) disposed under the rear face of the substrate, in ohmic contact with the second surface layer (C2).
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17. Semiconductor component (1) according to the preceding claim, comprising an adhesion layer (B), such as a silver sintering paste layer, disposed between the metal sheet (M) and the second surface layer (C2).

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18. Semiconductor component (1) according to any of the two preceding claims, comprising a metal layer disposed against the second surface layer (C2).