CLAIMS

1. A method of manufacturing a lead frame including a lead frame main body and a plating film on a surface thereof, the method comprising:

a plating step of

performing plating treatment to dispose a first electrode connected to a polarity inversion power source so as to face a first main face of a lead frame main body and to dispose a second electrode connected to a pulse power source so as to face a second main face opposite to the first main face and

forming the plating film on the first main face, the second main face, and a side face of the lead frame main body.

2. The method of manufacturing a lead frame according to claim 1, wherein the plating film on the first main face has a larger roughness than the plating film on the second main face.

3. The method of manufacturing a lead frame according to claim 1 or 2, wherein the duty ratio of the pulse power source in the plating step is 0.2 to 0.85.

4. The method of manufacturing a lead frame according to any one of claims 1 to 3, wherein the average current density of the pulse power source in the plating step is 1 to 10 A/dm^2.

5. The method of manufacturing a lead frame according to any one of claims 1 to 4, wherein, when roughnesses of the plating films on the first main face, the second main face and the side face are denoted by S_1, S_2, and S_3, respectively, S_1 is 1.4 or more, S_2 is in a range of 1.0 and 1.2, and S_3 is 1.3 or more.

6. The method of manufacturing a lead frame according to claim 5,

wherein $S_3/S_1 < 1$ is satisfied.

7. A method of manufacturing a lead frame package using the lead frame manufactured by the manufacturing method according to any one of claims 1 to 6, the method of manufacturing a lead frame package comprising:

a step of providing a semiconductor chip on a first main face of the lead frame; and

a step of sealing at least the semiconductor chip with a resin so as to cover the semiconductor chip and the first main face and a side face of the lead frame and to expose at least a portion of a second main face having a smaller roughness than the first main face and the side face of the lead frame.

8. A lead frame comprising:

a lead frame main body; and

a plating film on a surface thereof,

wherein, when roughnesses of plating films on a first main face, a second main face opposite to the first main face, and a side face are denoted by S_1, S_2, and S_3, respectively, S_1 is 1.4 or more, S_2 is in a range of 1.0 and 1.2, S_3 is 1.3 or more, and $S_3/S_1 < 1$ is satisfied.

9. A lead frame package comprising:

the lead frame according to claim 8;

a semiconductor chip on the first main face of the lead frame; and

a sealing resin provided so as to cover the semiconductor chip and the first main face and the side face of the lead frame and to expose at least a portion of the second main face having a smaller roughness than the first main face and the side face of the lead frame.