

Description

The invention relates to an amplifier arrangement for amplifying an input signal, the arrangement comprising an input terminal for receiving the input signal, a first transistor having a control electrode, a first main electrode coupled to a first supply-voltage terminal, and a second main electrode, a second transistor having a control electrode, a first main electrode coupled to the second main electrode of the first transistor, and a second main electrode coupled both to a second supply-voltage terminal via a first current source and to an output terminal for supplying an output signal, the control electrode of the second transistor being coupled to an output of an amplifier, the second main electrode of the first transistor being coupled to an inverting input of the amplifier, and a non-inverting input of the amplifier being coupled to a first reference-voltage terminal for receiving a first reference voltage.

Such an amplifier arrangement is known from Japanese patent application JP-A-59-12603. In general, such an amplifier arrangement can be used for amplifying a voltage in integrated semiconductor circuits. The first and second transistors are connected in cascode arrangement, as is known inter alia from the book "CMOS analog circuit design" by P.E. Allen and D.R. Holberg, published in 1987, see Fig. 6.3-1 on page 288. Fig. 1 shows this known cascode amplifier arrangement in which the control electrode of the second transistor N2 is coupled to a reference voltage V_{ref1} . The first transistor N1 converts the input voltage V_{in} applied at its control electrode into a current which is proportional to the input voltage and which produces potential variations on the first main electrode of the second transistor N2. These variations, amplified by the gain factor of the second transistor N2, appear on the output terminal 3 of the amplifier arrangement. The overall gain is therefore equal to the product of the gain factors of the first transistor N1 and the second transistor N2. Consequently, the second transistor N2 makes the gain of the arrangement higher than that of an amplifier arrangement comprising only one transistor. This also results in an increased output impedance. In order to achieve a large unity-gain-bandwidth by means of this cascode arrangement large bias currents and transistors having a very short channel length are needed. However, this results in the output impedance and hence the gain being reduced substantially. Consequently, this known cascode arrangement is not capable of providing both a large unity-gain-bandwidth and a high gain.

In order to provide both a high gain and a large unity-gain-bandwidth the above mentioned Japanese patent application discloses a cascode arrangement wherein, as shown in Fig. 2, the control electrode of the second transistor N2 is coupled to an output VO

of an amplifier A, the second main electrode of the first transistor N1 is coupled to an inverting input V2 of the amplifier A and a first reference-voltage terminal 2 is coupled to a non-inverting input V1 of the amplifier. A quite similar approach is known from Electronic Engineering, Vol. 53, No. 647, January 1981, pages 59, 63-65, London GB, M.A. Rehman, MOS-FET Analog integrated circuits Part 3.

In the cascode arrangement known from the Japanese patent application the potential of the first main electrode of the second transistor N2 is maintained substantially constant by employing the amplifier A. This is achieved by negative feedback of the potential variations on said electrode to the control electrode of the second transistor N2 via the amplifier A. This causes the gain of the amplifier arrangement to increase by the gain of said amplifier A without the unity-gain-bandwidth being adversely affected. The amplifier A need not to have a large bandwidth. As a result of this, the amplifier A can be of simple construction and can be integrated on a small surface area.

In the known amplifier arrangement the input signal V_{in} is applied to the control electrode of the first transistor N1. A drawback of this construction is the rather limited voltage swing of the input signal. Therefore, it is an object of the invention to provide an amplifier arrangement having more input voltage swing. In accordance to the invention the amplifier arrangement is characterized in that the amplifier arrangement further comprises an input transistor having a control electrode coupled to the input terminal, a first main electrode coupled to the second supply-voltage terminal via a bias current source and a second main electrode coupled to the first main electrode of the second transistor, and in that the control electrode of the first transistor is coupled to a further reference-voltage terminal for receiving a further reference voltage.

The control electrode of the first transistor is now coupled to a reference voltage and the input terminal is coupled to the control electrode of the input transistor. The input transistor forms a folded cascode with the second transistor allowing a greater input voltage swing.

A first embodiment of an amplifier arrangement in accordance with the invention may be characterized in that the amplifier comprises a third transistor having a control electrode coupled to the inverting input of the amplifier, a first main electrode coupled to the non-inverting input of the amplifier and a second main electrode coupled both to the output of the amplifier and via a second current source to the second supply-voltage terminal, the first reference-voltage terminal being coupled to the first supply-voltage terminal. The amplifier is constituted by means of the third transistor, as known per se from the above mentioned Japanese patent application.

A second embodiment of an amplifier arrange-

ment in accordance with the invention may be characterized. In that the control electrode of the third transistor is coupled to the inverting input of the amplifier via a level-shifting circuit comprising a fourth transistor having a control electrode coupled to the inverting input of the amplifier, a first main electrode coupled both to the second supply-voltage terminal via a third current source and to the control electrode of the third transistor, and a second main electrode coupled to the first supply-voltage terminal. The level shifting circuit provides a lower potential on the first main electrode of the second transistor as compared with the first embodiment, so that the output voltage swing of the amplifier arrangement can be larger. This is of particular importance in the case of low supply voltages.

A third embodiment of an amplifier arrangement in accordance with the invention may be characterized in that a ladder network ($S_1..S_n$) is arranged between the inverting input of the amplifier and the first main electrode of the second transistor and the second main electrode of the third transistor and the output of the amplifier, the ladder network comprising n cascoded ladder elements, n being equal or greater than 1, each comprising a first ladder transistor and a second ladder transistor, i being a sequence number smaller than or equal to n , each ladder element having four terminals, a first terminal being coupled to the first main electrode of the first ladder transistor, a second terminal being coupled to both the control electrode of the first ladder transistor and to the first main electrode of the second ladder transistor, a third terminal being coupled to the second main electrode of the first ladder transistor and to the control electrode of the second ladder transistor, and a fourth terminal being coupled to the second main electrode of the second ladder transistor, each ladder element having its first terminal and its second terminal coupled respectively to the third terminal and to the fourth terminal of a preceding ladder element, the first terminal and the second terminal of the first ladder element being coupled to the inverting input of the amplifier and the second main electrode of the third transistor respectively, and the third terminal and the fourth terminal of the last ladder element being coupled to the first main electrode of the second transistor and to the output of the amplifier respectively.

The addition of each ladder element leads to an increase in the gain of the amplifier arrangement, so that a very high gain can be attained. This is because every transistor in a ladder element provides an amplification of the voltage on its first main electrode to the voltage on its second main electrode, so that the overall gain increases by the gain factor of said transistor.

A fourth embodiment of an amplifier arrangement in accordance with the invention may be characterized in that a ladder network is arranged between the

second main electrode of the third transistor and the output of the amplifier and the first supply-voltage terminal and the second supply-voltage terminal, the ladder network comprising m cascoded ladder elements, m being equal or greater than 1, each comprising a first ladder transistor and a second ladder transistor and a current source, j being a sequence number smaller than or equal to m , each ladder element having six terminals, a first terminal being coupled to the first main electrode of the first ladder transistor and to the control electrode of the second ladder transistor, a second terminal being coupled to second main electrode of the first ladder transistor, a third terminal being coupled to the first main electrode of the second ladder transistor, a fourth terminal being coupled to the current source, a fifth terminal being coupled to the second main electrode of the first ladder transistor and the sixth terminal being coupled both to the control electrode of the first ladder transistor and to the current source, each ladder element having its first terminal and its second terminal coupled respectively to the fifth terminal and to the sixth terminal of a preceding ladder element, the third terminal and the fourth terminal of a ladder element being coupled to the first supply-voltage terminal and the second supply-voltage terminal respectively, the first terminal and the second terminal of the first ladder element being coupled to the second main electrode of the third transistor and to the output of the amplifier respectively, and the fifth terminal and the sixth terminal of the last ladder element being coupled to one another.

The addition of each ladder element also in this case leads to an increased overall gain, so that again a very high gain can be obtained. Moreover, in order to achieve a constant voltage swing of the output signal, the difference between the first and second supply voltages need not increase when a ladder element is added.

The invention will now be described in more detail, by way of example, with reference to the accompanying drawings, in which

Fig. 1 shows a prior-art amplifier arrangement, Fig. 2 shows a prior-art amplifier subcircuit for use in an amplifier arrangement according to the invention,

Fig. 3 shows a Bode diagram of the subcircuits shown in Fig. 1 and 2,

Fig. 4 shows a subcircuit for use in an amplifier arrangement according to the invention,

Fig. 5 shows a subcircuit for use in an amplifier arrangement according to the invention,

Fig. 6 shows a subcircuit for use in an amplifier arrangement according to the invention,

Fig. 7 shows a subcircuit for use in an amplifier arrangement according to the invention,

Fig. 8 shows a subcircuit for use in an amplifier arrangement according to the invention,

main electrode coupled both to the supply-voltage terminal Vdd by a third current source J3 and to the control electrode of the transistor N3. Since the transistor P1 is of a conductivity type opposite to that of the other transistors the voltage on the inverting input v2 of the amplifier A is at least equal to the threshold voltage of the transistor N3 minus the threshold voltage of the transistor P1. Consequently, the output voltage Vout will have a larger maximum voltage swing than the output voltage Vout in the arrangement shown in Fig. 4, where the voltage on the inverting input v2 of the amplifier A is at least equal to the threshold voltage of the transistor N3.

Fig. 6 shows a third implementation of the amplifier arrangement, in which like parts bear the same reference numerals as in Fig. 4. In this Figure a ladder network is arranged between the inverting input v2 of the amplifier A and the first main electrode of the transistor N2 on the one hand and the second main electrode of the transistor N3 and the output v0 of the amplifier A on the other hand. The ladder network comprises n cascoded ladder elements Si, each comprising two transistors Nia and Nib, where i is a sequence number smaller than or equal to n. Each ladder element Si has four terminals, the first terminal i1 being coupled to the first main electrode of the transistor Nia, the second terminal i2 being coupled both to the control electrode of the transistor Nia and to the first main electrode of the transistor Nib, the third terminal i3 being coupled both to the second main electrode of the transistor Nia and to the control electrode of the transistor Nib, and the fourth terminal i4 being coupled to the second main electrode of the transistor Nib. Each ladder element Si has its first terminal i1 and its second terminal i2 coupled respectively to the third terminal i3 and to the fourth terminal i4 of a preceding ladder element Si-1, the first and the second terminal i1 and i2 of the first ladder element S1 being coupled to the inverting input v2 of the amplifier A and the second main electrode of the transistor N3 respectively, and the third and the fourth terminal i3 and i4 of the last ladder element Sn being coupled to the first main electrode of the transistor N2 and the output v0 of the amplifier A respectively. The function of each ladder element Si is to increase the gain of the entire circuit arrangement. To this end each transistor amplifies the voltage on its first main electrode to the voltage on its second main electrode and thus augments the overall gain by its gain factor. Moreover, negative feedback is provided of the potential on the first main electrode of each transistor to its control electrode. For the transistor N1a this is achieved by means of the transistor N3, for the transistor N1b by the transistor N1 etc. When this ladder network is used the difference between the two supply voltages Vdd and Vss should be adequate for the number of ladder elements used.

Fig. 7 shows a fourth implementation of the am-

plifier arrangement for use in accordance with the invention, in which like parts bear the same reference numerals as in Fig. 4. The arrangement also comprises a ladder network in order to increase the gain. The ladder network is coupled between the second main electrode of the transistor N3 and the output v0 of the amplifier on the one hand and the two supply-voltage terminals Vss and Vdd on the other hand. The ladder network comprises m cascoded ladder elements PJ, which each comprise two transistors Njc and Njd and a current source Jj+5, j being a sequence number larger than n and smaller than or equal to n+m. Each ladder element PJ comprises six terminals, the first terminal j1 being coupled to the first main electrode of the transistor Njc and to the control electrode of the transistor Njd, the second terminal j2 being coupled to the second main electrode of the transistor Njc, the third terminal j3 being coupled to the first main electrode of the transistor Njd, the fourth terminal j4 being coupled to the current source Jj+5, the fifth terminal j5 being coupled to the second main electrode of the transistor Njc, and the sixth terminal j6 being coupled both to the control electrode of the transistor Njc and to the current source Jj+5. Each ladder element PJ has its first terminal j1 and its second terminal j2 coupled respectively to the fifth terminal j5 and the sixth terminal j6 of a preceding ladder element PJ-1, the third terminal j3 and the fourth terminal j4 of a ladder element PJ being coupled to the supply-voltage terminals Vss and Vdd respectively, the first terminal j1 and the second terminal j2 of the first ladder element Pn+1 being coupled to the second main electrode of the transistor N3 and the output v0 of the amplifier A respectively, and the fifth terminal j5 and the sixth terminal j6 of the last ladder element Pm being coupled to one another. An advantage of this construction of the ladder network is that the supply-voltage difference need not increase as the number of network elements Sj increases. Each additional ladder element Sj provides both cascoding of a transistor in the cascade circuit and negative feedback of the potential on the first main electrode of the transistor Njc by means of a transistor Njd. This results in an increased gain of the arrangement and it enables any desired value to be obtained by changing the number of ladder elements.

Fig. 8 shows a fifth implementation of the amplifier arrangement used in accordance with the invention, in which like parts bear the same reference numerals as in Fig. 2. In this arrangement the amplifier A is formed by means of a folded cascode circuit, employing a third, a fourth, a fifth and a sixth transistor P2, P3, N4 and N5, a second current source J4 and a third current source J5, a second reference voltage terminal 4 and a third reference voltage terminal 5 for applying the reference voltages Vref2 and Vref3 respectively. The transistor P2 is coupled to the inverting input v2 of the amplifier A via its control electrode

and to the second supply-voltage terminal Vdd by means of the current source J4 via its first main electrode. The transistor P3 has its control electrode coupled both to the non-inverting input v1 of the amplifier A and to the reference-voltage terminal 2 for the reference voltage Vref1, has its first main electrode coupled to the first main electrode of the third transistor P2, and has its second main electrode coupled to the first supply-voltage terminal Vss. The transistor N4 is coupled to the reference-voltage terminal 4 for the reference voltage Vref2 via its control electrode and to the first supply-voltage terminal Vss via its first main electrode. The transistor N5 is coupled to the reference voltage terminal 5 for the reference voltage Vref3 via its control electrode, to the second main electrodes of both the transistor P2 and the transistor N4 via its first main electrode, and to the second supply-voltage terminal Vdd by the current source J5 and to the output v0 of the amplifier A via its second main electrode. The transistors P2 and P3 are both of a conductivity type opposite to that of the other transistors and together constitute a differential pair. Consequently, the signal on the inverting input V2 of the amplifier A is amplified to the second main electrode of the transistor N4, after which the transistor N4 again amplifies the signal to the output v0 of the amplifier A. This arrangement also has the advantage that the output voltage swing can be comparatively large because in the balanced state the voltage on the inverting input V2 of the amplifier A is dictated by the reference voltage Vref1.

Fig. 9 shows a sixth implementation of the amplifier arrangement for use accordance with the invention, in which like parts bear the same reference numerals as in Fig. 8. In this embodiment, however, the transistor P3 and the current source J4 are replaced by a transistor N6, which has its control electrode coupled both to the non-inverting output v1 of the amplifier A and to the reference-voltage terminal 2 for the reference voltage Vref1, which has its first main electrode coupled to the first main electrode of the transistor P2, and which has its second main electrode coupled to the second supply-voltage terminal Vdd. This modification of the circuit arrangement as shown in Fig. 8 has the advantage that the current which was drained via the transistor P3 is saved. In the balanced state the voltage on the inverting input v2 of the amplifier A is equal to the reference voltage Vref1 minus at least the threshold voltage of both the transistor N6 and the transistor P2, so that again a maximum voltage swing on the output 3 is attainable.

Fig. 10 shows a seventh implementation of the amplifier arrangement for use in accordance with the invention, in which like parts bear the same reference numerals as in Fig. 5. Both the transistor P1 and the transistor N3 in this arrangement are cascoded by means of the transistor P4 and the transistor N7 respectively. Thus, the transistor P4 is arranged be-

tween the first main electrode of the transistor P1 and the current source J3, which transistor P4 has its control electrode coupled to the inverting input v2 of the amplifier A, its first main electrode to the current source J3, and its second main electrode to the transistor P1. Moreover, the transistor N7 is arranged between the second main electrode of the transistor N3 and the output v0 of the amplifier A and has its control electrode coupled to the first main electrode of the transistor P4, its first main electrode to the second main electrode of the transistor N3 and its second main electrode to the current source J2. This arrangement also enables a comparatively large output voltage swing to be obtained. Cascoding in this way results in an increase in the overall gain, as compared with the arrangement shown in Fig. 5, by the gain factor of the transistor N7. The transistors P1 and P4 are of a conductivity type opposite to that of the other transistors and operate as source followers.

Fig. 11 shows an operational amplifier in accordance with the invention comprising amplifier arrangements as shown in Fig. 2. The operational amplifier comprises a symmetrical input stage I and two mutually similar output stages EF and GH. The input stage I comprises two transistors N8 and N9 arranged as a differential pair and having their mutually coupled first main electrodes coupled both to the supply voltage terminal Vss by a current source J6 and to the supply voltage terminal Vdd by two transistors N10 and N11 which are arranged completely in parallel. The first main electrodes of the transistors N10 and N11 are connected to the corresponding electrodes of the transistors N8 and N9, a reference voltage Vref4 being applied to the control electrodes of the transistors N10 and N11. The control electrodes of the transistors N8 and N9 are coupled to a terminal 1EF and a terminal 1GH respectively, the terminal 1EF being arranged to receive an input signal VinEF and the terminal 1GH being arranged to receive an input signal VinGH. The input stage I drives the output stages EF and GH via the second main electrodes of the transistors N8 and N9, which output stages each comprise an amplifier section, EE and GG respectively, and a current-source section, FF and HH respectively. The amplifier section EE comprises a transistor P1E, having its control electrode coupled to a terminal 1E arranged to receive a reference voltage VrefE, having its first main electrode coupled to the supply voltage terminal Vdd, and having its second main electrode coupled to an inverting input of an amplifier E, to a first main electrode of a transistor P2E, and to the second main electrode of the transistor N8. The second main electrode of the transistor P2E is coupled to an output terminal 3EF arranged to supply an output signal VoutEF and the control electrode of the transistor P2E is coupled to an output of the amplifier E, which has its non-inverting input coupled to a terminal 2E arranged to receive a reference

voltage V_{ref1E} . The current-source section FF comprises a transistor N1F having its control electrode coupled to a terminal 1F arranged to receive a reference voltage V_{refF} , having its first main electrode coupled to the supply voltage terminal V_{ss} , and having its second main electrode coupled to an inverting input of an amplifier F and to a first main electrode of a transistor N2F. The second main electrode of the transistor N2F is coupled to the output terminal 3EF and the control electrode of the transistor N2F is coupled to an output of the amplifier F, which has its non-inverting input coupled to a terminal 2F arranged to receive a reference voltage V_{ref1F} . The amplifier section GG comprises a transistor P1G having its control electrode coupled to a terminal 1G arranged to receive a reference voltage V_{refG} , having its first main electrode coupled to the supply voltage terminal V_{dd} , and having its second main electrode coupled to an inverting input of an amplifier G, to a first main electrode of a transistor P2G and to the second main electrode of the transistor N9. The second main electrode of the transistor P2G is coupled to an output terminal 3GH arranged to supply an output signal V_{outGH} , and the control electrode of the transistor P2G is coupled to an output of the amplifier G, which has its non-inverting input coupled to a terminal 2G arranged to receive a reference voltage V_{ref1G} . The current-source-section HH comprises a transistor N1H having its control electrode coupled to a terminal 1H arranged to receive a reference voltage V_{refH} , having its first main electrode coupled to the supply voltage terminal V_{ss} , and having its second main electrode coupled to an inverting input of an amplifier H and to a first main electrode of a transistor N2H. The second main electrode of the transistor N2H is coupled to the output terminal 3GH and the control electrode of the transistor N2H is coupled to an output of the amplifier H, which has its non-inverting input coupled to a terminal 2H arranged to receive a reference voltage V_{ref1H} .

In the operational amplifier of this construction both the transistors N8 and P2E and the transistors N9 and P2G each constitute a folded cascode pair, the transistors N10 and N11 dictating the voltages on the input terminals 1EF and 1GH depending on the reference voltage V_{ref4} and the current of the current source J6. As a result of the use of said folded cascode pairs the relevant voltages can be controlled in such a manner that the input signals V_{inEF} and V_{inGH} can each assume a maximum amplitude dictated by the supply voltages. An alternative to the illustrated method of driving the two output stages EF and GH, in which the input stage I is dispensed with, is to apply the respective input signals V_{inEF} and V_{inGH} either to the terminals 1E and 1G or to the terminals 1F and 1H. However, the last-mentioned driving method means that the functions of the output-stage sections EE and FF and those of the output-stage sections GG and HH are interchanged.

The operational amplifier shown herein thus comprises two output stages operating similarly to the amplifier arrangement shown in Fig. 2 but in which the input signals V_{inEF} and V_{inGH} are each applied via a folded cascode pair, the transistors P1E and P1G merely being co-decisive for the bias currents in the amplifier. The amplifier sections EE, EF, GS and HH can each be implemented in various ways, for example like one of the amplifier arrangements in the preceding Figures. In case of sections EE and SS the supply voltages and the conductivity type of the transistors shown in the preceding figures should be reversed. In all cases the terminal 1 shown in the preceding figures must be connected to a reference voltage. For an optimum operation of the amplifier arrangements shown in all the Figures the current sources coupled to the relevant output terminals should have a high impedance in order to obtain a high output impedance and a high gain. The current source sections FF and HH shown in Fig. 11 are exemplary of such current sources.

Claims

1. An amplifier arrangement for amplifying an input signal, the arrangement comprising an input terminal (1EF;1) for receiving the input signal, a first transistor (P1E;N1) having a control electrode, a first main electrode coupled to a first supply-voltage terminal (V_{dd}), and a second main electrode, a second transistor (P2E;N2) having a control electrode, a first main electrode coupled to the second main electrode of the first transistor (P1E;N1), and a second main electrode coupled both to a second supply-voltage terminal (V_{ss}) via a first current source (FF;J1) and to an output terminal (3EF;3) for supplying an output signal, the control electrode of the second transistor (P2E;N2) being coupled to an output (V0) of an amplifier (E;A), the second main electrode of the first transistor (P1E;N1) being coupled to an inverting input (-;V2) of the amplifier (E;A), and a non-inverting input (+;V1) of the amplifier (E;A) being coupled to a first reference-voltage terminal (2E;2) for receiving a first reference voltage, characterized in that the amplifier arrangement further comprises an input transistor (N8) having a control electrode coupled to the input terminal (1EF), a first main electrode coupled to the second supply-voltage terminal (V_{ss}) via a bias current source (J6) and a second main electrode coupled to the first main electrode of the second transistor (P2E), and in that the control electrode of the first transistor (P1E) is coupled to a further reference-voltage terminal (1E) for receiving a further reference voltage.

voltage Vref1E. The current-source section FF comprises a transistor N1F having its control electrode coupled to a terminal 1F arranged to receive a reference voltage VrefF, having its first main electrode coupled to the supply voltage terminal Vss, and having its second main electrode coupled to an inverting input of an amplifier F and to a first main electrode of a transistor N2F. The second main electrode of the transistor N2F is coupled to the output terminal 3EF and the control electrode of the transistor N2F is coupled to an output of the amplifier F, which has its non-inverting input coupled to a terminal 2F arranged to receive a reference voltage Vref1F. The amplifier section GG comprises a transistor P1G having its control electrode coupled to a terminal 1G arranged to receive a reference voltage VrefG, having its first main electrode coupled to the supply voltage terminal Vdd, and having its second main electrode coupled to an inverting input of an amplifier G, to a first main electrode of a transistor P2G and to the second main electrode of the transistor N9. The second main electrode of the transistor P2G is coupled to an output terminal 3GH arranged to supply an output signal VoutGH, and the control electrode of the transistor P2G is coupled to an output of the amplifier G, which has its non-inverting input coupled to a terminal 2G arranged to receive a reference voltage Vref1G. The current-source-section HH comprises a transistor N1H having its control electrode coupled to a terminal 1H arranged to receive a reference voltage VrefH, having its first main electrode coupled to the supply voltage terminal Vss, and having its second main electrode coupled to an inverting input of an amplifier H and to a first main electrode of a transistor N2H. The second main electrode of the transistor N2H is coupled to the output terminal 3GH and the control electrode of the transistor N2H is coupled to an output of the amplifier H, which has its non-inverting input coupled to a terminal 2H arranged to receive a reference voltage Vref1H.

In the operational amplifier of this construction both the transistors N8 and P2E and the transistors N9 and P2G each constitute a folded cascode pair, the transistors N10 and N11 dictating the voltages on the input terminals 1EF and 1GH depending on the reference voltage Vref4 and the current of the current source J6. As a result of the use of said folded cascode pairs the relevant voltages can be controlled in such a manner that the input signals VinEF and VinGH can each assume a maximum amplitude dictated by the supply voltages. An alternative to the illustrated method of driving the two output stages EF and GH, in which the input stage I is dispensed with, is to apply the respective input signals VinEF and VinGH either to the terminals 1E and 1G or to the terminals 1F and 1H. However, the last-mentioned driving method means that the functions of the output-stage sections EE and FF and those of the output-stage sections GG and HH are interchanged.

The operational amplifier shown herein thus comprises two output stages operating similarly to the amplifier arrangement shown in Fig. 2 but in which the input signals VinEF and VinGH are each applied via a folded cascode pair, the transistors P1E and P1G merely being co-decisive for the bias currents in the amplifier. The amplifier sections EE, EF, GS and HH can each be implemented in various ways, for example like one of the amplifier arrangements in the preceding Figures. In case of sections EE and SS the supply voltages and the conductivity type of the transistors shown in the preceding figures should be reversed. In all cases the terminal 1 shown in the preceding figures must be connected to a reference voltage. For an optimum operation of the amplifier arrangements shown in all the Figures the current sources coupled to the relevant output terminals should have a high impedance in order to obtain a high output impedance and a high gain. The current source sections FF and HH shown in Fig. 11 are exemplary of such current sources.

Claims

1. An amplifier arrangement for amplifying an input signal, the arrangement comprising an input terminal (1EF;1) for receiving the input signal, a first transistor (P1E;N1) having a control electrode, a first main electrode coupled to a first supply-voltage terminal (V_{dd}), and a second main electrode, a second transistor (P2E;N2) having a control electrode, a first main electrode coupled to the second main electrode of the first transistor (P1E;N1), and a second main electrode coupled both to a second supply-voltage terminal (V_{ss}) via a first current source (FF;J1) and to an output terminal (3EF;3) for supplying an output signal, the control electrode of the second transistor (P2E;N2) being coupled to an output (;V0) of an amplifier (E;A), the second main electrode of the first transistor (P1E;N1) being coupled to an inverting input (- ;V2) of the amplifier (E;A), and a non-inverting input (+;V1) of the amplifier (E;A) being coupled to a first reference-voltage terminal (2E;2) for receiving a first reference voltage, characterized in that the amplifier arrangement further comprises an input transistor (N8) having a control electrode coupled to the input terminal (1EF), a first main electrode coupled to the second supply-voltage terminal (V_{ss}) via a bias current source (J6) and a second main electrode coupled to the first main electrode of the second transistor (P2E), and in that the control electrode of the first transistor (P1E) is coupled to a further reference-voltage terminal (1E) for receiving a further reference voltage.



2. An amplifier arrangement as claimed in Claim 1, characterized in that the amplifier (E;A) comprises a third transistor (N3) having a control electrode coupled to the inverting input (V2) of the amplifier (A), a first main electrode coupled to the non-inverting input (V1) of the amplifier (A) and a second main electrode coupled both to the output (V0) of the amplifier (A) and via a second current source (J2) to the second supply-voltage terminal (V_{ss}), the first reference-voltage terminal (2) being coupled to the first supply-voltage terminal (V_{dd}).
3. An amplifier arrangement as claimed in Claim 2, characterized in that the control electrode of the third transistor (N3) is coupled to the inverting input (V2) of the amplifier (A) via a level-shifting circuit comprising a fourth transistor (P1) having a control electrode coupled to the inverting input (V2) of the amplifier (A), a first main electrode coupled both to the second supply-voltage terminal (V_{ss}) via a third current source (J3) and to the control electrode of the third transistor (N3), and a second main electrode coupled to the first supply-voltage terminal (V_{dd}).
4. An amplifier arrangement as claimed in Claim 2, characterized in that a ladder network (S1..Sn) is arranged between the inverting input (V2) of the amplifier (A) and the first main electrode of the second transistor (N2) and the second main electrode of the third transistor (N3) and the output (V0) of the amplifier (A), the ladder network comprising n cascoded ladder elements (S1, Si, Sn), n being equal or greater than 1, each comprising a first ladder transistor (Nia) and a second ladder transistor (Nib), i being a sequence number smaller than or equal to n, each ladder element (Si) having four terminals, a first terminal (i1) being coupled to the first main electrode of the first ladder transistor (Nia), a second terminal (i2) being coupled to both the control electrode of the first ladder transistor (Nia) and to the first main electrode of the second ladder transistor (Nib), a third terminal (i3) being coupled to the second main electrode of the first ladder transistor (Nia) and to the control electrode of the second ladder transistor (Nib), and a fourth terminal (i4) being coupled to the second main electrode of the second ladder transistor (Nib), each ladder element (Si) having its first terminal (i1) and its second terminal (i2) coupled respectively to the third terminal (i3) and to the fourth terminal (i4) of a preceding ladder element (Si-1), the first terminal (i1) and the second terminal (i2) of the first ladder element (S1) being coupled to the inverting input (V2) of the amplifier (A) and the second main electrode of the third transistor (N3) respectively, and the third terminal (n3) and the fourth terminal (n4) of the last ladder element (Sn) being coupled to the first main electrode of the second transistor (N2) and to the output (V0) of the amplifier (A) respectively.
5. An amplifier arrangement as claimed in Claim 2, characterized in that a ladder network (P1..Pn) is arranged between the second main electrode of the third transistor (N3) and the output (V0) of the amplifier (A) and the first supply-voltage terminal (V_{dd}) and the second supply-voltage terminal (V_{ss}), the ladder network comprising m cascoded ladder elements (P1, Pj, Pm), m being equal or greater than 1, each comprising a first ladder transistor (Njc) and a second ladder transistor (Njd) and a current source (Jj+5), j being a sequence number smaller than or equal to m, each ladder element (Pj) having six terminals, a first terminal (j1) being coupled to the first main electrode of the first ladder transistor (Njc) and to the control electrode of the second ladder transistor (Njd), a second terminal (j2) being coupled to second main electrode of the first ladder transistor (Njc), a third terminal (j3) being coupled to the first main electrode of the second ladder transistor (Njd), a fourth terminal (j4) being coupled to the current source (Jj+5), a fifth terminal (j5) being coupled to the second main electrode of the first ladder transistor (Njc) and the sixth terminal (j6) being coupled both to the control electrode of the first ladder transistor (Njc) and to the current source (Jj+5), each ladder element (Pj) having its first terminal (j1) and its second terminal (j2) coupled respectively to the fifth terminal (j5) and to the sixth terminal (j6) of a preceding ladder element (Pj-1), the third terminal (j3) and the fourth terminal (j4) of a ladder element (Pj) being coupled to the first supply-voltage terminal (V_{ss}) and the second supply-voltage terminal (V_{dd}) respectively, the first terminal (j1) and the second terminal (j2) of the first ladder element (P1) being coupled to the second main electrode of the third transistor (N3) and to the output (V0) of the amplifier (A) respectively, and the fifth terminal (j5) and the sixth terminal (j6) of the last ladder element (Pm) being coupled to one another.
6. An amplifier arrangement as claimed in Claim 1, characterized in that the amplifier (A) comprises a third transistor (P2) having a first main electrode, a second main electrode and a control electrode, which is coupled to the inverting input (V2) of the amplifier (A), a fourth transistor (P3;N6) having a control electrode coupled to the non-inverting input (V1) of the amplifier (A), a first main electrode coupled to the first main electrode of the third transistor (P2), and a second



main electrode, a fifth transistor (N4) having a control electrode coupled to a second reference-voltage terminal (4) for receiving a second reference voltage, a first main electrode coupled to the first supply-voltage terminal (V_{dd}), and a second main electrode, and a sixth transistor (N5) having a control electrode coupled to a third reference-voltage terminal (5) for receiving a third reference voltage, a first main electrode coupled to the second main electrode of both the third transistor (P2) and the fifth transistor (N4) and a second main electrode coupled both to the second supply-voltage terminal (V_{ss}) via a second current source (J5) and to the output (V0) of the amplifier (A).

7. An amplifier arrangement as claimed in Claim 6, characterized in that the first main electrode of the fourth transistor (P3) is coupled to the second supply-voltage terminal (V_{dd}) via a third current source (J4) and the second main electrode of the fourth transistor (P3) is coupled to the first supply-voltage terminal (V_{dd}).
8. An amplifier arrangement as claimed in Claim 6, characterized in that the second main electrode of the fourth transistor (N6) is coupled to the second supply-voltage terminal (V_{ss}).
9. An amplifier arrangement as claimed in any one of the preceding Claims, characterized in that the amplifier arrangement further comprises a reference transistor (N10) having a first main electrode coupled to the first main electrode of the input transistor (N8), a second main electrode coupled to the first supply-voltage terminal (V_{dd}) and a control electrode coupled to a second further reference-voltage terminal (V_{ref4}).

Patentansprüche

1. Verstärkeranordnung zum Verstärken eines Eingangssignals, wobei die Anordnung eine Eingangsklemme (1EF;1) zum Empfangen des Eingangssignals umfaßt, sowie einen ersten Transistor (P1E;N1) mit einer Steuerelektrode, einer ersten Hauptelektrode, die mit einer ersten Speisespannungsklemme (V_{dd}) gekoppelt ist, und einer zweiten Hauptelektrode, einen zweiten Transistor (P2E;N2) mit einer Steuerelektrode, einer ersten Hauptelektrode, die mit der zweiten Hauptelektrode des ersten Transistors (P1E;N1) gekoppelt ist, und einer zweiten Hauptelektrode, die sowohl mit einer zweiten Speisespannungsklemme (V_{ss}) mittels einer ersten Stromquelle (FF;J1) als auch mit einer Ausgangsklemme (3EF;3) zum Liefern eines Ausgangssignals verbunden ist,

wobei die Steuerelektrode des zweiten Transistors (P2E;N2) mit einem Ausgang (V0) eines Verstärkers (E; A) gekoppelt ist, die zweite Hauptelektrode des ersten Transistors (P1E;N1) mit einem invertierenden Eingang (-; V2) des Verstärkers (E; A) gekoppelt ist, und ein nichtinvertierender Eingang (+; V1) des Verstärkers (E; A) mit einer ersten Bezugsspannungsklemme (2E; 2) zum Empfangen einer ersten Bezugsspannung gekoppelt ist, dadurch gekennzeichnet, daß die Verstärkeranordnung weiterhin einen Eingangstransistor (N8) enthält, der eine Steuerelektrode hat, die mit der Eingangsklemme (1EF) gekoppelt ist, eine erste Hauptelektrode, die mittels einer Ruhestromquelle (J6) mit der zweiten Speisespannungsklemme (V_{ss}) gekoppelt ist, und eine zweite Hauptelektrode, die mit der ersten Hauptelektrode des zweiten Transistors (P2E) gekoppelt ist, und daß die Steuerelektrode des ersten Transistors (P1E) mit einer weiteren Bezugsspannungsklemme (1E) zum Empfangen einer weiteren Bezugsspannung gekoppelt ist.

2. Verstärkeranordnung nach Anspruch 1, dadurch gekennzeichnet, daß der Verstärker (E; A) einen dritten Transistor (N3) umfaßt, der eine Steuerelektrode hat, die mit dem invertierenden Eingang (V2) des Verstärkers (A) gekoppelt ist, eine erste Hauptelektrode, die mit dem nichtinvertierenden Eingang (V1) des Verstärkers (A) gekoppelt ist, und eine zweite Hauptelektrode, die sowohl mit dem Ausgang (V0) des Verstärkers (A) als auch mittels einer zweiten Stromquelle (J2) mit der zweiten Speisespannungsklemme (V_{ss}) gekoppelt ist, wobei die erste Bezugsspannungsklemme (2) mit der ersten Speisespannungsklemme (V_{dd}) gekoppelt ist.
3. Verstärkeranordnung nach Anspruch 2, dadurch gekennzeichnet, daß die Steuerelektrode des dritten Transistors (N3) mit dem invertierenden Eingang (V2) des Verstärkers (A) mittels einer Pegelverschiebeschaltung gekoppelt ist, die einen vierten Transistor (P1) umfaßt, der eine Steuerelektrode hat, die mit dem invertierenden Eingang (V2) des Verstärkers (A) gekoppelt ist, eine erste Hauptelektrode, die sowohl mit der zweiten Speisespannungsklemme (V_{ss}) mittels einer dritten Stromquelle (J3) als auch mit der Steuerelektrode des dritten Transistors (N3) gekoppelt ist, und eine zweite Hauptelektrode, die mit der ersten Speisespannungsklemme (V_{dd}) gekoppelt ist.
4. Verstärkeranordnung nach Anspruch 2, dadurch gekennzeichnet, daß ein Kettenleiternetz ($S1...Sn$) zwischen dem invertierenden Eingang (V2) des Verstärkers (A) und der ersten Haupt-



elektrode des zweiten Transistors (N2) und der zweiten Hauptelektrode des dritten Transistors (N3) und dem Ausgang (V0) des Verstärkers (A) angeordnet ist, wobei das Kettenleiternetz n kaskodengeschaltete Kettenleiter Elemente (S1, Si, Sn) umfaßt, mit n gleich oder größer als 1, wobei jedes einen ersten Kettenleitertransistor (Nia) und einen zweiten Kettenleitertransistor (Nib) umfaßt, mit i eine Folgenummer kleiner oder gleich n, wobei jedes Kettenleiter Element (Si) vier Anschlußklemmen hat, eine erste Anschlußklemme (I1) mit der ersten Hauptelektrode des ersten Kettenleitertransistors (Nia) gekoppelt ist, eine zweite Anschlußklemme (I2) mit sowohl der Steuerelektrode des ersten Kettenleitertransistors (Nia) als auch der ersten Hauptelektrode des zweiten Kettenleitertransistors (Nib) gekoppelt ist, eine dritte Anschlußklemme (I3) mit der zweiten Hauptelektrode des ersten Kettenleitertransistors (Nia) und der Steuerelektrode des zweiten Kettenleitertransistors (Nib) gekoppelt ist und eine vierte Anschlußklemme (I4) mit der zweiten Hauptelektrode des zweiten Kettenleitertransistors (Nib) gekoppelt ist, wobei die erste Anschlußklemme (I1) und die zweite Anschlußklemme (I2) eines jeden Kettenleiter Elements (Si) mit der dritten Anschlußklemme (I3) bzw. der vierten Anschlußklemme (I4) eines vorhergehenden Kettenleiter Elements (Si-1) gekoppelt sind, die erste Anschlußklemme (I1) und die zweite Anschlußklemme (I2) des ersten Kettenleiter Elements (S1) mit dem invertierenden Eingang (V2) des Verstärkers (A) bzw. der zweiten Hauptelektrode des dritten Transistors (N3) gekoppelt sind und die dritte Anschlußklemme (I3) und die vierte Anschlußklemme (I4) des letzten Kettenleiter Elements (Sn) mit der ersten Hauptelektrode des zweiten Transistors (N2) bzw. dem Ausgang (V0) des Verstärkers (A) gekoppelt sind.

5. Verstärkeranordnung nach Anspruch 2, dadurch gekennzeichnet, daß ein Kettenleiternetz (P1...Pn) zwischen der zweiten Hauptelektrode des dritten Transistors (N3) und dem Ausgang (V0) des Verstärkers (A) und der ersten Speisespannungsklemme (V_{dd}) und der zweiten Speisespannungsklemme (V_{ss}) angeordnet ist, wobei das Kettenleiternetz m kaskodengeschaltete Kettenleiter Elemente (P1, Pj, Pm) umfaßt, mit m gleich oder größer als 1, wobei jedes einen ersten Kettenleitertransistor (Njc) und einen zweiten Kettenleitertransistor (Njd) und eine Stromquelle (Jj+5) umfaßt, mit j eine Folgenummer kleiner oder gleich m, wobei jedes Kettenleiter Element (Pj) sechs Anschlußklemmen hat, eine erste Anschlußklemme (J1) mit der ersten Hauptelektrode des ersten Kettenleitertransistors (Njc) und der Steuerelektrode des zweiten Kettenleitertransi-

stors (Njd) gekoppelt ist, eine zweite Anschlußklemme (J2) mit der zweiten Hauptelektrode des ersten Kettenleitertransistors (Njc) gekoppelt ist, eine dritte Anschlußklemme (J3) mit der ersten Hauptelektrode des zweiten Kettenleitertransistors (Njd) gekoppelt ist, eine vierte Anschlußklemme (J4) mit der Stromquelle (Jj+5) gekoppelt ist, eine fünfte Anschlußklemme (J5) mit der zweiten Hauptelektrode des ersten Kettenleitertransistors (Njc) gekoppelt ist und die sechste Anschlußklemme (J6) sowohl mit der Steuerelektrode des ersten Kettenleitertransistors (Njc) als auch der Stromquelle (Jj+5) gekoppelt ist, wobei die erste Anschlußklemme (J1) und die zweite Anschlußklemme (J2) eines jeden Kettenleiter Elements (Pj) mit der fünften Anschlußklemme (J5) bzw. der sechsten Anschlußklemme (J6) eines vorhergehenden Kettenleiter Elements (Pj-1) gekoppelt sind, die dritte Anschlußklemme (J3) und die vierte Anschlußklemme (J4) eines Kettenleiter Elements (Pj) mit der ersten Speisespannungsklemme (V_{dd}) bzw. der zweiten Speisespannungsklemme (V_{ss}) gekoppelt sind, die erste Anschlußklemme (J1) und die zweite Anschlußklemme (J2) des ersten Kettenleiter Elements (P1) mit der zweiten Hauptelektrode des dritten Transistors (N3) bzw. dem Ausgang (V0) des Verstärkers (A) gekoppelt sind und die fünfte Anschlußklemme (J5) und die sechste Anschlußklemme (J6) des letzten Kettenleiter Elements (Pm) miteinander gekoppelt sind.

6. Verstärkeranordnung nach Anspruch 1, dadurch gekennzeichnet, daß der Verstärker (A) einen dritten Transistor (P2) mit einer ersten Hauptelektrode, einer zweiten Hauptelektrode und einer mit dem invertierenden Eingang (V2) des Verstärkers (A) gekoppelten Steuerelektrode umfaßt und einen vierten Transistor (P3; N6) mit einer mit dem nichtinvertierenden Eingang (V1) des Verstärkers (A) gekoppelten Steuerelektrode, mit einer ersten Hauptelektrode, die mit der ersten Hauptelektrode des dritten Transistors (P2) gekoppelt ist, und mit einer zweiten Hauptelektrode, sowie einen fünften Transistor (N4) mit einer mit einer zweiten Bezugsspannungsklemme (4) zum Empfangen einer zweiten Bezugsspannung gekoppelten Steuerelektrode, mit einer ersten Hauptelektrode, die mit der ersten Speisespannungsklemme (V_{dd}) gekoppelt ist, und mit einer zweiten Hauptelektrode, und einen sechsten Transistor (N5) mit einer mit einer dritten Bezugsspannungsklemme (5) zum Empfangen einer dritten Bezugsspannung gekoppelten Steuerelektrode, mit einer ersten Hauptelektrode, die mit der zweiten Hauptelektrode sowohl des dritten Transistors (P2) als auch des fünften Transistors (N4) gekoppelt ist, und mit einer zweiten



Hauptelektrode, die sowohl mit der zweiten Speisespannungsklemme (V_{ss}) mittels einer zweiten Stromquelle als auch mit dem Ausgang (V0) des Verstärkers (A) gekoppelt ist.

7. Verstärkeranordnung nach Anspruch 6, dadurch gekennzeichnet, daß die erste Hauptelektrode des vierten Transistors (P3) mittels einer dritten Stromquelle (J4) mit der zweiten Speisespannungsklemme (V_{ss}) und die zweite Hauptelektrode des vierten Transistors (P3) mit der ersten Speisespannungsklemme (V_{dd}) gekoppelt ist.
8. Verstärkeranordnung nach Anspruch 6, dadurch gekennzeichnet, daß die zweite Hauptelektrode des vierten Transistors (N6) mit der zweiten Speisespannungsklemme (V_{ss}) gekoppelt ist.
9. Verstärkeranordnung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die Verstärkeranordnung weiterhin einen Bezugstransistor (N10) umfaßt, der eine erste Hauptelektrode hat, die mit der ersten Hauptelektrode des Eingangstransistors (N8) gekoppelt ist, eine zweite Hauptelektrode, die mit der ersten Speisespannungsklemme (V_{ss}) gekoppelt ist, und eine Steuerelektrode, die mit einer zweiten weiteren Bezugsspannungsklemme (V_{ref4}) gekoppelt ist.

Revendications

1. Circuit amplificateur pour amplifier un signal d'entrée, comprenant une borne d'entrée (1EF; 1) pour la réception du signal d'entrée, un premier transistor (P1E; N1) présentant une électrode de commande, une première électrode principale couplée à une première borne de tension d'alimentation (V_{dd}), et une deuxième électrode principale, un deuxième transistor (P2E; N2) présentant une électrode de commande, une première électrode principale couplée à la deuxième électrode principale du premier transistor (P1E; N1) et une deuxième électrode principale couplée à une deuxième borne de tension d'alimentation (V_{ss}) par l'intermédiaire d'une première source de courant (FF; J1) et à une borne de sortie (3EF; 3) pour fournir un signal de sortie, l'électrode de commande du deuxième transistor (P2E; N2) étant couplée à une sortie (-; V0) d'un amplificateur (E; A) la deuxième électrode principale du premier transistor (P1E; N1) étant couplée à une entrée inverseuse (-; V2) de l'amplificateur (E; A) et une entrée non inverseuse (+; V1) de l'amplificateur (E; A) étant couplée à une première borne de tension de référence (2E; 2) pour la réception d'une première tension de référence,

caractérisé en ce que le circuit amplificateur comprend en outre un transistor d'entrée (N8) présentant une électrode de commande couplée à la borne d'entrée (1EF), une première électrode principale couplée à la deuxième borne de tension d'alimentation (V_{ss}) par l'intermédiaire d'une source de courant de polarisation (J6) et une deuxième électrode principale couplée à la première électrode principale du deuxième transistor (P2E) et en ce que l'électrode de commande du premier transistor (P1E) est couplée à une autre borne de tension de référence (1E) pour la réception d'une autre tension de référence.

2. Circuit amplificateur selon la revendication 1, caractérisé en ce que l'amplificateur (E; A) comprend un troisième transistor (N3) présentant une électrode de commande couplée à l'entrée inverseuse (V2) de l'amplificateur (A), une première électrode principale couplée à l'entrée non inverseuse (V1) de l'amplificateur (A) et une deuxième électrode principale couplée à la sortie (V0) de l'amplificateur (A) et par l'intermédiaire d'une deuxième source de courant (J2) à la deuxième borne de tension d'alimentation (V_{ss}), la première borne de tension de référence (2) étant couplée à la première borne de tension d'alimentation (V_{dd}).
3. Circuit amplificateur selon la revendication 2, caractérisé en ce que l'électrode de commande du troisième transistor (N3) est couplée à une entrée inverseuse (V2) de l'amplificateur (A) par l'intermédiaire d'un circuit de décalage de niveau comprenant un quatrième transistor (P1) présentant une électrode de commande couplée à l'entrée inverseuse (V2) de l'amplificateur (A), une première électrode principale couplée à la deuxième borne de tension d'alimentation (V_{ss}) par l'intermédiaire d'une troisième source de courant (J3) et à l'électrode de commande du troisième transistor (N3) et une deuxième électrode principale couplée à la première borne de tension d'alimentation (V_{dd}).
4. Circuit amplificateur selon la revendication 2, caractérisé en ce qu'un réseau en échelle ($S1...Sn$) est disposé entre l'entrée inverseuse (V2) de l'amplificateur (A) et la première électrode principale du deuxième transistor (N2) et la deuxième électrode principale du troisième transistor (N3) et la sortie (V0) de l'amplificateur (A), le réseau en échelle comprenant n éléments d'échelle en cascode ($S1, Si, Sn$), n étant égal ou supérieur à 1, chacun comprenant un premier transistor d'échelle (Nia) et un deuxième transistor d'échelle (Nib), i étant un numéro d'ordre inférieur ou égal à n, chaque élément d'échelle (Si) présen-



tant quatre bornes, une première borne (i1) étant couplée à la première électrode principale du premier transistor d'échelle (Nia), une deuxième borne (i2) étant couplée à l'électrode de commande du premier transistor d'échelle (Nia) et à la première électrode principale du deuxième transistor d'échelle (Nib), une troisième borne (i3) étant couplée à la deuxième électrode principale du premier transistor d'échelle (Nia) et à l'électrode de commande du deuxième transistor d'échelle (Nib), et une quatrième borne (i4) étant couplée à la deuxième électrode principale du deuxième transistor d'échelle (Nib), la première borne (i1) et la deuxième borne (i2) de chaque élément d'échelle (Si) étant couplées respectivement à la troisième borne (i3) et à la quatrième borne (i4) d'un élément d'échelle précédent (Si-1), la première borne (i1) et la deuxième borne (i2) du premier élément d'échelle (S1) étant couplées respectivement à l'entrée inverseuse (V2) de l'amplificateur (A) et à la deuxième électrode principale du troisième transistor (n3), et la troisième borne (n3) et la quatrième borne (n4) du dernier élément d'échelle (Sn) étant couplées respectivement à la première électrode principale du deuxième transistor (N2) et à la sortie (V0) de l'amplificateur.

5. Circuit amplificateur selon la revendication 2, caractérisé en ce qu'un réseau en échelle (P1...Pn) est disposé entre la deuxième électrode principale du troisième transistor (N3) et la sortie (V0) de l'amplificateur (A) et la première borne de tension d'alimentation (V_{dd}) et la deuxième borne de tension d'alimentation (V_{ss}), le réseau en échelle comprenant m éléments d'échelle en cascade (P1, Pj, Pm), m étant égal ou supérieur à 1, chacun comprenant un premier transistor d'échelle (Njc) et un deuxième transistor d'échelle (Njd) et une source de courant ($J_j + 5$), j étant un numéro d'ordre inférieur ou égal à m, chaque élément d'échelle (Pj) présentant six bornes, une première borne (j1) étant couplée à la première électrode principale du premier transistor d'échelle (Njc) et à l'électrode de commande du deuxième transistor d'échelle (Njd), une deuxième borne (j2) étant couplée à la deuxième électrode principale du premier transistor d'échelle (Njc), une troisième borne (j3) étant couplée à la première électrode principale du deuxième transistor d'échelle (Njd), une quatrième borne (j4) étant couplée à la source de courant ($J_j + 5$), une cinquième borne (j5) étant couplée à la deuxième électrode principale du premier transistor d'échelle (Njc) et la sixième borne (j6) étant couplée à l'électrode de commande du premier transistor d'échelle (Njc) et à la source de courant ($J_j + 5$), la première borne (j1) et la deuxième borne (j2) de chaque élément

d'échelle (Pj) étant couplées respectivement à la cinquième borne (j5) et à la sixième borne (j6) d'un élément d'échelle précédent (Pj-1), la troisième borne (j3) et la quatrième borne (j4) d'un élément d'échelle (Pj) étant couplées respectivement à la première borne de tension d'alimentation (V_{ss}) et à la deuxième borne de tension d'alimentation (V_{dd}), la première borne (j1) et la deuxième borne (j2) du premier élément d'échelle (P1) étant couplées respectivement à la deuxième électrode principale du troisième transistor (N3) et à la sortie (V0) de l'amplificateur (A), et la cinquième borne (j5) et la sixième borne (j6) du dernier élément d'échelle (Pm) étant couplées l'une à l'autre.

6. Circuit amplificateur selon la revendication 1, caractérisé en ce que l'amplificateur (A) comprend un troisième transistor (P2) présentant une première électrode principale, une deuxième électrode principale et une électrode de commande, qui est couplée à l'entrée inverseuse (V2) de l'amplificateur (A), une électrode de commande d'un troisième transistor (P3; N6) étant couplée à l'entrée non inverseuse (V1) de l'amplificateur (A), une première électrode principale étant couplée à la première électrode principale du troisième transistor (P2), et une deuxième électrode principale, une électrode de commande d'un cinquième transistor (N4) étant couplée à une deuxième borne de tension de référence (4) pour la réception d'une deuxième tension de référence, une première électrode principale étant couplée à la première borne de tension d'alimentation (V_{dd}) et à une deuxième électrode principale, et une électrode de commande d'un sixième transistor (N5) étant couplée à une troisième borne de tension de référence (5) pour la réception d'une troisième tension de référence, une première électrode principale étant couplée à la deuxième électrode principale du troisième transistor (P2) et une cinquième transistor (N4) et une deuxième électrode principale étant couplée à la deuxième borne de tension d'alimentation (V_{ss}) par l'intermédiaire d'une deuxième source de courant (J5) et à la sortie (V0) de l'amplificateur (A).
7. Circuit amplificateur selon la revendication 6, caractérisé en ce que la première électrode principale du quatrième transistor (P3) est couplée à la deuxième borne de tension d'alimentation (V_{dd}) par l'intermédiaire d'une troisième source de courant (J4) et la deuxième électrode principale du quatrième transistor (P3) est couplée à la première borne de tension d'alimentation (V_{dd}).
8. Circuit amplificateur selon la revendication 6, ca-



ractérisé en ce que la deuxième électrode principale du quatrième transistor (N6) est couplée à la deuxième borne de tension d'alimentation (V_{ss}).

9. Circuit amplificateur selon l'une des revendications précédentes, caractérisé en ce que le circuit amplificateur comprend en outre un transistor de référence (N10) présentant une première électrode principale couplée à la première électrode principale du transistor d'entrée (N8), une deuxième électrode principale couplée à la première borne de tension d'alimentation (V_{ss}) et une électrode de commande couplée à la deuxième borne de tension de référence (V_{ref4}).

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