

Description

- Arrangement for determining the configuration of a memory

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Memories are usually formed by insertion regions into which memory modules can be inserted. In this case, the insertion regions constitute plug-in locations into which memory modules of very diverse types having different storage capacities can be plugged. The insertion regions or the plug-in locations are in this case coordinated with commercially available memory modules or memory chips. The reading and writing of information from and to the memory is usually carried out by means of a memory controller. In addition to the data lines required for the communication of the data which has been read or is to be written, n address lines - for example 13 address lines are passed from the memory controller to the insertion regions or plug-in regions. Voltage potentials are routed to these address lines in the memory controller in such a way that binary coded address information items pass to all of the insertion regions or to memory modules inserted or plugged into the latter.

For error-free addressing, the memory controller must know the configuration of the memory of the memory arrangement. This means that knowledge about the presence of memory modules in the insertion regions and knowledge about the storage capacity of the inserted memory modules must be available in the memory controller. This is usually achieved by information - for example voltage potentials - applied to the terminals of the memory controller or by programming of an internal memory. This means additional adjustment and/or programming complexity.

The object on which the invention is based consists in reducing this additional adjustment and/or programming complexity. The object is achieved by means of the features of Claim 1.

The essential aspect of the method according to the invention is to be seen in the fact that at least one of the control lines or address lines passed to the insertion regions is used as an additional information line. For this purpose, coding means are provided for forming and communicating capacity information items via a capacity line - Claim 2 - and presence information items via a presence line - Claim 3 -, the presence information items indicating memory modules which have been inserted into the insertion region - that is to say the presence of said memory modules - and the capacity information items indicating the storage capacity of said memory modules. Assessment means are provided in the memory controller for the purpose of insertion region-specific assessment of the capacity and presence information items communicated via the capacity line and presence line.

According to an advantageous development of the method according to the invention, in each case at least one of the further address or control lines is determined as type lines for each of the insertion regions. Additional, insertion region-specific coding means are provided for forming and communicating memory module-specific type information items, the type information items in each case indicating the type of the memory module which has been inserted. To this end, additional assessment means are provided in the memory controller for the purpose of insertion region-specific assessment and storage of the type information items communicated via the type line - Claim 4. This means an extension of the method according to the invention for communicating a type information item - for example DRAM or SRAM - specified in the memory module to the memory controller.

According to an advantageous development of the method according to the invention, as coding means, in the memory controller a predetermined resistor, which is connected to a predetermined voltage potential, is connected to the capacity, presence and type lines, and

in each memory module, which has been inserted into an insertion region, a resistor indicating its presence and its storage capacity and its type is connected to the respective capacity and presence and type lines and to a predetermined voltage potential - Claim 5. This means that the resistor which is connected both to the capacity line and to a predetermined voltage potential is determined, for example, as a function of the storage capacity of the memory module - for example one or four Mbytes. In the case of a predetermined resistor [lacuna] to a predetermined voltage potential in the memory controller, different voltage potentials occur at the voltage divider point of the capacity line as a function of the magnitude of the resistance set in the insertion region or memory module, by means of which voltage potentials the storage capacity, the presence and the type of the memory module which has been inserted are indicated to the memory controller. In order to achieve an unambiguous voltage divider function, in the memory controller the resistor is connected to the voltage potential which corresponds to the voltage supply, and in the insertion regions to the earth potential - Claim 6. The resistor which is provided in the memory controller for each capacity, presence and type line is to be dimensioned in such a way that voltage potentials for address and control information formation can be routed by the memory controller to the n address lines and control lines, the control and address information formation being deactivated during the communication of the configuration information items - Claim 7. This means that the resistors in the memory controller and in the insertion regions are to be dimensioned in such a way that the voltage potentials for address and control information formation can be connected to the n address and control lines and voltage potentials are achieved by which the memory can be addressed and the corresponding control can be effected.

In order to identify the insertion regions, given a plurality of capacity lines, the capacity, presence and type information is formed by binary coded capacity, presence and type information item [sic] -

5 Claim 10. This means that a voltage potential representing the binary 0 or 1 information item is in each case routed to the capacity, presence and type lines in such a way that by joint consideration of the voltage potentials present on the capacity, presence

10 and type lines, a binary coded capacity, presence and type information item, respectively, is represented.

Further advantageous refinements of the arrangement according to the invention can be found in the further claims.

15 The arrangement according to the invention is explained in more detail below with reference to a block diagram. The block diagram shows a memory controller SAS and two of four insertion regions EB1...4, which together form the memory SP. Instead of the four

20 insertion regions EB1...4, it is possible according to the invention to configure different insertion regions which can be adapted to the respective application. Referring to the exemplary embodiment, it will be assumed, furthermore, that memory modules SM having a

25 storage capacity K_{1,4} of one or four Mbytes can be inserted or plugged into these insertion regions EB1...4, which are realized by suitable plug-in locations. In the exemplary embodiment, the memory modules SM constitute small printed circuit boards having integrated RAM

30 memory [sic] (Random Access Memory), which are also used, for example, in personal computers - indicated by a word RAM placed in brackets in the block diagram.

The memory controller SAS contains a controller ST, which contains the known functions of a commercially available RAM memory controller - known as a RAM

35 controller to technical specialists.

In each case two control lines SL1...8 are passed from each insertion region EB1...4 into the memory controller SAS. RAS signals RAS0...7 (Row Address

Strobe) which are frequently used by the memory controller SAS are transmitted, for example, via these control lines SL1...8. Together with a CAS signal (Column Address Strobe), the columns and rows of the memory SP are addressed, that is to say at a predetermined voltage potential, the addresses present are determined as row and column addresses. In the absence of an RAS signal RAS0...7, the control lines SL1...8 each have a high voltage potential, in which case this voltage may vary in practice on account of realization tolerances. In order to avoid these voltage fluctuations, in the memory controller SAS each control line SL1...8 is connected via a series resistor RV to the stabilized supply voltage +V - illustrated once in the block diagram by way of example for the eight control lines SL1...8. Furthermore, in the memory controller SAS a respective line transceiving unit LSE is connected to each control line SL1...8 - one of the eight line transceiving units LSE is illustrated by way of example in the block diagram. In each of the line transceiving units LSE, the control line SL1...8 is connected to the input of one line amplifier LV and to an output of a further line amplifier LV. The output and the input, respectively, of the two line amplifiers LV are connected to the controller ST. The voltage potentials which have been received or are to be communicated are forwarded unchanged by the line amplifiers LV, only impedance transformation being carried out. During the communication of the capacity, presence and type information k_i, v_i, t_i , the line amplifiers LV which act in the direction of the insertion regions EB1...4 acquire a high impedance, that is to say are deactivated. The line amplifier LV which acts in the direction of the controller ST remains active and forwards the voltage potential occurring at the voltage divider point SPT to the controller ST for the purpose of measurement and assessment.

In each of the insertion regions EB1...4, one of the control lines SL1...8 is determined as the

capacity line and one is determined as the presence line - in the exemplary embodiment, for the first insertion region EB1, the first control line SL1 is determined as the capacity line and the second control line SL2 as the presence line. The two control lines SL1...8 of an insertion region EB1...4 can be respectively connected to a resistor R1...8. The connection configuration of the two resistors R1...8 is implemented as a function of the presence of a plugged-in memory module SM and its storage capacity. If no memory module SM is plugged in, no second resistor R2,4,6,8 is connected from the negative voltage potential -V - in practice earth potential - to the respective control lines [sic] SL2,4,6,8 representing the presence line. When a memory module SM is inserted, a second resistor R2,4,6,8 arranged on the circuit board or the memory module SM is connected from earth potential -V to the respective control line SL2,4,6,8 representing the presence line. This means that in the memory controller SAS the voltage level at the voltage divider point SPT for the respective control line SL2,4,6,8 drops to a low voltage level provided that the line amplifier LV which acts in the direction of the insertion regions EB1...4 is driven to a high impedance by the controller ST. The low voltage level consequently indicates to the memory controller that a memory module SM is plugged in the respective insertion region EB1 and a high voltage potential indicates that no memory module SM is plugged in the respective insertion region EB1...4. In accordance with the voltage level measured by the control unit ST, a presence information item vi - advantageously represented by a binary information item - is formed in the said control unit and stored. The controller ST switches the line amplifiers LV which act in the direction of the insertion regions EB1...4 to a high impedance only for the purpose of measuring the communicated capacity, presence and type information ki,vi,ti.

Given a plugged-in memory module SM in an insertion region EB1...4, the storage capacity [lacuna] specified by the configuration of the first resistor R1,3,5,7. If no first resistor R1,3,5,7, which is to be
5 arranged in the memory module SM, is connected from earth potential -V to the respective control line SL1,3,5,7 representing the capacity line, then the inserted memory module SM has a large storage capacity - for example 4 Mbytes - and if a first resistor
10 R1,3,5,7 is connected, then the inserted memory module SM has a small storage capacity - for example 1 Mbyte.

In the memory controller SAS, different voltage levels occur at the voltage divider point SPT of the respective control line SL1,3,5,7 as a function of the
15 configuration of the first resistor R1,3,5,7, which voltage levels are forwarded to the control unit ST via the line transceiving unit LSE and measured there. As a function of the magnitude of the measured voltage levels, capacity information items ki indicating a large
20 or small storage capacity are formed for each insertion region EB1...4 and stored in an insertion region-specific manner. The two resistors R1...8 can each be configured during the production of the memory modules SM or of the circuit boards, that is to say can be incorporated in the latter in an economical manner from the
25 point of view of production engineering.

In the exemplary embodiment, furthermore, issuing from the control unit ST of the memory controller SAS, 13 address lines ADL1...13 are connected via a re-
30 spective line transceiving unit LSE in parallel to each insertion region EB1...4. The address lines ADL are connected to the memory modules SM in the insertion regions EB1...4. It will be assumed for the exemplary embodiment that an additional configuration information
35 item, namely a type information item ti, is to be communicated via in each case one of the address lines ADL1...13. For this purpose, the first to fourth address line ADL1...4 is determined as type line for the first to fourth insertion region EB1...4. As type

information item t_i , for example, a high voltage potential represents a "fast memory module" and a low voltage potential represents a "slow memory module".

In a manner analogous to the connection of the control lines $SL1...8$, the four determined address lines $ADL1..4$ are connected in the memory controller SAS to the positive supply voltage $+V$ via a respective resistor RV - indicated by the resistor RV in the block diagram. In the insertion regions $EB1...4$, a type resistor RT , which is connected to the earth potential $-V$, can be connected to the assigned address lines $ADL1..4$ - indicated by one [lacuna] illustrated resistors RT in the block diagram. Referring to the exemplary embodiment, no resistors RT are connected in the event of fast memory modules SM having been inserted and resistors RT are connected in the event of slow memory modules SM having been inserted. The voltage potential at the voltage divider point SBT is communicated and measured analogously to the communication and measurement of the capacity and presence information vi . Incorrect population of the insertion regions $EB1..4$ can be ascertained by these measurements, that is to say all of the insertion regions $EB1..4$ must be populated with slow or fast memory modules SM , since memory modules SM having different access speeds do not interact. In the respective insertion regions $EB1..4$, the unconnected address lines $ADL2-12..A1-3/5-13$ - that is to say those having no resistor circuitry - are connected to the plug-in devices of the memory modules SM .

In the case of a plurality of address lines ADL , a type information item t_i to be communicated is alternatively specified by a binary coding of the address lines ADL - not illustrated -, a non-connected resistor RT denoting a high potential and thus a binary 1 information item and a connected resistor RT denoting a low voltage potential and thus a binary 0 information item at the voltage divider point SP [sic]. The type information item t_i specifies, in particular, the type

of the inserted memory module SM via the address lines ADL present - for example SRAM or DRAM -, a predetermined number of address lines ADL being respectively assigned to an insertion region EB1..4.

5 Since the memory modules SM are usually realized by very diverse chips and chip types, communicating the type information item t_i to the control unit ST of the memory controller SAS makes it possible to check the extent to which uniform memory chip types or memory

10 chip types which cooperate in practice have been inserted into the respective insertion regions EB1...4.

The arrangement according to the invention consequently makes it possible to communicate not only capacity and presence information k_i, v_i but also type information items t_i and further configuration information items not described, as a result of which extensive knowledge about the storage capacity and the presence of memory modules SM and knowledge about the memory chip types used are present in the control unit

15 ST. In this case, the voltage potentials present at the voltage divider points SPT of the address lines ADL which represent the type lines are forwarded via the line transceiving units LSE to the control unit ST. In the latter, the voltage potentials are measured and,

20 following decoding, are stored as type information - advantageously in a binary form. It should be taken into consideration here that in each case specific address lines ADL are assigned to specific insertion regions EB1..4, taking account of the addressing

25 procedure or addressing method used, in order to achieve unambiguous assignment of the communicated type information items t_i to the insertion regions EB1..4.

The measurement of the voltage potentials present at the voltage divider point SPT can be carried out

35 by means of an externally arranged analog/digital converter chip or by means of an analog/digital converter chip which is integrated in the control unit ST or already present in the latter - not illustrated. In the case of external arrangement, the line transceiving

units LSE must be realized externally, that is to say not in the memory controller SAS. Using the stored configuration information items k_i, v_i, t_i , the control unit ST of the memory controller SAS can automatically determine a suitable setting for addressing the inserted memory modules SM, the memory controller SAS being connected in a known manner to a microprocessor MP, which controls and monitors the memory controller SAS.



Patent Claims

1. Arrangement for determining the configuration of a memory (SP), which is formed by insertion regions (EB1..4) which accommodate memory modules (SM) and to
5 which address lines (ADL1..13) issuing from a memory controller (SAS) are passed in parallel, and having at least one insertion region-specific control line (SL1..8) in each case from the memory controller (SAS) to each insertion region (EB1..4),
10 - in which at least one of the address or control lines (ADL1..13, SL1..8) is determined as the information line for each insertion region (EB1..4),
- having coding means (RV,R1,R2) for forming and communicating insertion region-specific configuration
15 information items (vi,ki,ti) from the memory (SP) via the at least one information line to the memory controller (SAS), and
- having assessment means (ST) in the memory controller (SAS) for the insertion region-specific assessment and storage of the configuration information
20 items (ki,vi,ti) communicated via the information line.
2. Arrangement according to Claim 1, characterized
- in that at least in each case one of the address or
25 control lines (SL1..8,ADL1..13) connected between the memory controller (SAS) and an insertion region (EB1..4) is determined as the capacity line (SL1,3,5,7) for each insertion region (EB1..4), and
- in that insertion region-specific coding means
30 (R1,R2,RV) for forming and communicating capacity information items (ki) via the respective capacity line are provided, the capacity information items (ki) in each case indicating the storage capacity of the inserted memory modules (SM).
- 35 3. Arrangement according to Claim 1 or 2, characterized
in that at least in each case one of the further address or control lines (SL1..8,ADL1..13) connected between the memory controller (SAS) and an



insertion region (EB1..4) is determined as the presence line (SL2,4,6,8) for each insertion region (EB1..4), and

- in that insertion region-specific coding means (R1,R2,RV) for forming and communicating presence information items (vi) via the respective presence line are provided, the presence information item [sic] (vi) in each case indicating the presence of a memory module (SM) which has been inserted into the respective insertion region (EB1..4).

4. Arrangement according to one of Claims 1 to 3, characterized

- in that in each case at least one of the further address or control lines (ADL1..13, SL1..8) is determined as type lines (ADL1..4) for each of the insertion regions (EB1..4),
- in that additional, insertion region-specific coding means (RV, TR) for forming and communicating memory module-specific type information items (ti) are provided, the type information items (ti) in each case indicating the type of the memory module (SM) which has been inserted, and
- in that additional assessment means (ST) are provided in the memory controller (SAS) for the insertion region-specific assessment and storage of the type information items (ti) communicated via the type line.

5. Arrangement according to one of Claims 1 to 4, characterized

- in that, as coding means (RV,RT,R1,2),
 - in the memory controller (SAS) a predetermined resistor (RV), which is connected to a predetermined voltage potential (+V), is connected to each capacity, presence and type line, and
 - in the [sic] each memory module (SM), which has been inserted into an insertion region (EB1..4), a resistor (R1,2,RT) indicating its presence and its storage capacity and its type is connected to the



respective capacity and presence and type line and to a predetermined voltage potential (-V).

6. Arrangement according to Claim 5, characterized in that in the memory controller (SAS) the resistors (RV) are connected to the voltage potential (+V) which is provided for the voltage supply, and in the insertion regions (EB1..4) the resistors (R1,2,RT) are connected to the earth potential (-V).

7. Arrangement according to Claim 5 or 6, characterized in that the resistors (RV,R1,R2,RT), which are provided for each capacity, presence and type line, in the memory controller (SAS) and the insertion regions (EB1..4) are dimensioned in such a way that voltage potentials formed for the purpose of control and address information formation can be routed by the memory controller (SAS) to the control lines (SL1..8) and address lines (ADL1..13), the control and address information formation being deactivated during the communication of the configuration information items (ki,vi,ti).

8. Arrangement according to Claim 7, characterized in that voltage assessment means (ST) for assessing the voltage potentials present on the capacity, presence and type lines are provided in the memory arrangement (SAS) and configured in such a way that, as a function of the voltage potential present, a capacity, presence and type information item (ki,vi,ti) indicating the storage capacity, the presence and the type, respectively, of the memory module (SM) which has been inserted is formed and stored for each insertion region (EB1..4) in a manner appropriate to the memory, the means (LV) for communicating the control and address information items to the insertion regions (EB1..4) being switched to a high impedance.

9. Arrangement according to Claim 8, characterized in that the capacity, presence and type information item [sic] (ki,vi,ti) are represented by binary information items and stored.

10. Arrangement according to one of the preceding claims, characterized in that in the case of a



plurality of capacity, presence and type lines, the capacity, presence and type information item [sic] (ki,vi,ti) are formed by binary coded capacity, presence and type information items.

- 5 11. Arrangement according to Claim 10, characterized in that additional decoding means (ST) for assessing the binary coded voltage potentials present on the capacity and presence and type lines are provided in the memory controller (SAS) and configured in such a
10 way that, as a function of the binary coded voltage potential present, a capacity, presence and type information item (ki,vi,ti) indicating the storage capacity, the presence and the type, respectively, of the memory module (DM [sic]) which has been inserted is formed and
15 stored.