CLAIMS

1. A structure comprising:
   - a patterned crystalline semiconductor substrate with elevated regions (110, 130, 410, 610, 710) bounded by trenches (120, 320, 420, 430, 620, 720), the depth (h) of said trenches larger than their width (d); and
   - epitaxial semiconductor material deposited on said elevated substrate regions in the form of isolated, semiconductor patches (330);

   wherein perpendicular sidewalls (351) of adjacent patches are spaced, the spacing of said semiconductor patches being smaller than their width (314), so that most of the epitaxial material is deposited on top of said elevated regions.

2. The structure of claim 1, wherein:
   - said substrate is made from a first crystalline semiconductor material; and
   - said epitaxial semiconductor material comprises at least one second crystalline semiconductor material having a lattice mismatch or thermal mismatch to said substrate.

3. The structure of claim 1, wherein epitaxial regions consisting of merged structures (570) are formed on said elevated regions.

4. The structure of claim 1, wherein the spacing of said perpendicular sidewalls (351) is smaller than the width (d) of said trenches.

5. The structure of claim 1, wherein said elevated substrate regions are faceted.

6. The structure of claim 1, wherein sidewalls (650) and bottoms (640) of said trenches are covered with a dielectric layer (630) of thickness d_{ox}, said thickness d_{ox} being small with respect to the trench width (d).

7. The structure of claim 1, wherein said elevated regions comprise at least one region, the boundary of which is aligned along a high-symmetry direction of said substrate.

8. The structure of claim 1, wherein said trenches comprise at least one trench (720) which is under-etched.

9. The structure of claim 1, wherein said patches have facets (360).

10. The structure of claim 1, wherein said patches have horizontal surfaces (326).

11. The structure of claim 1, wherein said substrate is one of a group of substrates consisting of Si, SOI, Ge, GeOI, GaAs, InP, InSb, CdTe, SiC, Al_2O_3, A1N and GaN.

12. The structure of claim 1, wherein said epitaxial semiconductor material is one of a group of semiconductor materials, consisting of elemental group IV semiconductors and their alloys, and compound semiconductors from group III-V, group II-VI, and group IV-VI, and their alloys.

13. The structure of claim 1, wherein said epitaxial semiconductor material comprises a layer with compositional grading, said graded layer being chosen among a group of alloys consisting of an alloy of group IV, group III-V, group II-VI, and group IV-VI semiconductors.

14. The structure of claim 1, wherein said epitaxial semiconductor material comprises an active layer stack made from a plurality of semiconductor layers, such plurality selected from a group of semiconductor layers consisting of elemental group IV semiconductors and their alloys, and compound semiconductors from group III-V, group II-VI and group IV- VI, and their alloys.

15. A method of forming the structure of claim 1 having isolated semiconductor patches (330) on elevated regions, wherein it comprises the steps of:

- forming a patterned crystalline semiconductor substrate, the pattern comprising elevated regions (110, 130, 410, 610, 710) bounded by trenches (120, 320, 420, 430, 620, 720);
- loading the substrate into an epitaxy reactor;
- epitaxially depositing at least one semiconductor material on said elevated regions obtaining a vertical growth rate that is predominant with respect to the

lateral growth rate by tuning the surface diffusion lengths to be below facet sizes and by reducing the reactant supply to the sidewalls of said elevated regions, exploiting the mutual shielding of the incoming flux provided by said elevated regions;

- narrowing the trenches (120, 320) between said semiconductor patches by epitaxial growth.

16. The method of claim 15, wherein epitaxial growth conditions are tuned during growth, thereby favouring inclined facets (361, 362) to form, and thereby deflecting vertical defects (380) into oblique directions (381), whereby said defects may exit through sidewalls (351) of said closely spaced patches.

17. A semiconductor product comprising a structure of any one of the previous claims from 1 to 14.

CLAIMS

1. A structure comprising:
   - a patterned crystalline semiconductor substrate with elevated regions bounded by trenches, the depth (h) of said trenches larger than their width (d); and
   - epitaxial semiconductor material deposited on said elevated substrate regions in the form of isolated, semiconductor patches;

   wherein perpendicular sidewalls of adjacent patches are spaced, the spacing of said perpendicular sidewalls being smaller than the width (d) of said trenches, so that most of the epitaxial material is deposited on top of said elevated regions.

2. The structure of claim 1, wherein:
   - said substrate is made from a first crystalline semiconductor material; and
   - said epitaxial semiconductor material comprises at least one second crystalline semiconductor material having a lattice mismatch or thermal mismatch to said substrate.

3. The structure of claim 1, wherein epitaxial regions consisting of merged structures are formed on said elevated regions.

4. The structure of claim 1, wherein said elevated substrate regions are faceted.

5. The structure of claim 1, wherein sidewalls and bottoms of said trenches are covered with a dielectric layer of thickness d_{ox}, said thickness d_{ox} being small with respect to the trench width (d).

6. The structure of claim 1, wherein said elevated regions comprise at least one region, the boundary of which is aligned along a symmetry direction of said substrate.

7. The structure of claim 1, wherein said trenches comprise at least one trench which is under-etched.

8. The structure of claim 1, wherein said patches have facets.

9. The structure of claim 1, wherein said patches have horizontal surfaces.

10. The structure of claim 1, wherein said substrate is one of a group of substrates consisting of Si, SOI, Ge, GeOI, GaAs, InP, InSb, CdTe, SiC, $A1_2O_3$, A1N and GaN.

11. The structure of claim 1, wherein said epitaxial semiconductor material is one of a group of semiconductor materials, consisting of elemental group IV semiconductors and their alloys, and compound semiconductors from group III-V, group II-VI, and group IV-VI, and their alloys.

12. The structure of claim 1, wherein said epitaxial semiconductor material comprises a graded layer with compositional grading, said graded layer being chosen among a group of alloys consisting of an alloy of group IV, group III-V, group II-VI, and group IV-VI semiconductors.

13. The structure of claim 1, wherein said epitaxial semiconductor material comprises an active layer stack made from a plurality of semiconductor layers, such plurality selected from a group of semiconductor layers consisting of elemental group IV semiconductors and their alloys, and compound semiconductors from group III-V, group II-VI and group IV- VI, and their alloys.

14. A method of forming the structure of claim 1 having isolated semiconductor patches on elevated regions, wherein it comprises the steps of:
    - forming a patterned crystalline semiconductor substrate, the pattern comprising elevated regions bounded by trenches;
    - loading the substrate into an epitaxy reactor;

- epitaxially depositing at least one semiconductor material on said elevated regions obtaining a vertical growth rate that is predominant with respect to the lateral growth rate by tuning the surface diffusion lengths to be below facet sizes and by reducing the reactant supply to the sidewalls of said elevated regions, exploiting the mutual shielding of the incoming flux provided by said elevated regions;
- narrowing the trenches between said semiconductor patches by epitaxial growth.

15. The method of claim 14, wherein epitaxial growth conditions are tuned during growth, thereby favouring inclined facets to form, and thereby deflecting vertical defects into oblique directions, whereby said defects may exit through sidewalls of said closely spaced patches.

16. A semiconductor product comprising a structure of any one of the previous claims from 1 to 13.