CLAIMS

WHAT IS CLAIMED IS:

1. A three-dimensional semiconductor memory device, comprising:

first semiconductor patterns, which are vertically stacked on a substrate and are spaced apart from each other along a vertical direction, each of the first semiconductor patterns including:

a first end portion and a second end portion spaced apart from each other, and

a first side surface and a second side surface spaced apart from each other, each of the first and second side surfaces connecting the first end portion to the second end portion;

a first source/drain region and a second source/drain region in each of the first semiconductor patterns, the first and second source/drain regions being respectively adjacent to the first and second end portions;

a channel region in each of the first semiconductor patterns, the channel region being between the first and second source/drain regions;

a first word line adjacent to the first side surfaces of the first semiconductor patterns and the channel regions, the first word line extending in the vertical direction perpendicular to a top surface of the substrate; ~~and~~

a gate insulating layer between the first word line and the first side surfaces of the first semiconductor patterns, the gate insulating layer extending between first source/drain regions of adjacent first semiconductor patterns and filling a space between the adjacent first semiconductor patterns,

wherein a side surface of the first word line, which is in contact with the gate insulating layer, has a concavo-convex structure such that the first word line is adjacent to top and bottom surfaces of the first semiconductor patterns.

~~2. The device as claimed in claim 1, wherein the gate insulating layer fills a space between the adjacent first semiconductor patterns.~~

~~3~~2. The device as claimed in claim 1~~ or claim 2~~, further comprising an air gap region, the air gap region being between the adjacent first semiconductor patterns to expose the gate insulating layer.

~~4~~3. The device as claimed in ~~any one of claims 1 to 3~~claim 1, wherein a portion of the first word line extends between the adjacent first semiconductor patterns.

~~5~~4. The device as claimed in claim ~~4~~3, wherein the first word line includes a void between the adjacent first semiconductor patterns.

~~6~~5. The device as claimed in any one of claims 1 to ~~5~~4, further comprising an interlayered insulating layer between the adjacent first semiconductor patterns, the interlayered insulating layer being in contact with the gate insulating layer, and is formed of a material different from the gate insulating layer.

~~7~~6. The device as claimed in any one of claims 1 to ~~6~~5, further comprising:

second semiconductor patterns, which are vertically stacked on the substrate and are spaced apart from each other and from the first semiconductor patterns, the second semiconductor patterns including third side surfaces, respectively, which are adjacent to the first side surfaces of the first semiconductor patterns;

a second word line adjacent to the third side surfaces of the second semiconductor patterns, the second word line extending in the vertical direction perpendicular to the top surface of the substrate; and

a shielding line between the first and second word lines, the shielding line being spaced apart from the first and second word lines.

~~8~~7. The device as claimed in claim ~~7~~6, wherein the first word line, the second word line, and the shielding line are parallel to the vertical direction and have a same width.

~~9~~8. The device as claimed in any one of claims 1 to ~~8~~7, wherein an upper width of the first word line measured in a first direction is different from a lower width of the first word line measured in the first direction, the first direction being parallel to the top surface of the substrate.

~~10~~9. The device as claimed in claim ~~9~~8, wherein a width of a lowermost one of the first semiconductor patterns measured in a second direction is different from a width of an uppermost one of the first semiconductor patterns measured in the second direction, the second direction being parallel to the top surface of the substrate and different from the first direction.

~~11~~10. The device as claimed in any one of claims 1 to ~~10~~9, wherein, in each of the first semiconductor patterns, the first end portion has a first thickness, the second end portion has a second thickness, and the first thickness is different from the second thickness in the vertical direction.

~~12~~11. The device as claimed in any one of claims 1 to ~~11~~10, further comprising bit lines in contact with the first end portions of the first semiconductor patterns, respectively, the bit lines extending in a second direction parallel to the top surface of the substrate,

wherein each of the bit lines has a first thickness at a position in contact with the first end portions and has a second thickness, which is different from the first thickness, at a position spaced apart from the first end portions.

~~13~~12. The device as claimed in any one of claims 1 to ~~12~~11, further comprising data storage electrodes in contact with the second end portions of the first semiconductor patterns, respectively, a thickness of the data storage electrodes being different from a thickness of the first semiconductor patterns.

~~14~~13. A three-dimensional semiconductor memory device, comprising:

at least one first semiconductor pattern and at least one second semiconductor pattern on a substrate, the at least one first semiconductor pattern and the at least one second semiconductor pattern being spaced apart from each other in a first direction;

a first word line between the at least one first semiconductor pattern and the at least one second semiconductor pattern, the first word line being adjacent to the at least one first semiconductor pattern;

a second word line between the at least one first semiconductor pattern and the at least one second semiconductor pattern, the second word line being adjacent to the at least one second semiconductor pattern; and

a shielding line between the first and second word lines, the shielding line being insulated from the first and second word lines,

wherein the at least one first semiconductor pattern includes a plurality of first semiconductor patterns stacked on the substrate and spaced apart from each other,

wherein the device further includes a gate insulating layer between the first word line and side surfaces of the plurality of first semiconductor patterns, the gate insulating layer filling a space between adjacent ones of the plurality of first semiconductor patterns, and

wherein a side surface of the first word line, which is in contact with the gate insulating layer, has a concavo-convex structure such that the first word line is adjacent to top and bottom surfaces of the plurality of first semiconductor patterns.

~~15~~14. The device as claimed in claim ~~14~~13, wherein each of the first word line, the second word line, and the shielding line extends from a top surface of the substrate in a vertical direction, and a side surface of the shielding line is aligned with side surfaces of the first and second word lines.

~~16~~15. The device as claimed in claim ~~14~~ 13 or claim ~~15~~14, wherein:

~~the at least one first semiconductor pattern includes a plurality of first semiconductor patterns stacked on the substrate and spaced apart from each other,~~

each of the plurality of first semiconductor patterns includes a first end portion and a second end portion, which are spaced apart from each other,

the device further includes:

a first source/drain region and a second source/drain region in each of the plurality of first semiconductor patterns, the first and second source/drain regions being adjacent to the first and second end portions, respectively;

a channel region in each of the plurality of first semiconductor patterns, the channel region being between the first and second source/drain regions;

a first interlayered insulating layer between the channel regions of the plurality of first semiconductor patterns; and

a second interlayered insulating layer between the first source/drain regions or between the second source/drain regions of the plurality of first semiconductor patterns, the first interlayered insulating layer including a material different from that of the second interlayered insulating layer.

~~17. The device as claimed in claim 14 or claim 15, wherein the at least one first semiconductor pattern includes a plurality of first semiconductor patterns, which are stacked on the substrate and are spaced apart from each other, and~~

~~the device further includes spaces between adjacent ones of the plurality of first semiconductor patterns, the spaces exposing top and bottom surfaces of the first semiconductor patterns.~~

~~18~~16. The device as claimed in claim ~~14~~ 13 or claim ~~15~~14, wherein the ~~at least one first semiconductor pattern includes a plurality of first semiconductor patterns, which are stacked on the substrate and are spaced apart from each other, and~~

~~the device further includes a~~ gate insulating layer ~~covering~~ covers the top, the bottom, and the side surfaces of the plurality of first semiconductor patterns.

19. The device as claimed in claim 18, wherein the gate insulating layer fills a space between adjacent ones of the plurality of first semiconductor patterns.

20. A three-dimensional semiconductor memory device, comprising:

interlayered insulating layers and semiconductor patterns, which are alternately stacked on a substrate; and

a word line penetrating the semiconductor patterns and the interlayered insulating layers, the word lines being adjacent to the substrate,

wherein the word line includes:

a word line portion vertically extending from a top surface of the substrate, and

protruding portions protruding from a side surface of the word line portion toward the interlayered insulating layers, the protruding portions being spaced apart from each other.