CLAIMS

[Claim 1]

A lead frame, comprising:

a plurality of lead portions, wherein

at least a part of an upper surface of the lead portion and a sidewall surface of the lead portion is a rough surface having been subjected to roughening treatment, and

a value of a* in a CIELab color space of the rough surface is within a range from 12 to 19, and a value of b* is within a range from 12 to 17.

[Claim 2]

The lead frame according to claim 1, wherein

a part of the upper surface of the lead portion and the sidewall surface of the lead portion is the rough surface, and

a metal plating layer is provided on, of the upper surface of the lead portion, a part that is not the rough surface.

[Claim 3]

The lead frame according to claim 2, wherein

the metal plating layer includes at least one of an Ag plating layer, an Ni plating layer, a Pd plating layer, or an Au plating layer.

[Claim 4]

The lead frame according to claim 1, wherein

the lead portion includes an inner lead portion thinned from a lower surface side of the lead portion, and

a lower surface of the inner lead portion is the rough surface.

[Claim 5]

The lead frame according to claim 1, further comprising:

a die pad portion on which a semiconductor element is mountable, wherein

the plurality of lead portions is disposed around the die pad portion, and

the rough surface comprises an upper surface of the die pad portion and a sidewall surface of the die pad portion.

[Claim 6]

The lead frame according to claim 1 to be used for manufacturing a semiconductor device that includes a molding portion that seals at least the plurality of lead portions, wherein

the rough surface comprises an upper surface of the lead portion in contact with the molding portion and a sidewall surface of the lead portion in contact with the molding portion.

[Claim 7]

A method of manufacturing a lead frame, comprising:

a metal substrate preparation step of preparing a metal substrate that has a first surface and a second surface that is an opposite of the first surface;

a metal substrate processing step of forming a plurality of lead portions by processing the metal substrate; and

a rough surface forming step of forming a rough surface by roughening at least a part of an upper surface of the lead portion and a sidewall surface of the lead portion, wherein
in the rough surface forming step, the roughening is performed such that a value of a* in a CIELab color space of the rough surface is within a range from 12 to 19, and a value of b* is within a range from 12 to 17.

[Claim 8]

The method of manufacturing the lead frame according to claim 7,

wherein

alkaline treatment is applied to the lead portion after the rough surface forming step.

[Claim 9]

The method of manufacturing the lead frame according to claim 7,

wherein

a metal plating layer is provided on a part of the upper surface of the lead portion, and,

in the rough surface forming step, a part of the upper surface of the lead portion where the metal plating layer is not provided and the sidewall surface thereof are roughened.

[Claim 10]

The method of manufacturing the lead frame according to claim 9,

wherein

the metal plating layer includes at least one of an Ag plating layer, an Ni plating layer, a Pd plating layer, or an Au

plating layer.

[Claim 11]

The method of manufacturing the lead frame according to claim 7,

wherein,

in the metal substrate processing step, the lead portion that includes an inner lead portion thinned from a lower surface side of the lead portion is formed, and, in the rough surface forming step, the rough surface is formed at a lower surface of the inner lead portion.

[Claim 12]

The method of manufacturing the lead frame according to claim 7,

wherein,

in the metal substrate processing step, a die pad portion on which a semiconductor element is mountable is formed such that the plurality of lead portions is disposed around the die pad portion, and

in the rough surface forming step, the rough surface is formed by roughening an upper surface of the

die pad portion and a sidewall surface of the die pad portion and at least a part of an upper surface of the lead portion and a sidewall surface of the lead portion.