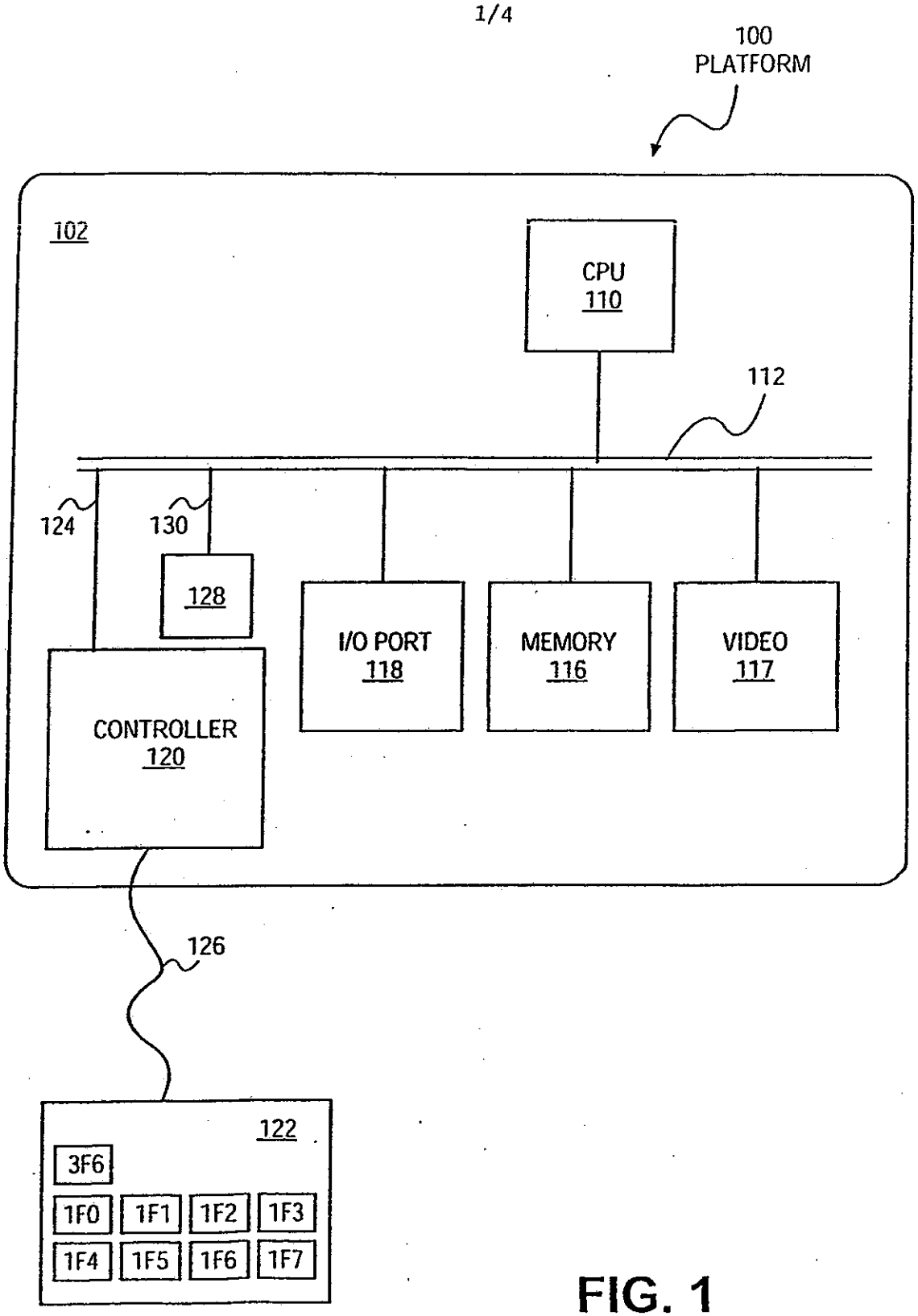

100
PLATFORM
102
CPU
110
112
124
130
128
I/O PORT
118
MEMORY
116
VIDEO
117
CONTROLLER
120
126
122
3F6
1F0
1F1
1F2
1F3
1F4
1F5
1F6
1F7

FIG. 1

Address storage device 122 so as to command the attention of storage device 122.

Read an alt-status register of storage device 122 to determine whether storage device 122 is busy.

If storage device 122 is busy, then return a "SRB_STATUS_BUSY" signal.

If storage device 122 is not busy, determine whether the BM is active.

If the BM engine is active, then the BM engine may be turned off and the drive reset.

If the BM engine is not active, then calculate the block count and the program device.

Calculate the logical block address (LBA) and the program device.

Programming up the direct memory access (DMA) descriptor table contents.

The command register of Table I may be programmed with a read or write command.

The DMA engine may be programmed.

Wait for an interrupt signal.

Receive an interrupt signal.

FIG. 2

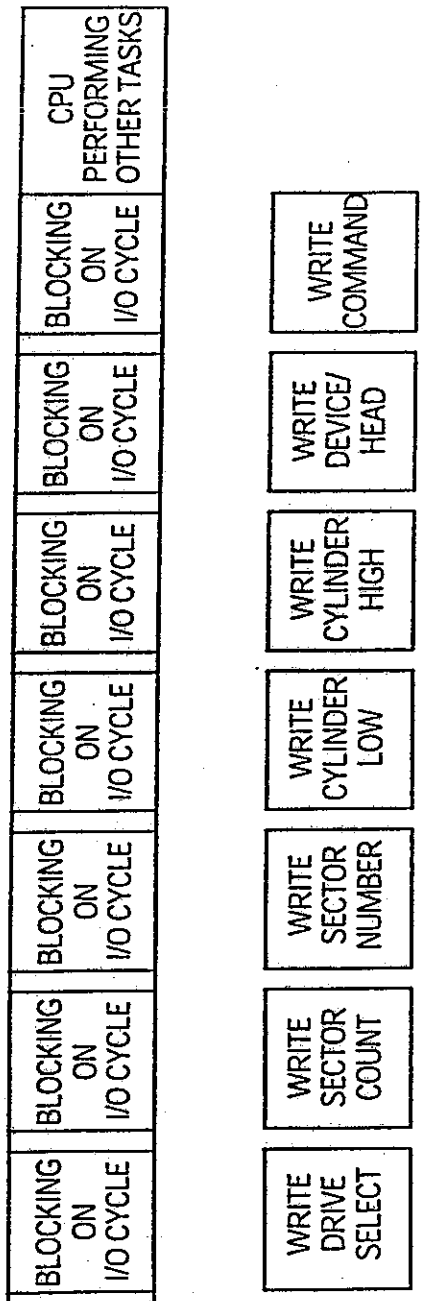

CPU ACTIVITY:
CPU PERFORMING OTHER TASKS
BLOCKING ON I/O CYCLE
BLOCKING ON I/O CYCLE
BLOCKING ON I/O CYCLE
BLOCKING ON I/O CYCLE
BLOCKING ON I/O CYCLE
BLOCKING ON I/O CYCLE
BLOCKING ON I/O CYCLE
CPU PERFORMING OTHER TASKS
ATA CHANNEL ACTIVITY:
WRITE DRIVE SELECT
WRITE SECTOR COUNT
WRITE SECTOR NUMBER
WRITE CYLINDER LOW
WRITE CYLINDER HIGH
WRITE DEVICE/ HEAD
WRITE COMMAND

FIG. 3

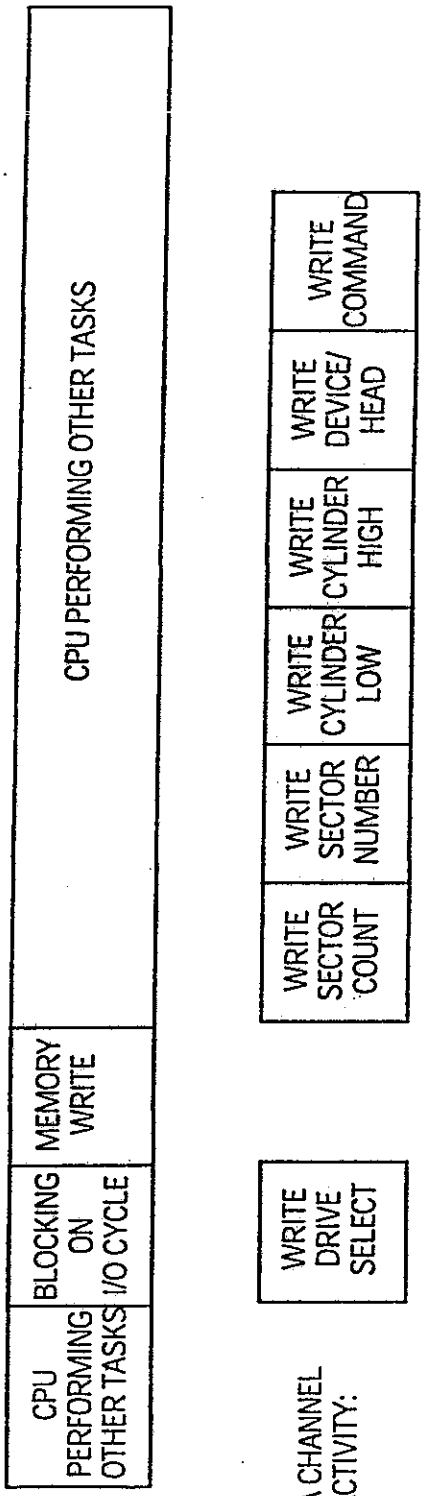

CPU ACTIVITY:
CPU PERFORMING OTHER TASKS
BLOCKING ON I/O CYCLE
MEMORY WRITE
CPU PERFORMING OTHER TASKS
ATA CHANNEL ACTIVITY:
WRITE DRIVE SELECT
WRITE SECTOR COUNT
WRITE SECTOR NUMBER
WRITE CYLINDER LOW
WRITE CYLINDER HIGH
WRITE DEVICE/ HEAD
WRITE COMMAND

FIG. 4