

SOFTWARE PROGRAMMABLE LOGIC ARRAY

(13)

Background Of The Invention

Programmed logic arrays, often referred to as PLAs are well known circuits for producing a set of predetermined output signals, the values of which depend upon the values of the inputs to the PLA. In the prior art, ordinary logic gates, such as NAND gates and/or NOR gates, or other known logic arrays may be utilized to construct a PLA. Alternatively, in the prior art, read only memories (ROMs) are also utilized as PLAs. For example, each address within a ROM can be initialized to a desired value. In this manner, by placing appropriate signals on the address lines of a ROM, a particular location in the ROM is addressed and its contents can then be placed on the output lines of the ROM. Of course, once desired values are loaded into locations in the ROM, such values become fixed. Although programmable ROMs are available (PROMs), by their very nature, such PROMs cannot be changed during normal operation. That is, in order to reprogram a PROM, it is necessary to subject the PROM to an environment which is substantially different than that encountered during its normal operation. In particular, PROMs may be UV PROMs or EE PROMs for ultraviolet erasable or electronically erasable PROMs respectively. In order to reprogram UV PROMs, it is necessary to remove the device from its normal operating environment and place it into a device specially designed to program the PROM. Similarly, in order to reprogram an EE PROM, voltages much higher than those utilized in logic circuits during normal operation must be provided.

Thus, while PLAs are extremely useful devices for providing predetermined output signals in response to received input signals, they cannot be utilized in applications wherein the

predetermined output signals must be dynamically changed notwithstanding that the same set of input signals are input to the PLA.

Of course, it is possible to build a PLA which provides all possible outputs. For example, if a PROM is utilized as a PLA
5 then, if there are eleven outputs, all possible outputs can be provided in an array of 2^{10} locations. However, excepting in cases where it is necessary to use all or substantially all possible outputs, such an array would be extremely inefficient since most locations would never be accessed. Additionally, even
10 with an array capable of producing all possible outputs, the output for a particular input would necessarily always be the same.

Summary Of The Invention

A software programmable logic array ("SPLA") is disclosed for creating a logic array which can be dynamically programmed to provide any combination of predetermined outputs from any combination of desired inputs. The foregoing is accomplished by providing a first plane of programmable bits for producing a plurality of AND terms which are input to a second plane of programmable bits for producing a plurality of OR terms, which are then input into a third plane of programmable bits for producing a plurality of outputs, each having a desired polarity.

To accomplish the foregoing, in addition to the desired inputs to the SPLA which produce the predetermined outputs, a second set of inputs are provided which are available only during initialization of the SPLA to program each programmable bit so that the predetermined outputs can be produced as desired. The second set of inputs are generated by placing desired addresses and data on an address/data bus, which addresses are decoded such that each programmable bit can be addressed and placed in a desired state by the data on the bus such that each programmable bit produces a desired predetermined output based upon a given input. In particular, in the AND plane, each programmable bit is programmed to output; a "0" regardless of its input; a "1" regardless of its input; whatever is input, that is, a "0" input yields a "0" output and a "1" input yields a "1" output; or the inverse of whatever is input. In the OR plane, each programmable bit is programmed to output; a "0" regardless of its input; or whatever is input, that is a "0" input yields a "0" output and a "1" input yields a "1" output. In the third, i.e. output plane, each programmable bit is programmed to output whatever is input or the inverse of whatever is input.

Description Of The Drawings

Figure 1 is a block diagram showing the various elements of an SPLA as contemplated by the present invention.

5 Figure 2 is a logic level diagram showing a single programmable bit in an AND term.

Figure 3 is a block diagram showing a plurality of programmable bits as shown in Figure 2 combined to form a single AND term.

10 Figure 4 is a logic level diagram showing a single programmable bit of an OR term.

Figure 5 is a diagram showing a plurality of programmable bits as shown in Figure 4 combined to produce a single OR term.

Figure 6 is a logic level diagram showing a single programmable bit of an output term.

Detailed Description Of The Invention

A software programmable logic array ("SPLA") is disclosed for producing a plurality of predetermined outputs based upon the values of desired inputs, such that the output for a given input can be dynamically programmed without removing the SPLA from the circuit and environment in which it is being utilized. In the following description, numerous specific details are set forth such as specific word or term lengths, etc. to provide a thorough understanding of the present invention. However, it will be obvious to those skilled in the art that the present invention may be practiced without such specific details. In other instances, well known circuits have been shown in block diagram form in order not to obscure the present invention in unnecessary detail. For the most part, details concerning timing considerations and the like have been omitted inasmuch as such details are not necessary to obtain a complete understanding of the present invention and are within the skills of persons of ordinary skill in the relevant art.

Referring to Figure 1, SPLA 11 comprises an M bit wide AND plane 13 into which inputs 0 through L are latched by latches 15. Of course, the latching of input 0 through L occurs based upon a predetermined clocking signal (not shown). The outputs from the AND plane are then input to an N-bit wide OR plane 17. In this connection, M and N refer to the number of AND terms and OR terms respectively in AND plane 13 and OR plane 17. M and N may be any number greater than or equal to 1. Of course, as a practical matter, M and N will usually range between 8 and 32 bits wide. It should be understood that the number of programmable bits within AND plane 13 is $L \cdot M$ and the number of programmable bits in OR plane 17 is $M \cdot N$. The OR terms generated by OR plane 17 are then input to output polarity select plane 21 the output of which

in turn is latched by output latch and register 23 which simply stores the SPLA output until such time as the output is needed or can be accepted by the circuit in which the SPLA is implemented.

Also shown in Figure 1 are SPLA register decode circuitry 39, bus 33, SPLA I/O drives 35 and address latches 37, each of which will be described in conjunction with the description of the SPLA below. While such elements are necessary for the SPLA to function, they do not form part of the claimed invention.

Referring now to Figure 2 the construction of a single programmable bit 31 within AND plane 13 will now be described. Functionally, programmable bit 31 is programmed to produce an output which is: the same as its input; the input inverted; a "0" regardless of the input; or a "1" regardless of the input. This function is accomplished by programming the bit prior to applying one of inputs 0-L to the programmable bit. In particular, the programmable bits in the AND plane are programmed by (referring to Figure 1) placing an address and data on bus 33 wherein the address on the bus is the address of a particular AND term in which a programmable bit 31 is located and the data on the bus is a string of 0's and 1's depending upon whether a "0" or "1" is to be applied to a particular input select register, i.e. flip flop 43 or 45 within the programmable bit of the AND term being addressed. An address on bus 33, as determined by appropriate clocking signals (not shown) is latched by address latches 37. The latched address is then input to SPLA register decode circuit 39 which decodes the address and places appropriate signals on line 40a to allow the appropriate programmable bits in AND plane 13 to be programmed according to data placed on bus 33. In particular, after addressing the desired programmable bits, data is placed on bus 33 for setting

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the addressed programmable bits in a desired configuration. The data on bus 33 is then input to the addressed programmable bits in AND plane 13 by SPLA I/O driver 35 and the addressed programmable bits are then reconfigured as desired. In a similar manner, programmable bits within OR plane 17 or output polarity select plane 21 can be addressed and reconfigured as desired.

Bus 33, SPLA I/O driver 35, address latches 37 and SPLA register decode circuit 39 may be implemented according to well known design criteria for such circuits, the details of which will not be set forth herein as such details are well within the skill of those skilled in the relevant art and are highly dependent upon the processor being used to generate the data and address signals. If desired, particular programmable bits within the SPLA can be read by addressing the desired bits through SPLA register decode circuit 39 and setting RD/WR control line 38 to instruct decoder 39 and driver 35 that a read operation is taking place in which case the outputs from addressed programmable bits are placed on bus 33 for subsequent processing.

For example, assume a particular programmable bit 31 is programmed by placing a "1" on line 41 input to flip flop 43 and a "1" on line 42 input to flip flop 45. In this manner, outputs 47 and 49 from flip flops 43 and 45 respectively will cause one input of AND gates 53 and 57 to be a "1." Now, if a "0" is placed on input line 51, the inputs to AND gate 53 will be a "1" and a "0" and, therefore, one input to OR gate 59 will be a "0." However, since the "0" input on line 51 will be inverted by inverter 55, both inputs to AND gate 57 will be "1" and, therefore, the other input to OR gate 59 will be "1" and, the output of programmable bit 31 will therefore be a "1." Similarly, if the input on line 51 is a "1" the two inputs to AND

gate 53 will be "1" in which case one of the inputs to OR gate 59 will be "1" and its output will, therefore be a "1." Thus, in this configuration, the programmable bit 31 will output a "1" regardless of whether "0" or "1" is input.

5 If "0's" are input on lines 41 and 42 to flip flops 43 and 45 such that the outputs of the flip flops on lines 47 and 49 will be "0" then, regardless of the input on line 51, the outputs from AND gates 53 and 57 will always be "0," the inputs to OR gate 59 will also be "0" and the output of OR gate 59 will
10 therefore be "0."

In a similar fashion, if programmable bit 31 is programmed such that a "1" is placed on line 41 and a "0" is placed on line 42, the output of AND gate 53 will always be the same as the input on line 51 and the output of AND gate 57 will always be
15 "0." In this manner, the output from OR gate 59 will always be the same as the input on input line 51.

If the programmable bit 31 is programmed such that a "0" is placed on line 41 and a "1" is placed on line 42, then only the inverse of the input on line 51 (i.e. the output of inverter 55)
20 will be input to OR gate 59, the other input always being a "0." In this manner, the output of the programmable bit will always be the inverse of the input on line 51. The following table summarizes the possible configurations and outputs of a particular programmable bit 31:

25	Line 51 Input	Flip Flop 43 Q Output	Flip Flop 45 Q Output	OR Gate 59 Output
	0	0	0	0
	0	0	1	1
	0	1	0	0
	0	1	1	1
	1	0	0	0
	1	0	1	0
	1	1	0	1
30	1	1	1	1

Of course, each of the inputs 0 through L is input to a different programmable bit for each AND term. Referring now to Figure 3, by ANDing together the set of programmable bits for each of inputs 0 through L, a single AND term is produced as an output of AND gate 61. By applying inputs 0 through L to a second set of programmable bits 31 whose outputs are in turn ANDed together, a second AND term is produced. In a similar manner, third, fourth fifth, etc. through M AND terms can also be provided. Thus, in an M-bit wide AND plane, M AND terms are output.

Referring now to Figure 4, a single programmable bit 65 of OR plane 17 is shown. Of course, for each level of the OR plane, there is a single programmable bit 65 for each of 0 through M inputs which comprise the 0 through M AND terms from AND plane 13. Each programmable bit 65 comprises a flip flop 67 whose $\bar{Q}$ output is one input to an AND gate 69. The other input to AND gate 69 is one of the inputs 0 through M. By programming each programmable bit 65 such that the $\bar{Q}$ output of flip flop 67 is either a "1" or a "0" the output of each programmable bit 65 will be either the input on line 68, if the $\bar{Q}$ output is "1," or "0" if the $\bar{Q}$ output is "0."

Referring now to Figure 5, as was the case with the AND terms, by ORing together the outputs of the programmable bits 65 for each of the AND terms 0 through M through OR gate 70, a single OR term is output. By applying AND terms 0 through M to a second set of programmable bits 65 whose outputs are in turn ORed together, a second OR term is produced. In a similar manner, third, fourth and fifth, etc. through N OR terms can also be provided. Thus, in an N-bit wide OR plane N OR terms are output.

Each of the OR terms are then input to output polarity select plane 21 which comprises N programmable bits 71 as shown in Figure 6. Each of the programmable bits is preprogrammed such that its output is either the inputted OR term or the inputted OR term inverted. In particular, by programming programmable bits 71 by placing a "1" on line 73 which is input to flip flop 75 the Q output is set to "1" and input to AND gate 77 and the $\bar{Q}$ output is set to "0" and input to AND gate 79. Now, if the input OR term is a "1" on line 81, the output of AND gate 77 will be "1" and the output of AND gate 79 will be "0." Since a "1" input and a "0" are input to OR gate 85, the output term will be "1" or the same as the input term. Similarly, if a "0" is placed on line 81, then one input to each of AND gates 77 and 79 will be "0," the two inputs to OR gate 85 will be "0" and the output will therefore be a "0" or the same as the inputted OR term on line 81.

However, if flip flop 75 is reset by a "0" on line 73, the $\bar{Q}$ output into AND gate 79 will be a "1" and the Q output into AND gate 77 will be a "0." In this manner, whatever is input on line 81 will be inverted by inverter 83 and output from AND gate 79 which, when combined with the "0" output from AND gate 77 will result in OR gate 85 outputting the inverse of whatever is input on line 81.

Referring back to Figure 1, depending upon the manner in which the output polarity select plane 21 was programmed, each of the N OR terms output from OR plane 17 will be output from the output polarity select plane 21 as input or as the input inverted. Output latch and register 23 according to a signal on line 85 generated by decoder 39 will then latch each of the N OR

terms and retain the same until needed by the circuit in which the SPLA is implemented or replaced by a subsequent set of outputs.

In our co-pending U.K. patent application No. 8522863 there is described and claimed a software programmable logic array comprising a first plurality of programmable bit means, each having a single data input and two single control bit inputs, for selectively generating an output which is dynamically programmable by the application of logic level signals to said control inputs wherein said output is selectively:

"0" regardless of whether its input is "0" or "1";

"1" regardless of whether its input is "0" or "1";

"0" if its input is "0" and "1" if its input is "1"

and

"1" if its input is "0" and "0" if its input is "1",

wherein the outputs of each of said programmable bit means are ANDed together to produce a single AND term, said selectable output of each of said programmable bit means being determined by the value of said control inputs to said programmable bit means.

Also, in our co-pending U.K. patent application No. 8703963.2, there is described and claimed a software programmable logic array comprising:

AND plane means for receiving a plurality of inputs, said AND plane means including at least one set of first programmable bit means, each having a single data input and at least one control input, and each of which produces a predetermined and dynamically programmable output by the application of logic level signals to said

at least one control input, wherein the outputs of each set of said first programmable bit means are ANDed together to output at least one AND term; and

OR plane means coupled to said AND plane means such that said at least one AND term output of said AND plane means is input to said OR plane means, said OR plane means including at least one set of second programmable bit means, each having a single data input and at least one control input and each of which produces a predetermined and dynamically programmable output, wherein the output of each set of said second programmable bit means are ORed together to output at least one OR term;

wherein each of said programmable bit means of said AND plane means is for selectively generating an output which is:

"0" regardless of whether its input is "0" or "1";

"1" regardless of whether its input is "0" or "1";

"0" if its input is "0" and 1" if its input is "1"; and

"1" if its input is "0" and "0" if its input is "1", wherein said selectable output of each of said programmable bits means is determined by the value of at least one input to said programmable bit means.

CLAIMS

1. A software programmable logic array comprising a first plurality of programmable bit means, each having a separate corresponding data input and a separate corresponding control bit input, for selectively generating an output which is dynamically programmable by the application of logic level signals to each of said controls inputs, wherein each of said separate corresponding control bit inputs are programmed in parallel and each of said separate data inputs are received in parallel, wherein said output is selectively:

"0" if a "1" is input and "0" if a "0" is input; and

"1" if a "1" is input and "0" if a "0" is input, wherein the outputs of each of said programmable bit means are ORed together to produce a single OR term, said selectable output of each of said programmable bit means, being determined by the value of said corresponding control input to said programmable bit means.

2. The software programmable logic array defined by claim 1 wherein each of said programmable bit means comprises a flip flop whose $\overline{Q}$ output is input to an AND gate, the second input of said AND gate being a predetermined input, wherein the output of said AND gate is the output of said programmable bit means.

