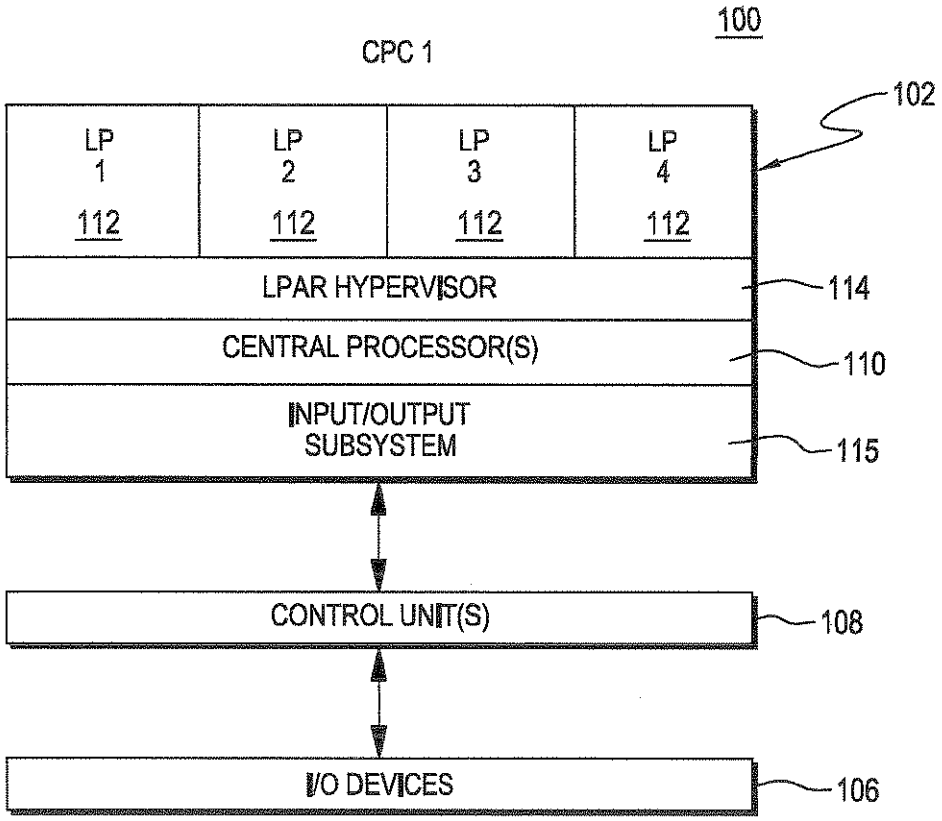
100
CPC 1
102
LP 1 112
LP 2 112
LP 3 112
LP 4 112
LPAR HYPERVISOR
114
CENTRAL PROCESSOR(S)
110
INPUT/OUTPUT SUBSYSTEM
115
CONTROL UNIT(S)
108
I/O DEVICES
106

FIG. 1

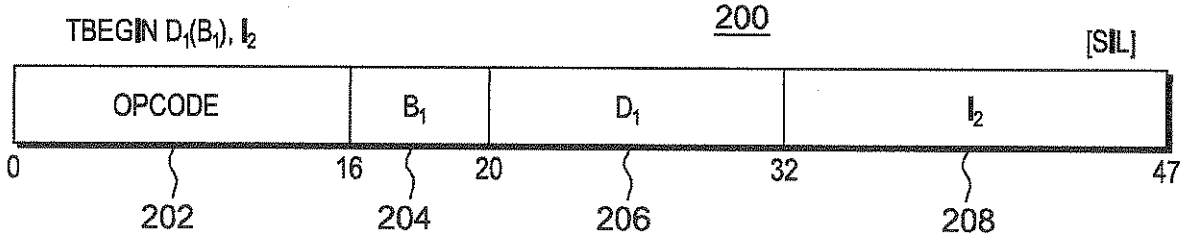

FIG. 2A

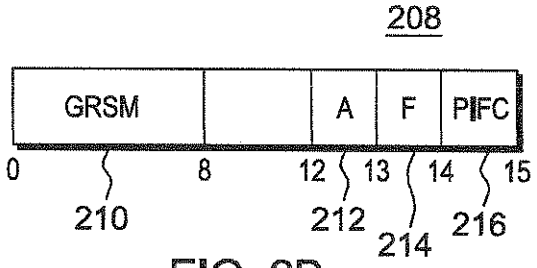

FIG. 2B

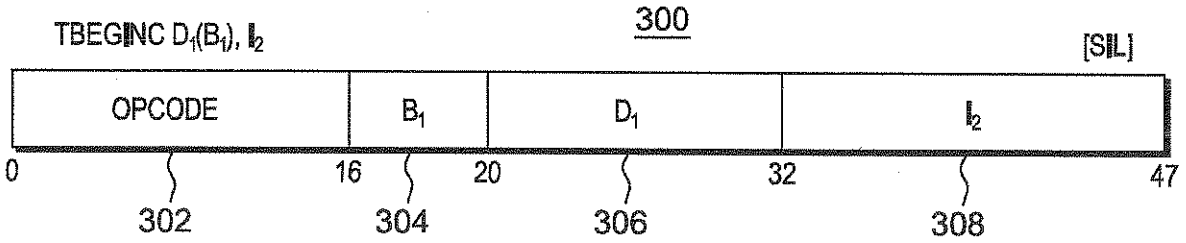

FIG. 3A

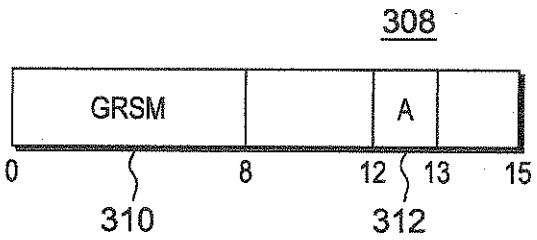

FIG. 3B

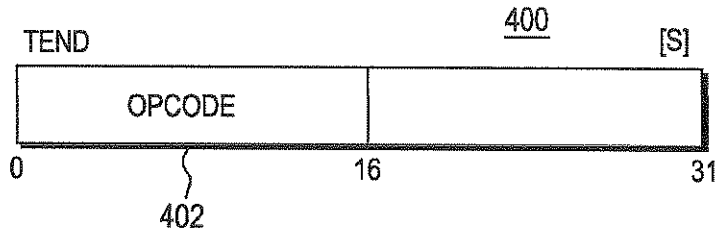
400
TEND
[S]
OPCODE
0
16
31
402

FIG. 4

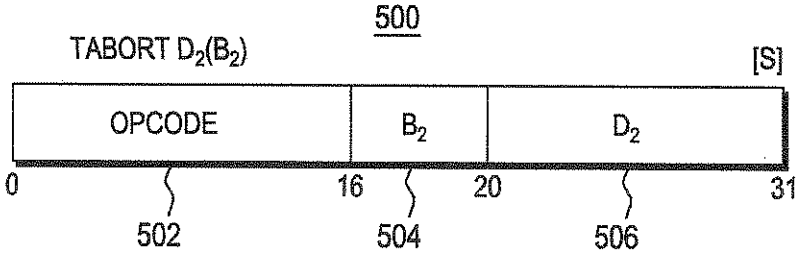
500
TABORT $D_2(B_2)$
[S]
OPCODE
B_2
D_2
0
16
20
31
502
504
506

FIG. 5

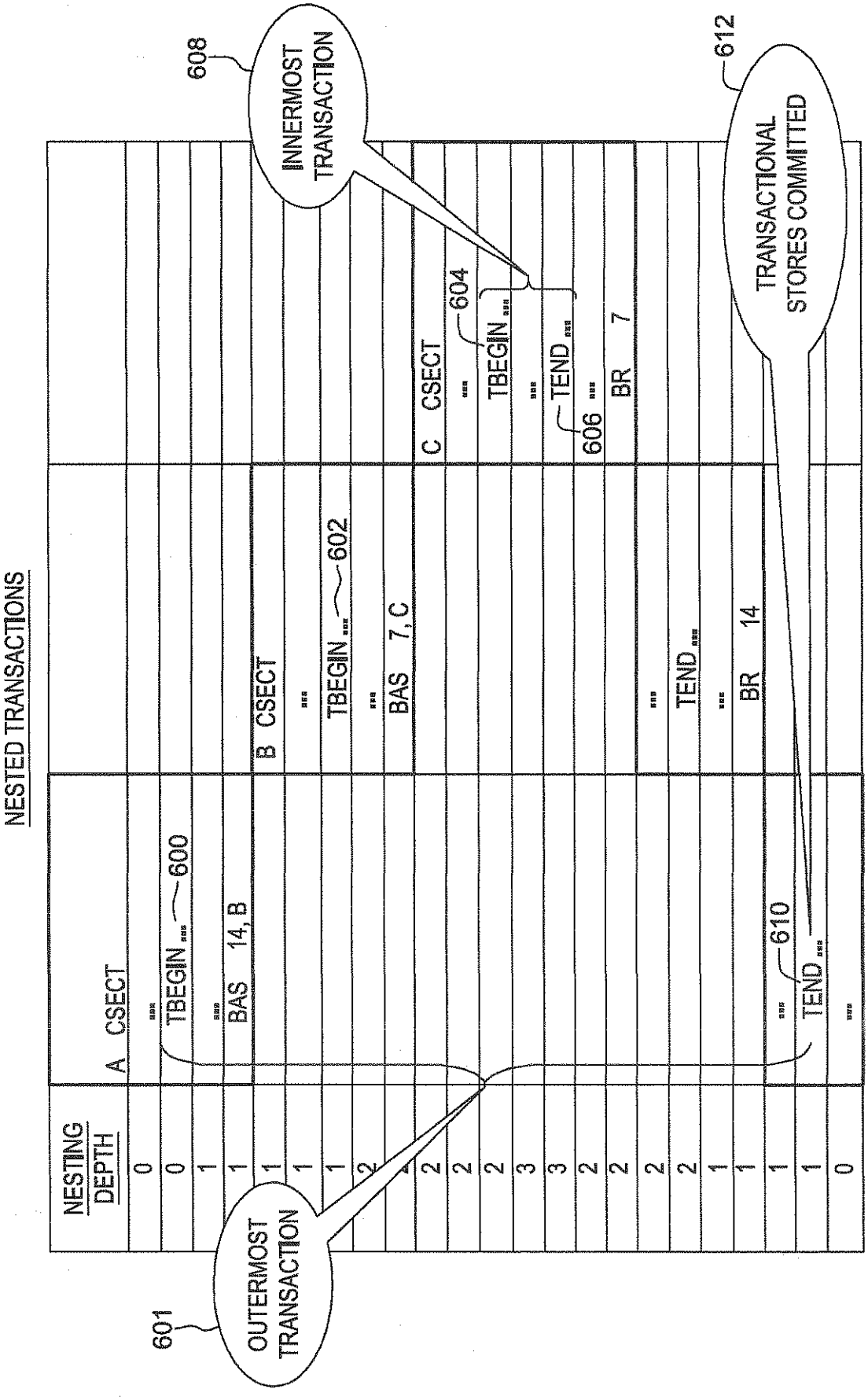
NESTED TRANSACTIONS
NESTING DEPTH
A CSECT
TBEGIN ... 600
BAS 14, B
B CSECT
TBEGIN ... 602
BAS 7, C
C CSECT
TBEGIN ... 604
TEND ... 606
BR 7
TEND ...
BR 14
TEND ... 610
601
OUTERMOST TRANSACTION
608
INNERMOST TRANSACTION
612
TRANSACTIONAL STORES COMMITTED

FIG. 6

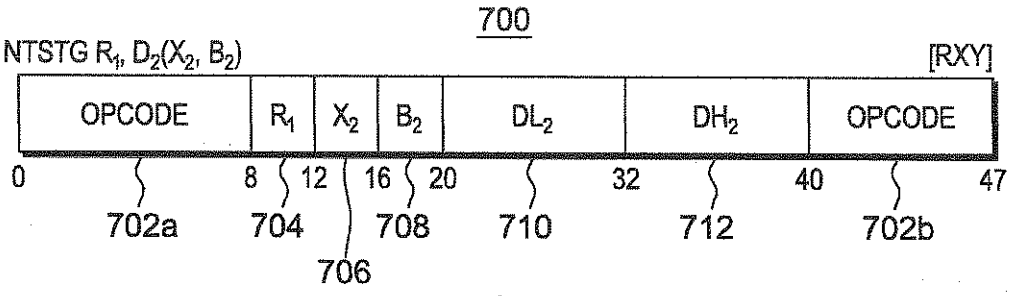
700
NTSTG R_1, $D_2(X_2, B_2)$
[RXY]
OPCODE
R_1
X_2
B_2
DL_2
DH_2
OPCODE
0
8
12
16
20
32
40
47
702a
704
706
708
710
712
702b

FIG. 7

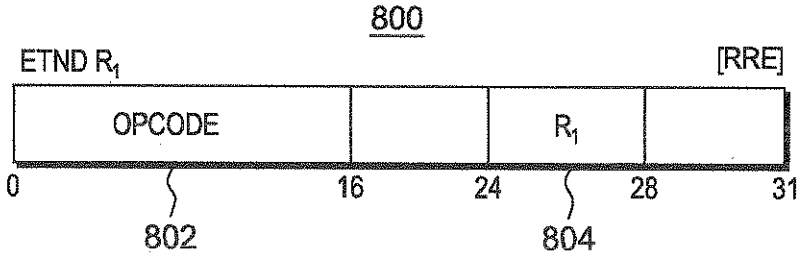
800
ETND R_1
[RRE]
OPCODE
R_1
0
16
24
28
31
802
804

FIG. 8

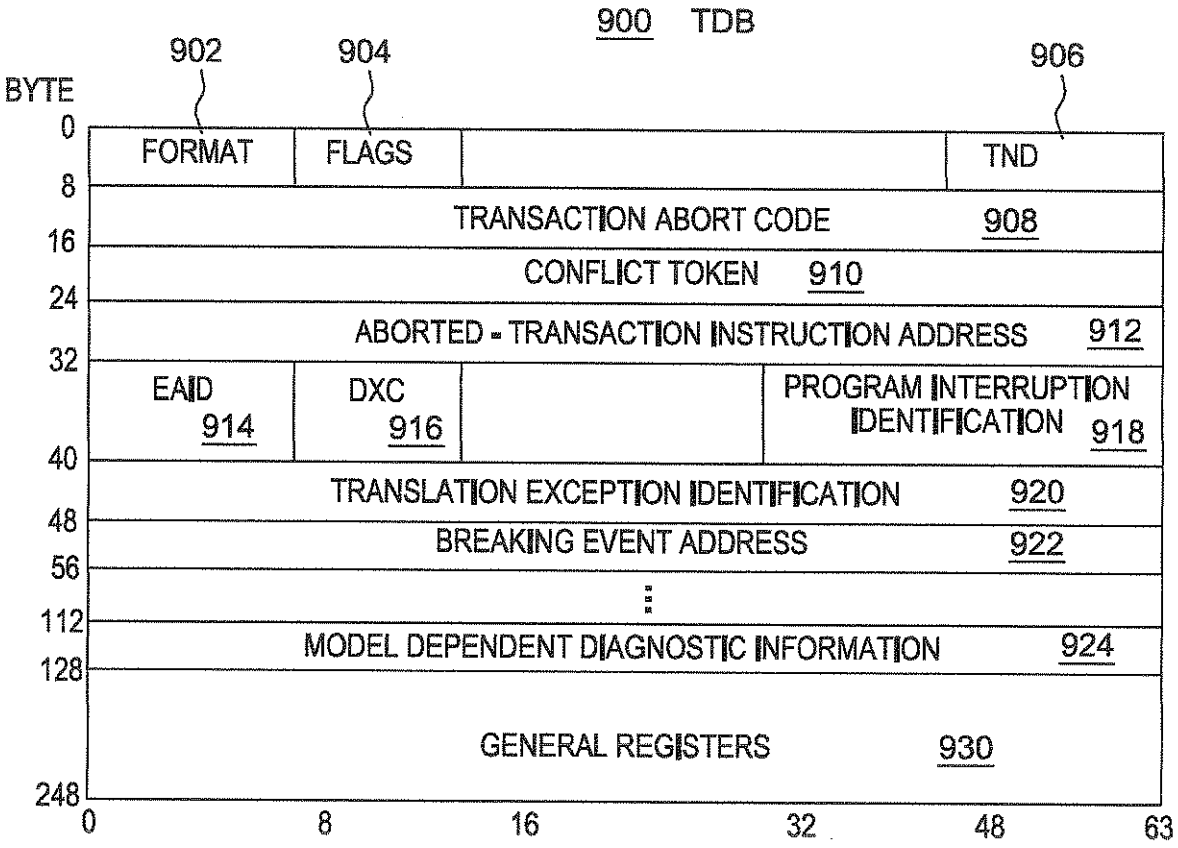
900 TDB
902
904
906
BYTE
0
8
16
24
32
40
48
56
112
128
248
FORMAT
FLAGS
TND
TRANSACTION ABORT CODE 908
CONFLICT TOKEN 910
ABORTED - TRANSACTION INSTRUCTION ADDRESS 912
EAID 914
DXC 916
PROGRAM INTERRUPTION IDENTIFICATION 918
TRANSLATION EXCEPTION IDENTIFICATION 920
BREAKING EVENT ADDRESS 922
MODEL DEPENDENT DIAGNOSTIC INFORMATION 924
GENERAL REGISTERS 930
0
8
16
32
48
63

FIG. 9

CODE	REASON FOR ABORT	CC SET
2	EXTERNAL INTERRUPTION	2
4	PROGRAM INTERRUPTION (UNFILTERED)	2 OR 3 +
5	MACHINE - CHECK INTERRUPTION	2
6	I/O INTERRUPTION	2
7	FETCH OVERFLOW	2 OR 3
8	STORE OVERFLOW	2 OR 3
9	FETCH CONFLICT	2
10	STORE CONFLICT	2
11	RESTRICTED INSTRUCTION	3
12	PROGRAM EXCEPTION CONDITION (FILTERED)	3
13	NESTING DEPTH EXCEEDED	3
14	CACHE FETCH RELATED	2 OR 3
15	CACHE STORE RELATED	2 OR 3
16	CACHE OTHER	2 OR 3
255	MISCELLANEOUS CONDITION	2 OR 3
>255	TABORT INSTRUCTION	2 OR 3
‡	CANNOT BE DETERMINED; NO TDB STORED	1

EXPLANATION:

\+ CONDITION CODE IS BASED ON INTERRUPTION CODE

‡ THIS SITUATION OCCURS WHEN A TRANSACTION ABORTS, BUT THE TDB HAS BECOME INACCESSIBLE SUBSEQUENT TO THE SUCCESSFUL EXECUTION OF THE OUTERMOST TBEGIN INSTRUCTION. NO TBEGIN SPECIFIED TDB IS STORED, AND THE CONDITION CODE IS SET TO 1.

FIG. 10

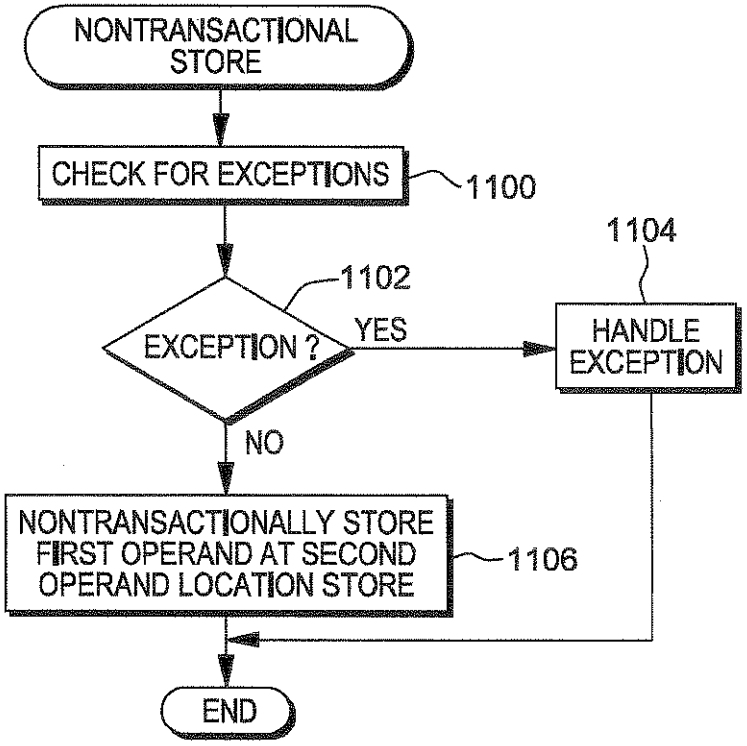

FIG. 11A

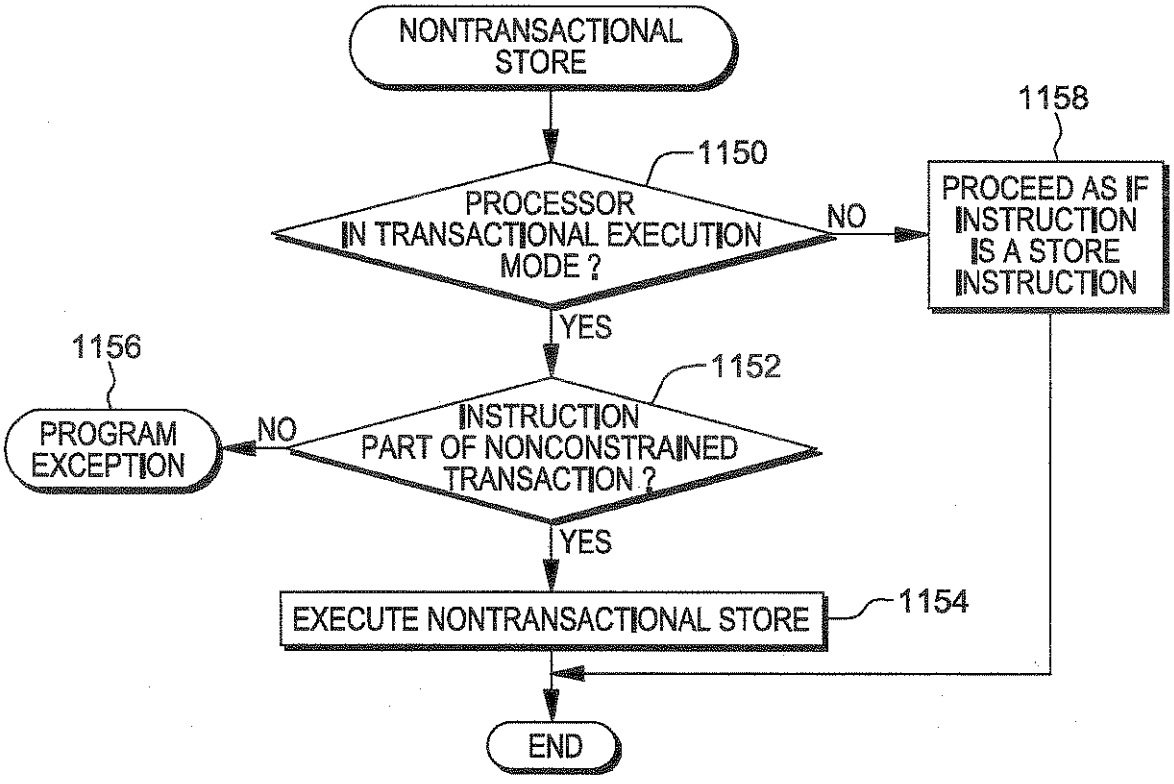

FIG. 11B

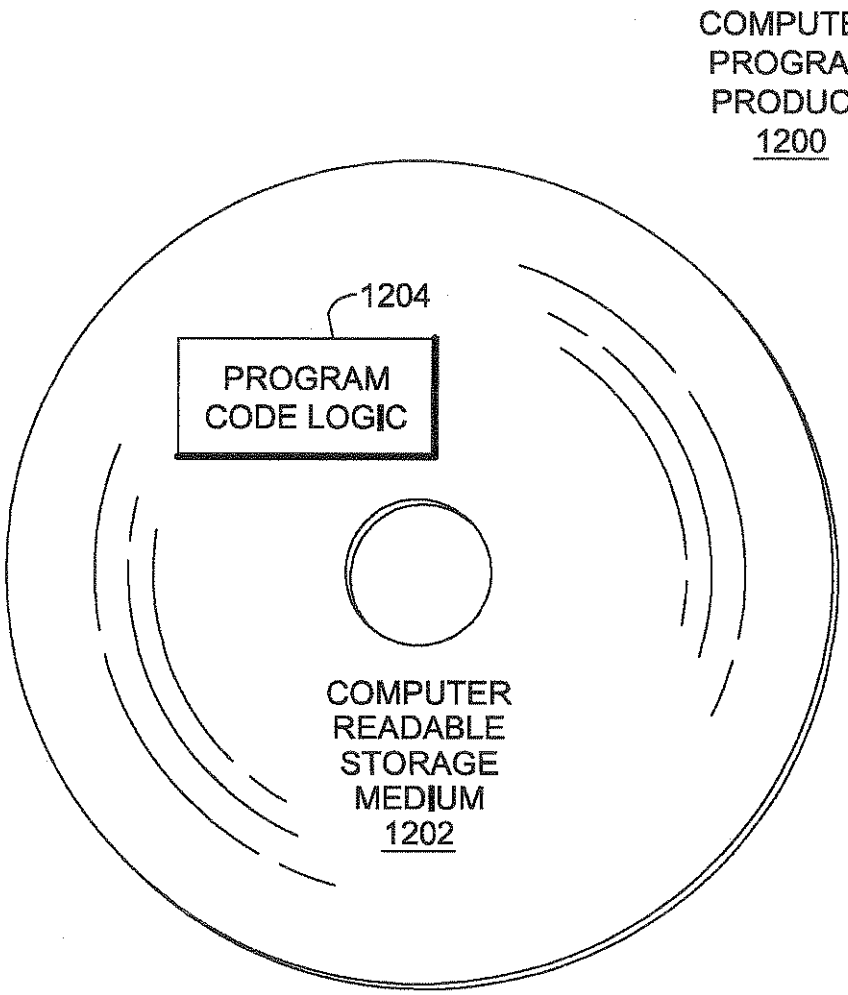
COMPUTER
PROGRAM
PRODUCT
1200
1204
PROGRAM
CODE LOGIC
COMPUTER
READABLE
STORAGE
MEDIUM
1202

FIG. 12

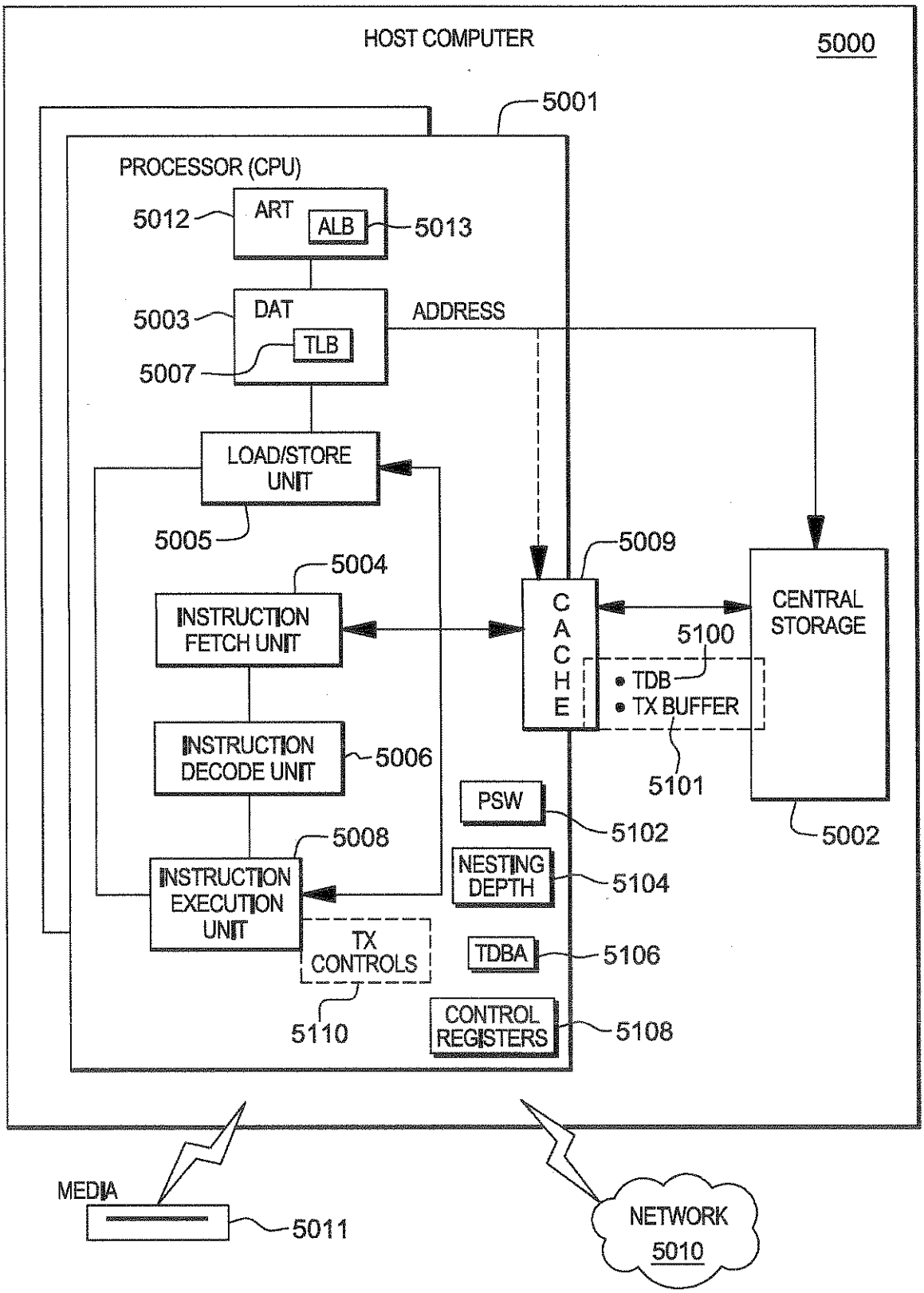
HOST COMPUTER
5000
5001
PROCESSOR (CPU)
5012
ART
ALB
5013
5003
DAT
ADDRESS
TLB
5007
LOAD/STORE UNIT
5005
5004
INSTRUCTION FETCH UNIT
5009
CACHE
5100
TDB
TX BUFFER
5101
CENTRAL STORAGE
5002
INSTRUCTION DECODE UNIT
5006
PSW
5102
5008
INSTRUCTION EXECUTION UNIT
NESTING DEPTH
5104
TX CONTROLS
TDBA
5106
5110
CONTROL REGISTERS
5108
MEDIA
5011
NETWORK
5010

FIG. 13

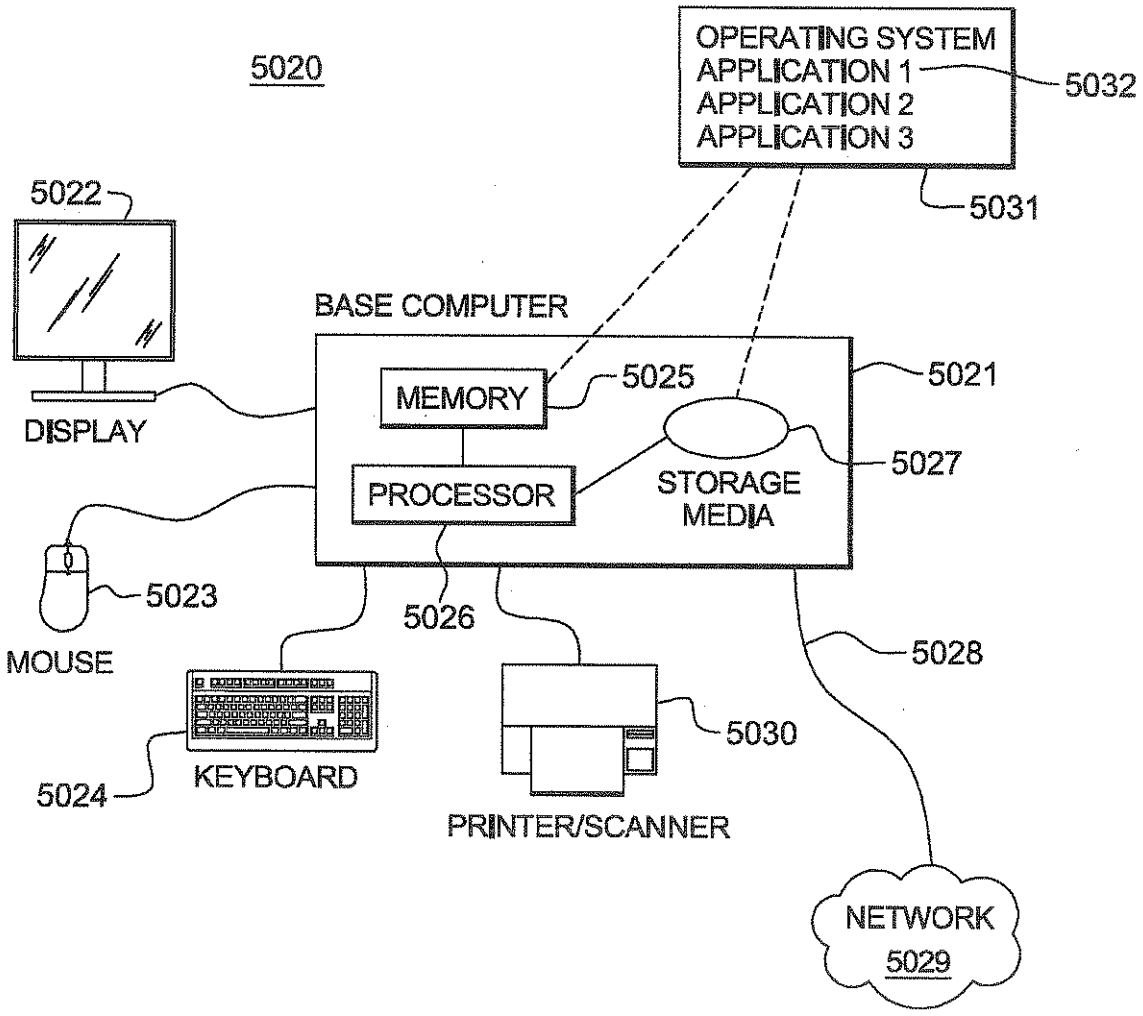
5020
OPERATING SYSTEM
APPLICATION 1
APPLICATION 2
APPLICATION 3
5032
5031
5022
BASE COMPUTER
MEMORY
5025
5021
5027
PROCESSOR
STORAGE MEDIA
DISPLAY
5023
MOUSE
5026
5028
5024
KEYBOARD
5030
PRINTER/SCANNER
NETWORK
5029

FIG. 14

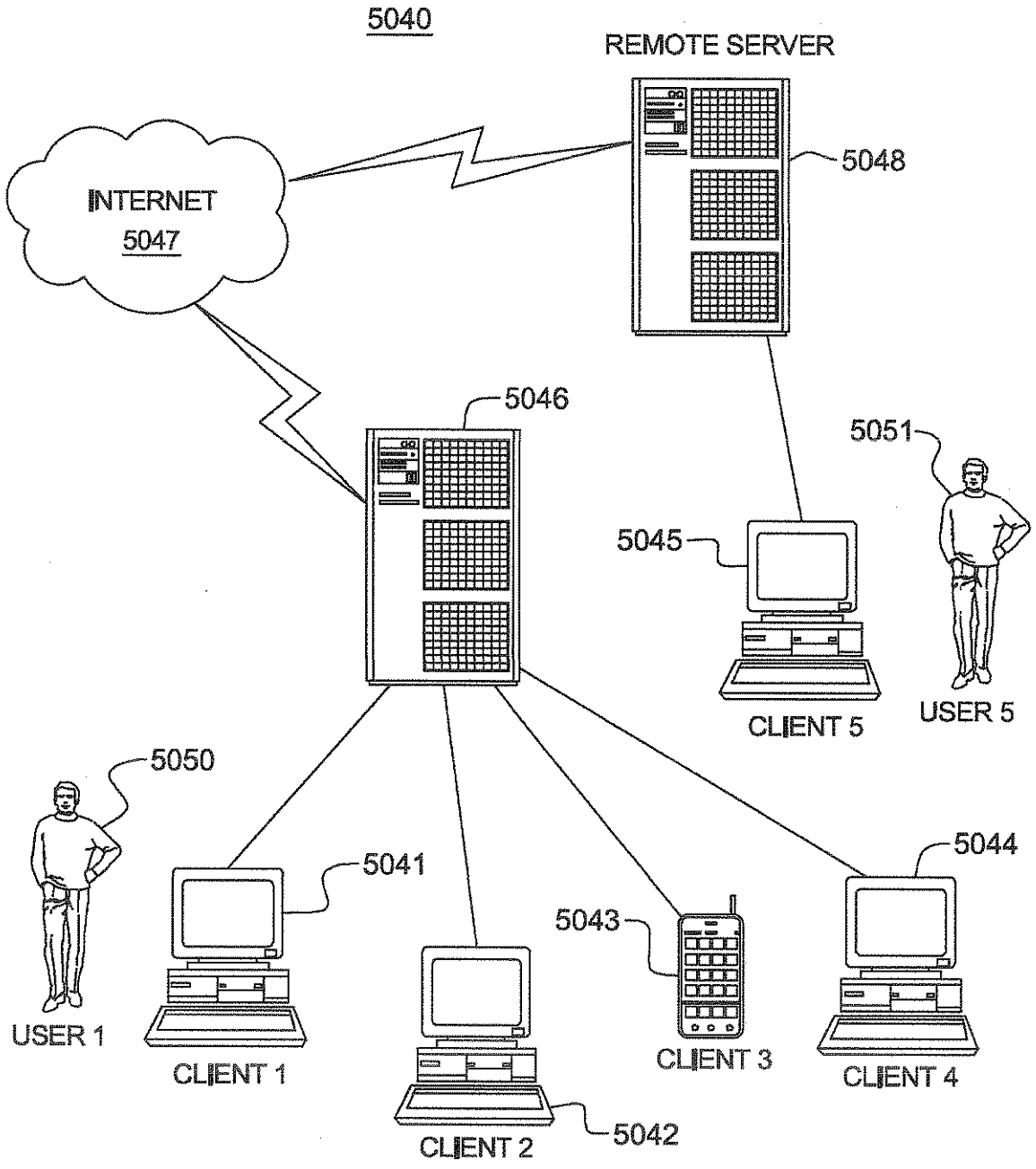
5040
REMOTE SERVER
5048
INTERNET
5047
5046
5051
5045
CLIENT 5
USER 5
5050
5041
5044
5043
USER 1
CLIENT 1
CLIENT 3
CLIENT 4
CLIENT 2
5042

FIG. 15

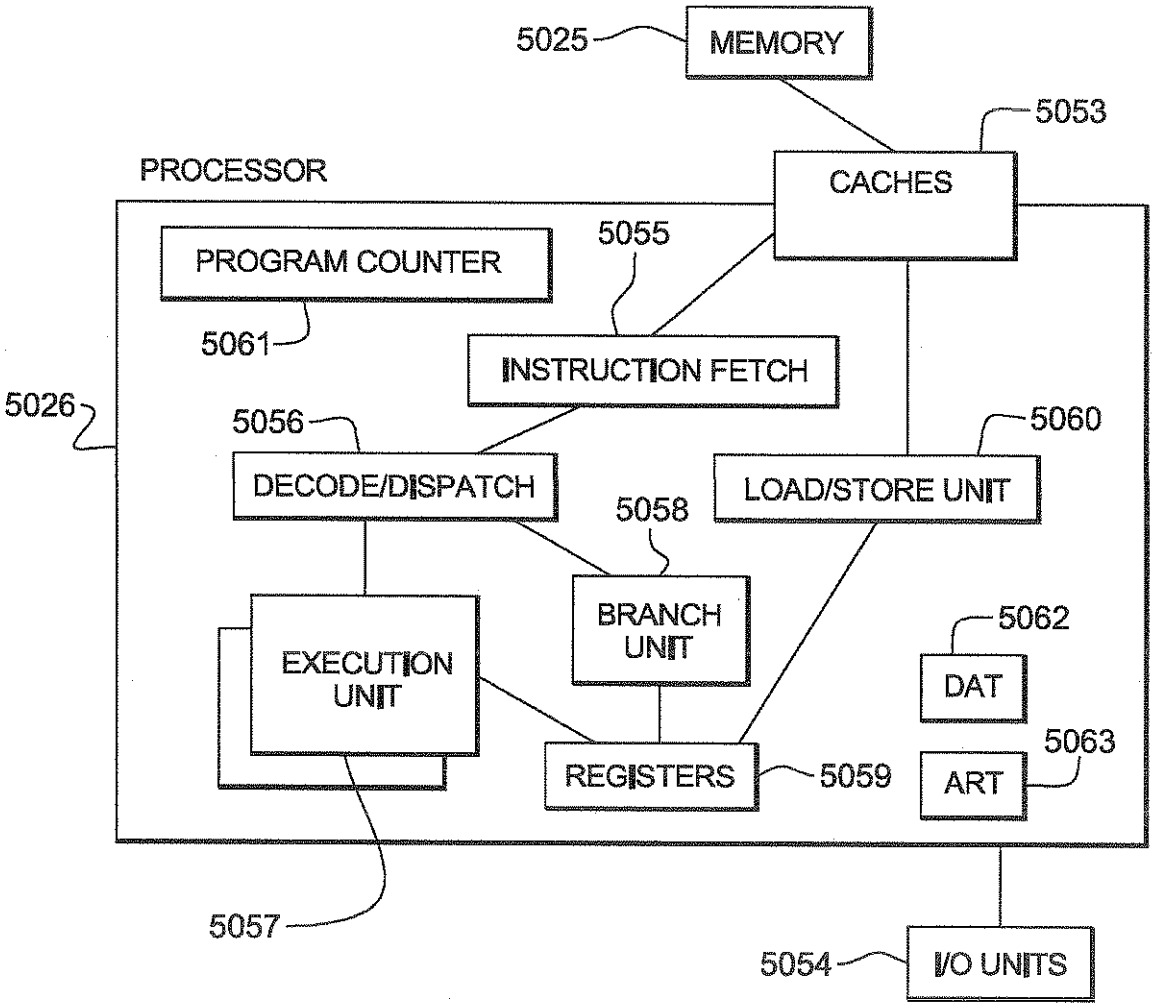
5025
MEMORY
5053
CACHES
PROCESSOR
PROGRAM COUNTER
5055
5061
INSTRUCTION FETCH
5026
5056
5060
DECODE/DISPATCH
LOAD/STORE UNIT
5058
BRANCH UNIT
5062
DAT
EXECUTION UNIT
5063
ART
REGISTERS
5059
5057
5054
I/O UNITS

FIG. 16

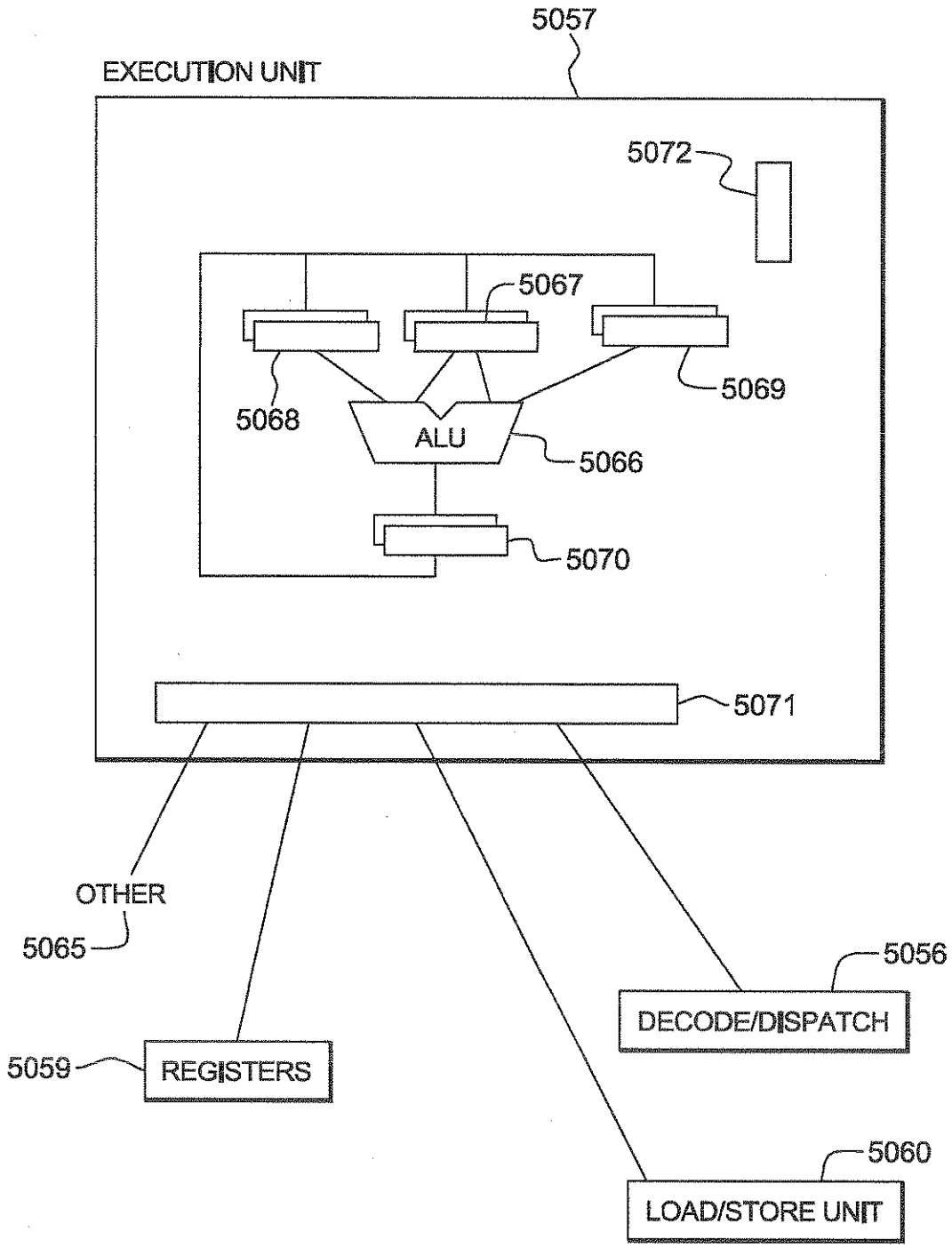
5057
EXECUTION UNIT
5072
5067
5068
5069
ALU
5066
5070
5071
OTHER
5065
5056
DECODE/DISPATCH
5059
REGISTERS
5060
LOAD/STORE UNIT

FIG. 17A

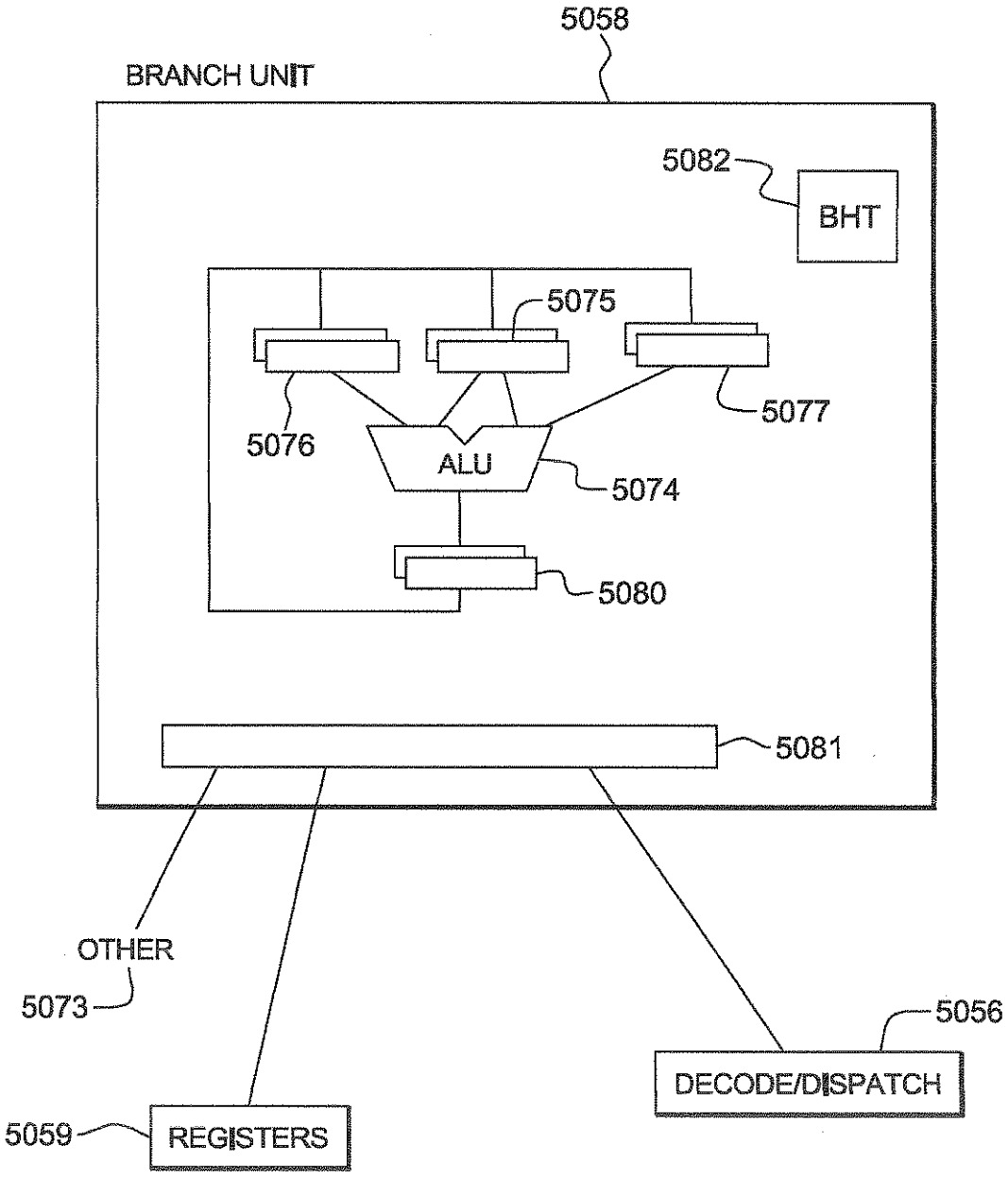
5058
BRANCH UNIT
5082
BHT
5075
5076
5077
ALU
5074
5080
5081
OTHER
5073
5056
DECODE/DISPATCH
5059
REGISTERS

FIG. 17B

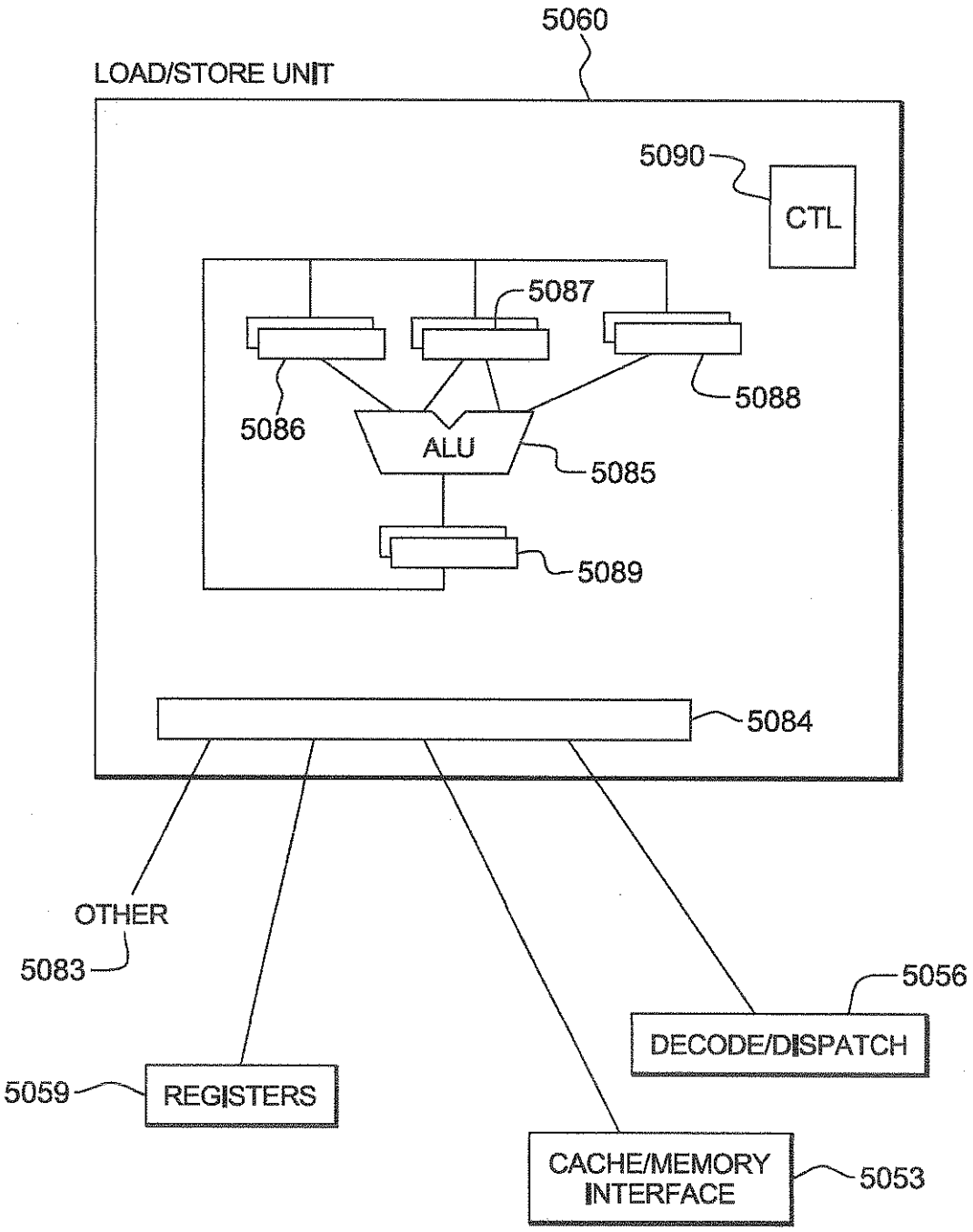
5060
LOAD/STORE UNIT
5090
CTL
5087
5086
5088
ALU
5085
5089
5084
OTHER
5083
5056
DECODE/DISPATCH
5059
REGISTERS
CACHE/MEMORY INTERFACE
5053

FIG. 17C

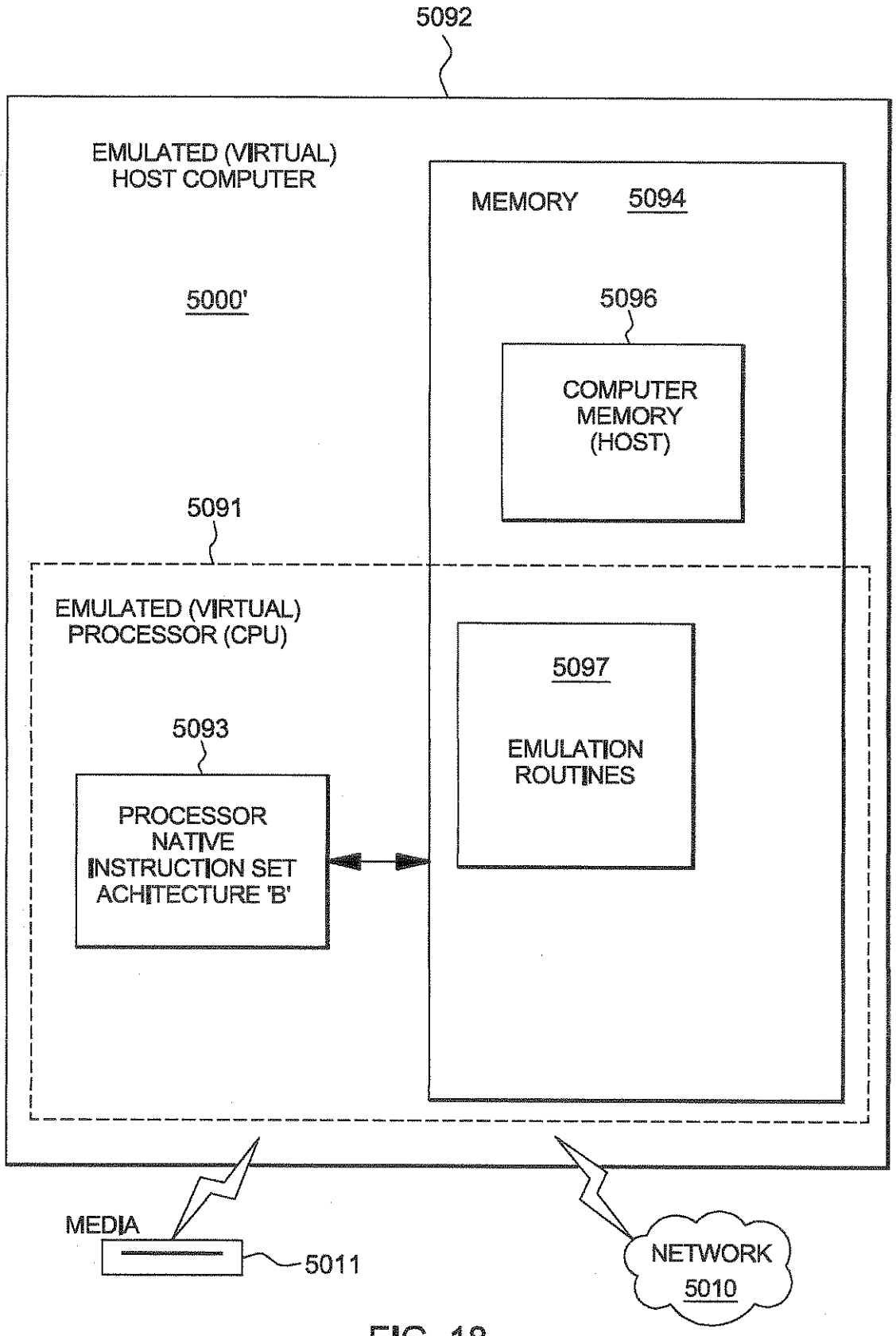
5092
EMULATED (VIRTUAL)
HOST COMPUTER
5000'
MEMORY 5094
5096
COMPUTER
MEMORY
(HOST)
5091
EMULATED (VIRTUAL)
PROCESSOR (CPU)
5097
EMULATION
ROUTINES
5093
PROCESSOR
NATIVE
INSTRUCTION SET
ACHITECTURE 'B'
MEDIA
5011
NETWORK
5010

FIG. 18