ABSTRACT

A semiconductor device includes an active region; an isolation region on a side surface of the active region; a gate trench intersecting the active region and extending into the isolation region; a gate structure in the gate trench; a first impurity region and a second impurity region in the active region on both sides of the gate structure and spaced apart from each other; a bit line structure including a line portion intersecting the gate structure and a plug portion below the line portion and electrically connected to the first impurity region; and an insulating structure on a side surface of the plug portion. The insulating structure includes a spacer including a first material; an insulating pattern between the plug portion and the spacer and including a second material; and an insulating liner covering a side surface and a bottom surface of the insulating pattern and including a third material.

FIG. 8