FIG. 3

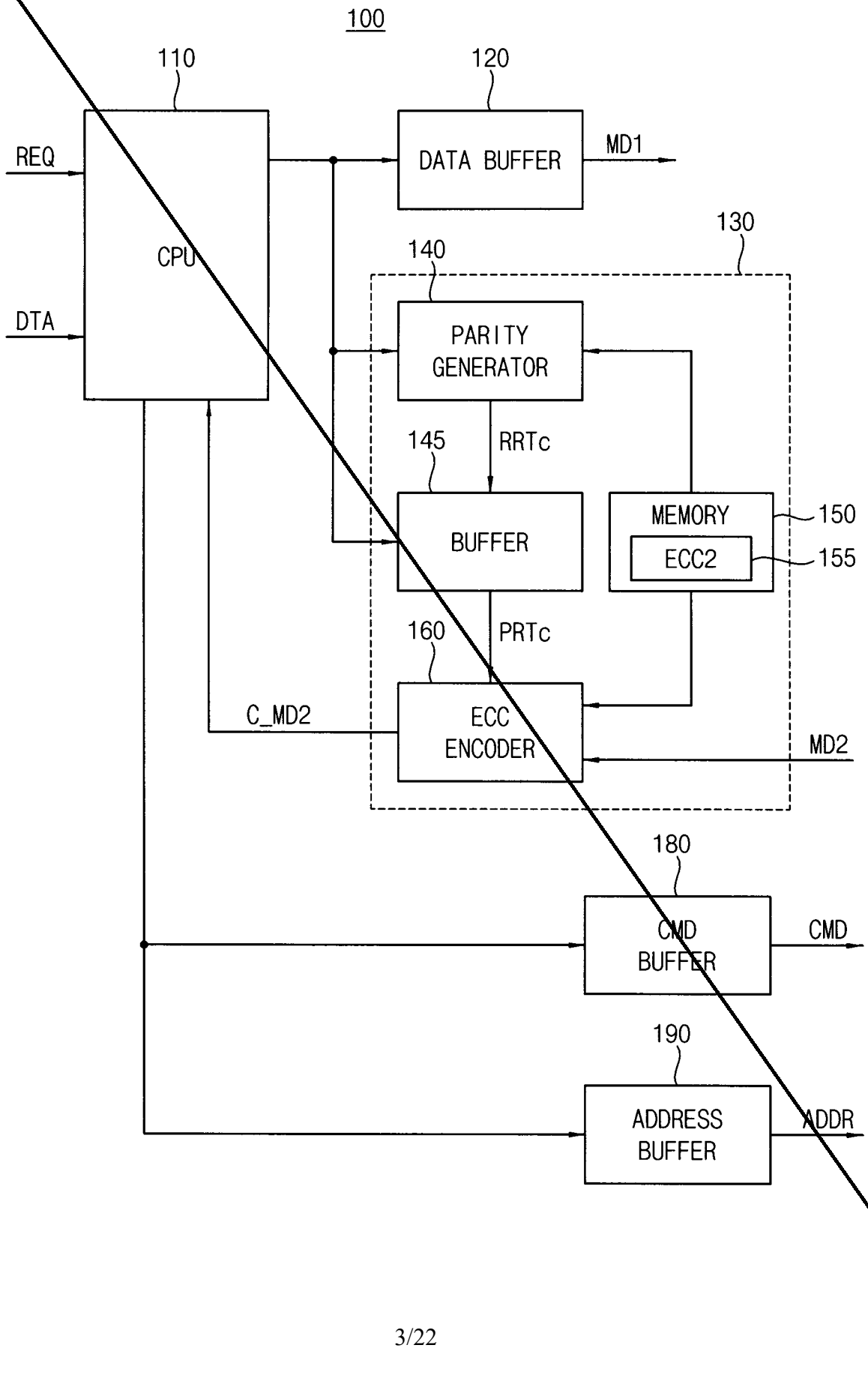

100
110
120
REQ
CPU
DATA BUFFER
MD1
130
140
DTA
PARITY GENERATOR
145
RRTc
BUFFER
MEMORY
150
ECC2
155
160
PRTc
C_MD2
ECC ENCODER
MD2
180
CMD BUFFER
CMD
190
ADDRESS BUFFER
ADDR

FIG. 3

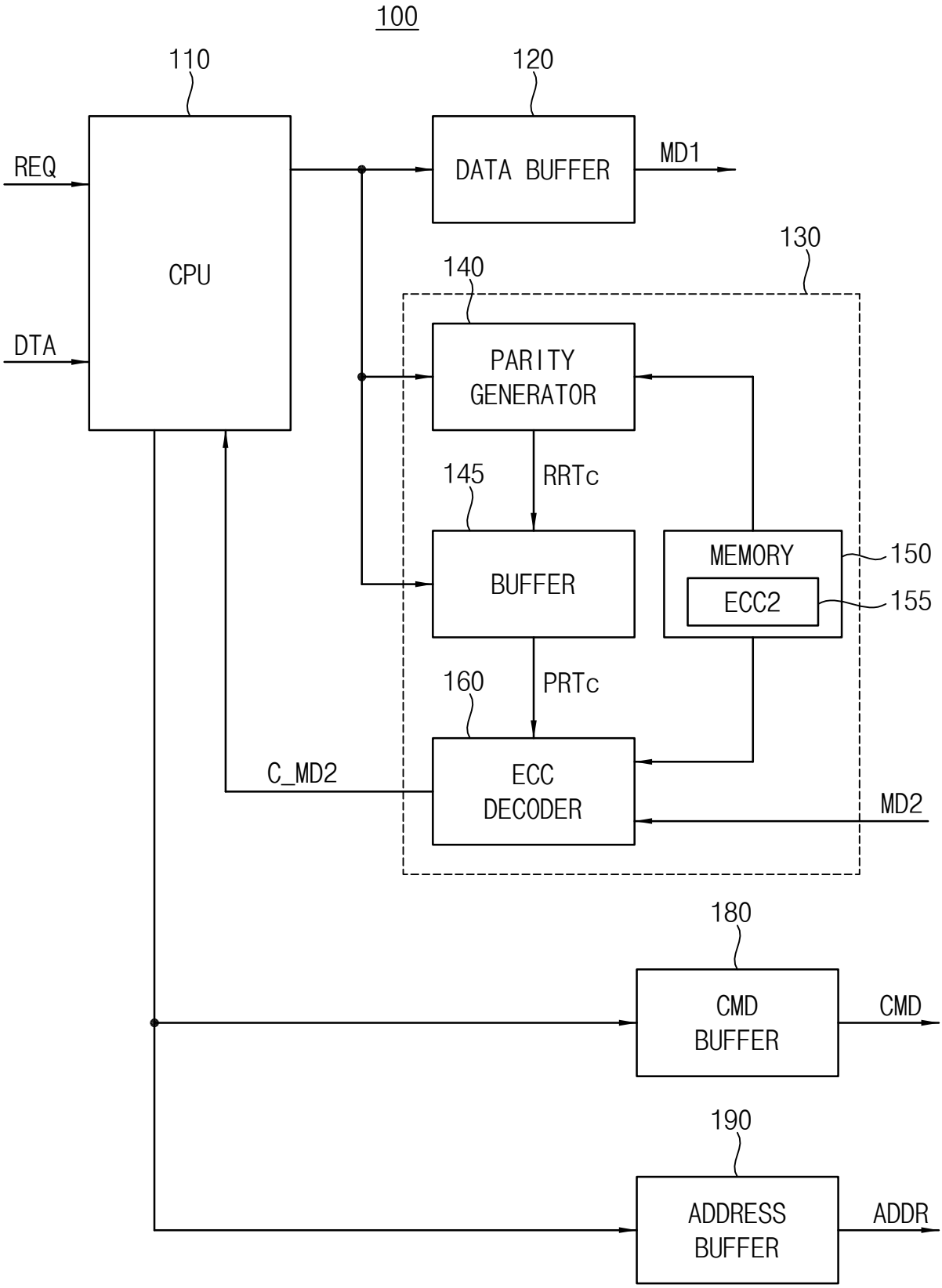

100
110
120
REQ
CPU
DTA
DATA BUFFER
MD1
130
140
PARITY
GENERATOR
145
RRTc
BUFFER
MEMORY
150
ECC2
155
160
PRTc
C_MD2
ECC
DECODER
MD2
180
CMD
BUFFER
CMD
190
ADDRESS
BUFFER
ADDR

FIG. 7

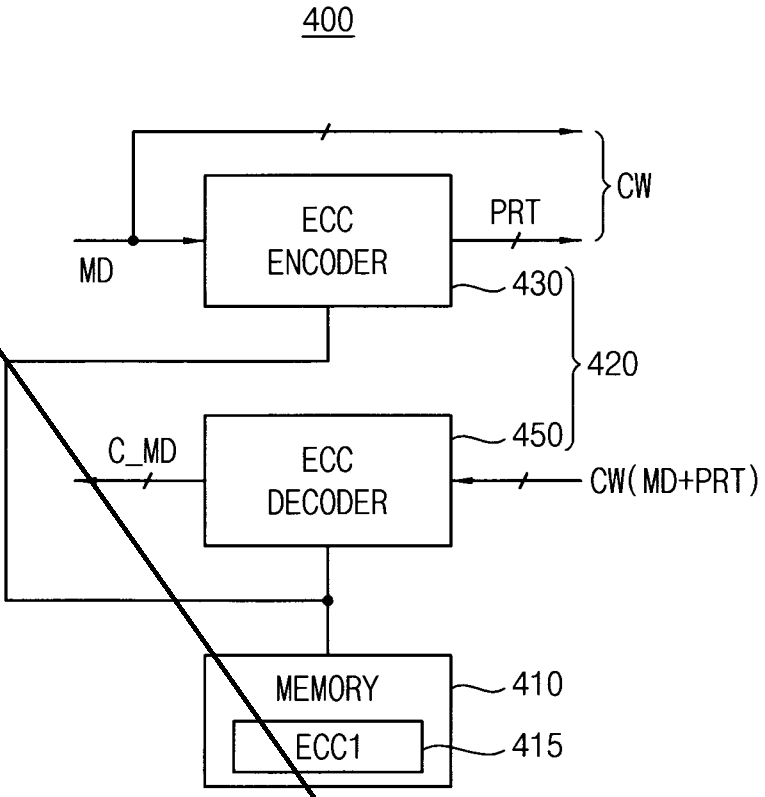

400
CW
ECC
ENCODER
PRT
MD
430
420
450
C_MD
ECC
DECODER
CW(MD+PRT)
MEMORY
410
ECC1
415

FIG. 8

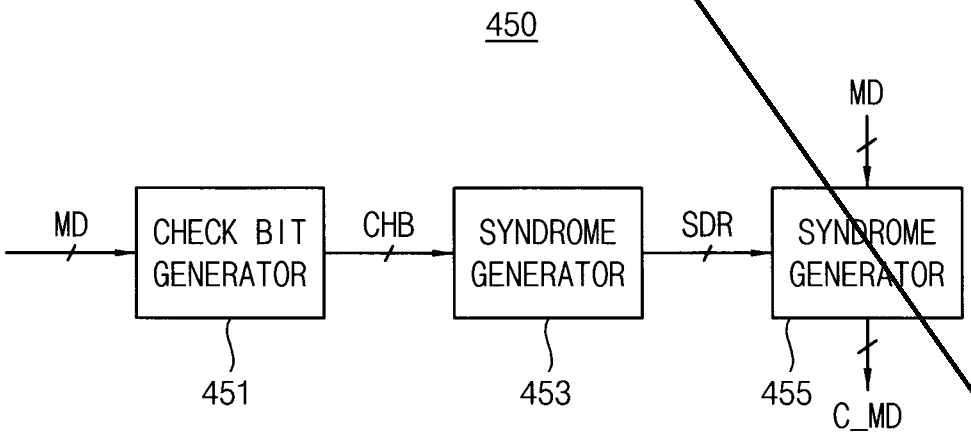

450
MD
MD
CHECK BIT
GENERATOR
CHB
SYNDROME
GENERATOR
SDR
SYNDROME
GENERATOR
451
453
455
C_MD

FIG. 7

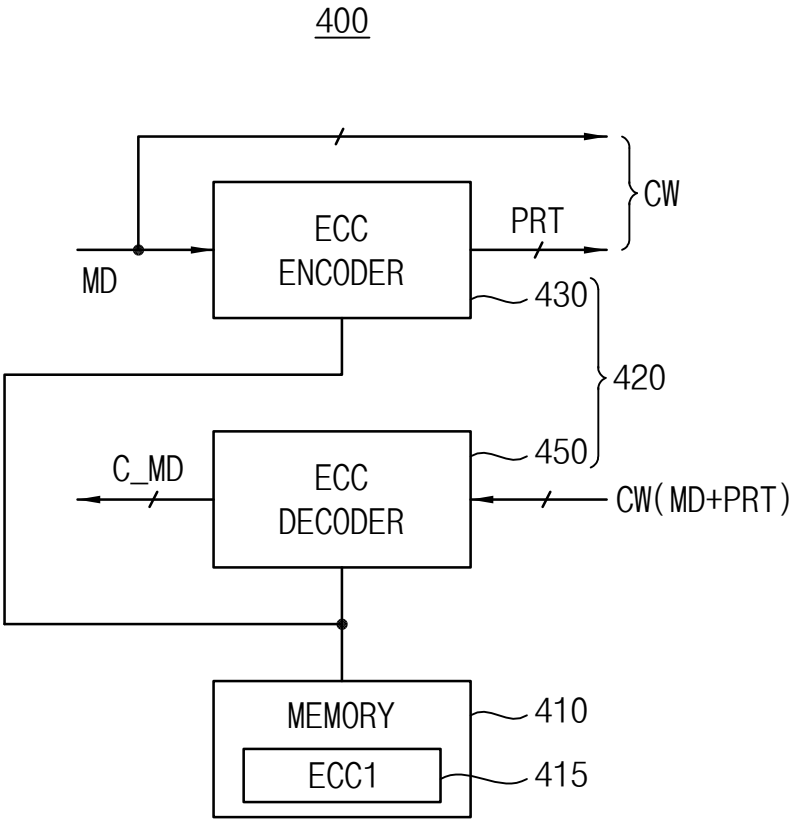
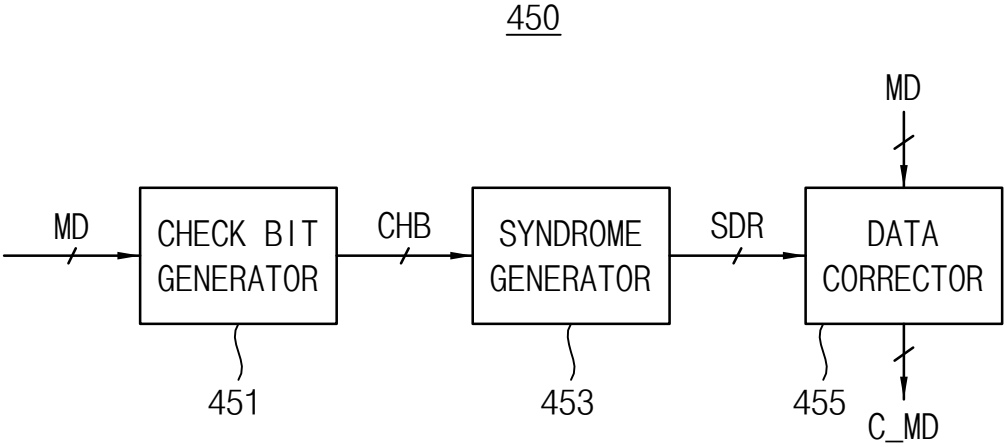

400
CW
ECC
ENCODER
PRT
MD
430
420
450
C_MD
ECC
DECODER
CW(MD+PRT)
MEMORY
410
ECC1
415

FIG. 8


450
MD
MD
CHECK BIT
GENERATOR
CHB
SYNDROME
GENERATOR
SDR
DATA
CORRECTOR
451
453
455
C_MD