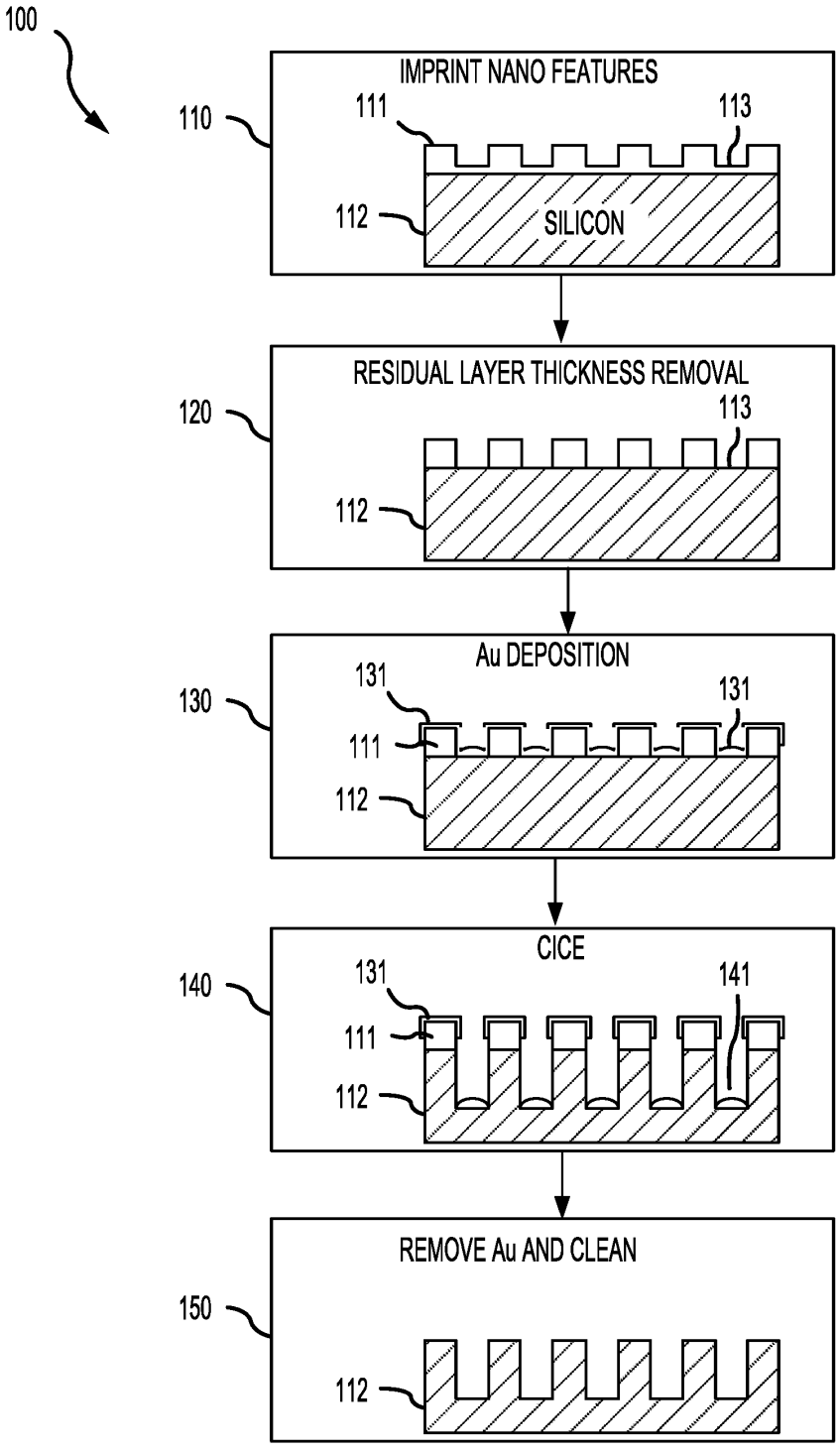
100
IMPRINT NANO FEATURES
110
111
113
112
SILICON
RESIDUAL LAYER THICKNESS REMOVAL
120
113
112
Au DEPOSITION
130
131
131
111
112
CICE
140
131
141
111
112
REMOVE Au AND CLEAN
150
112

FIG.1A

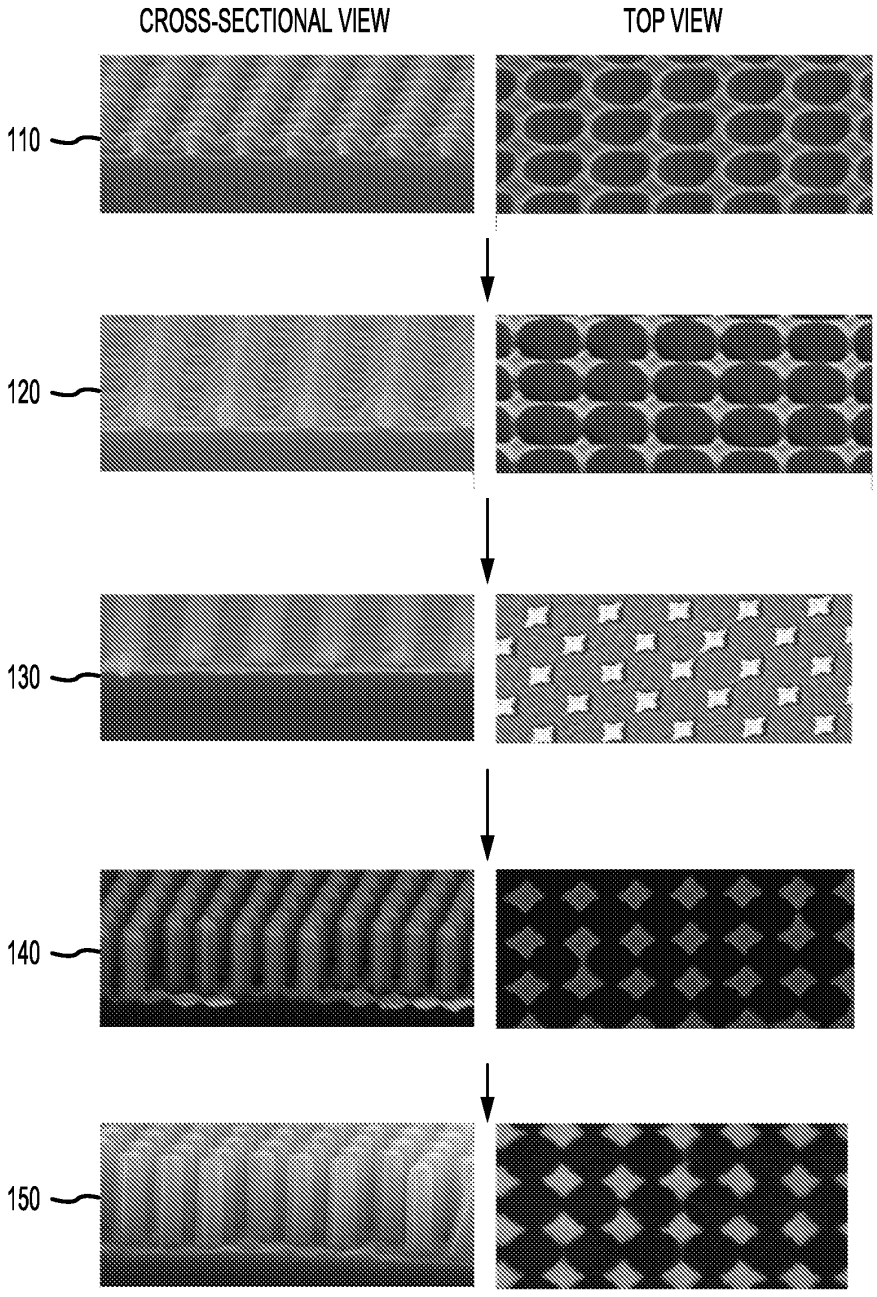


FIG.1B

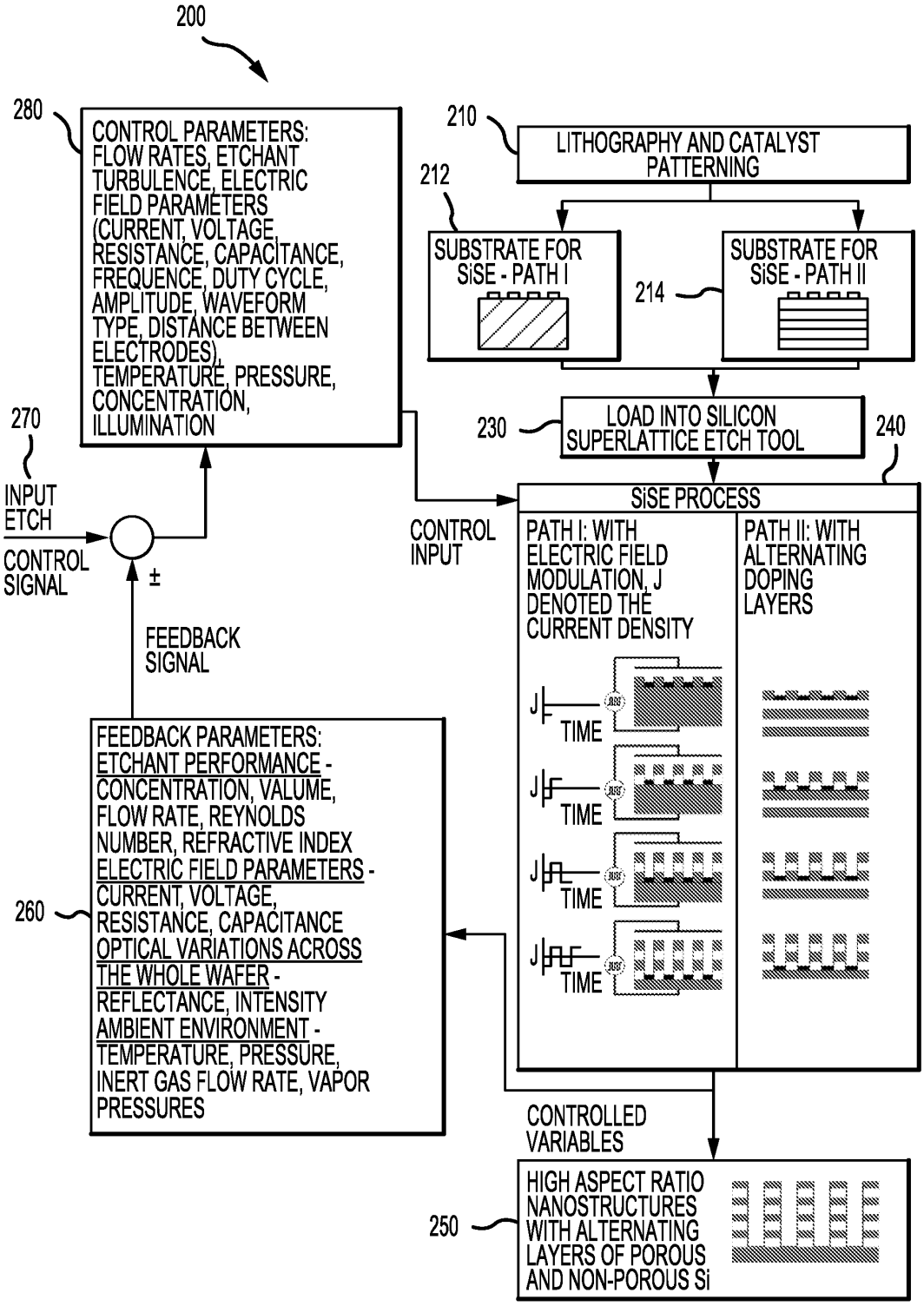
200
280
CONTROL PARAMETERS: FLOW RATES, ETCHANT TURBULENCE, ELECTRIC FIELD PARAMETERS (CURRENT, VOLTAGE, RESISTANCE, CAPACITANCE, FREQUENCE, DUTY CYCLE, AMPLITUDE, WAVEFORM TYPE, DISTANCE BETWEEN ELECTRODES), TEMPERATURE, PRESSURE, CONCENTRATION, ILLUMINATION
210
LITHOGRAPHY AND CATALYST PATTERNING
212
SUBSTRATE FOR SiSE - PATH I
214
SUBSTRATE FOR SiSE - PATH II
230
LOAD INTO SILICON SUPERLATTICE ETCH TOOL
240
SiSE PROCESS
PATH I: WITH ELECTRIC FIELD MODULATION, J DENOTED THE CURRENT DENSITY
PATH II: WITH ALTERNATING DOPING LAYERS
J
TIME
270
INPUT ETCH CONTROL SIGNAL
±
CONTROL INPUT
FEEDBACK SIGNAL
260
FEEDBACK PARAMETERS: ETCHANT PERFORMANCE - CONCENTRATION, VALUME, FLOW RATE, REYNOLDS NUMBER, REFRACTIVE INDEX ELECTRIC FIELD PARAMETERS - CURRENT, VOLTAGE, RESISTANCE, CAPACITANCE OPTICAL VARIATIONS ACROSS THE WHOLE WAFER - REFLECTANCE, INTENSITY AMBIENT ENVIRONMENT - TEMPERATURE, PRESSURE, INERT GAS FLOW RATE, VAPOR PRESSURES
CONTROLLED VARIABLES
250
HIGH ASPECT RATIO NANOSTRUCTURES WITH ALTERNATING LAYERS OF POROUS AND NON-POROUS Si

FIG.2

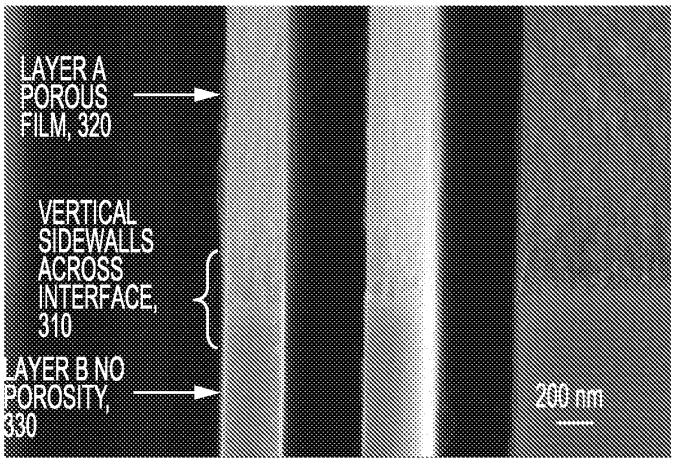
LAYER A POROUS FILM, 320
VERTICAL SIDEWALLS ACROSS INTERFACE, 310
LAYER B NO POROSITY, 330
200 nm

FIG.3A

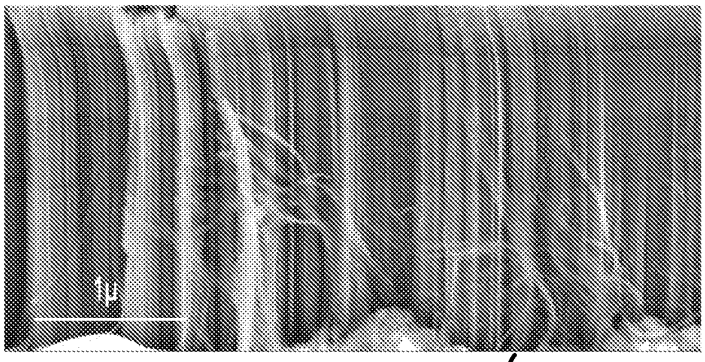
1u
340

FIG.3B

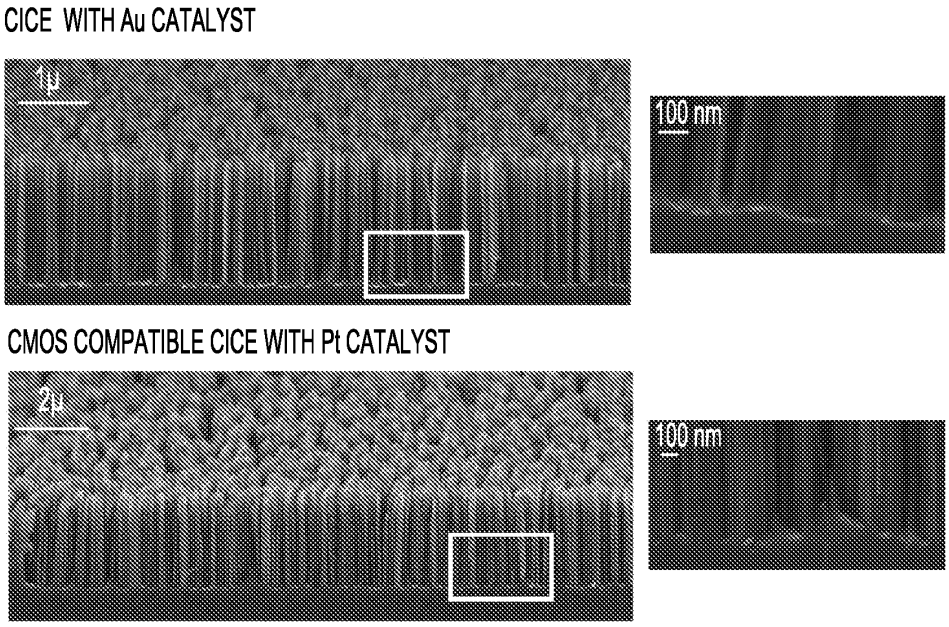
CICE WITH Au CATALYST
1μ
100 nm
CMOS COMPATIBLE CICE WITH Pt CATALYST
2μ
100 nm

FIG.4

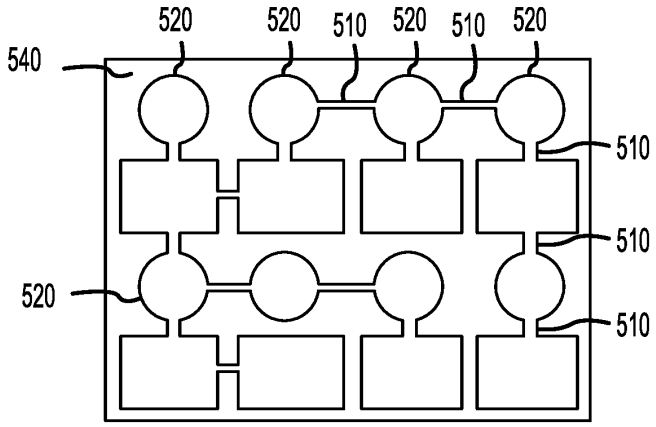
520
520
510
520
510
520
540
510
510
520
510

FIG.5A

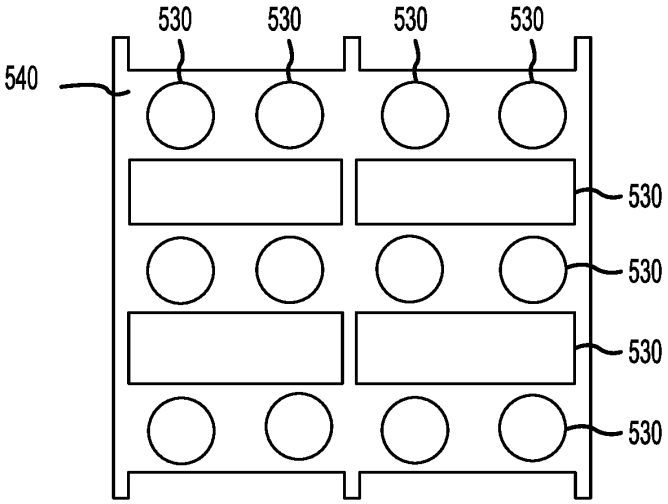
530
530
530
530
540
530
530
530
530

FIG.5B

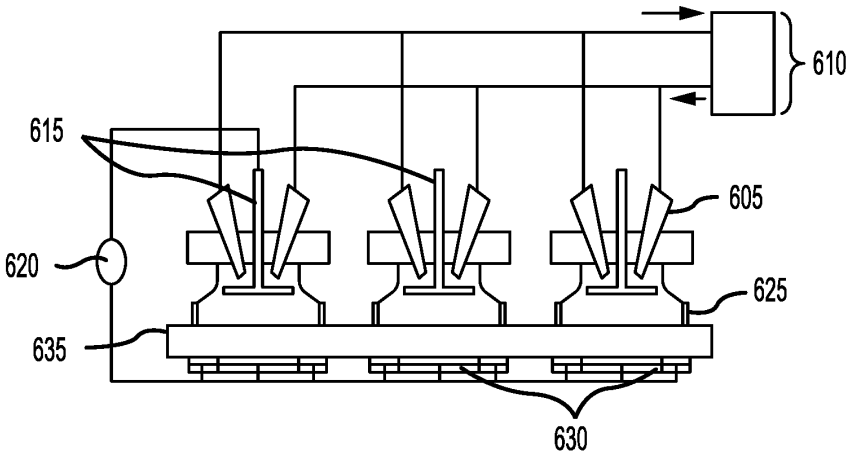


FIG.6A

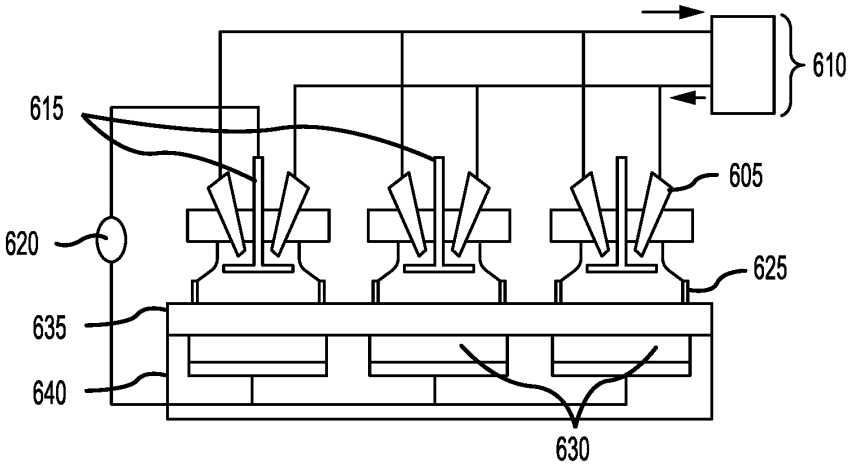


FIG.6B

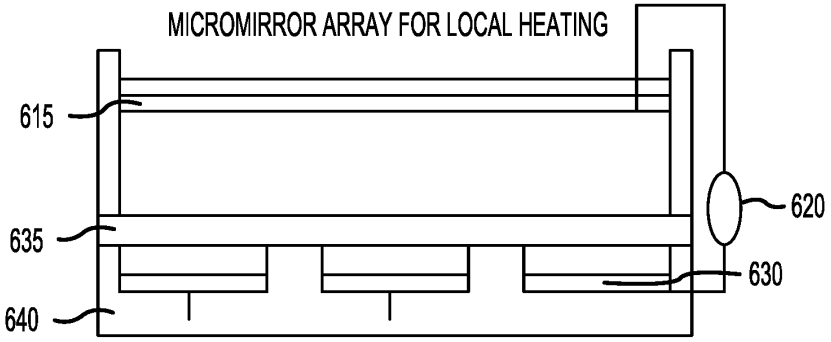
MICROMIRROR ARRAY FOR LOCAL HEATING
615
620
635
630
640

FIG.6C

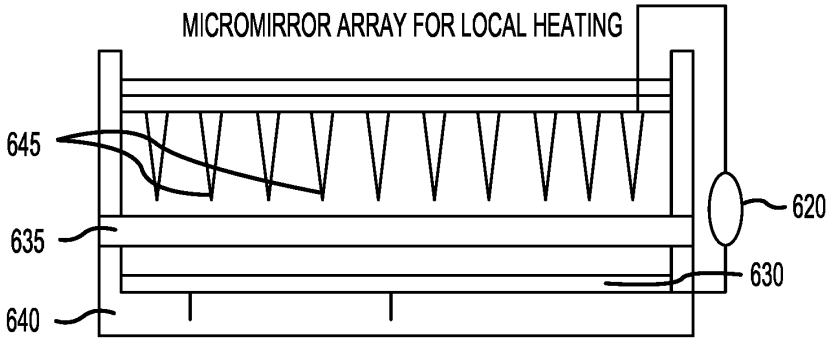
MICROMIRROR ARRAY FOR LOCAL HEATING
645
620
635
630
640

FIG.6D

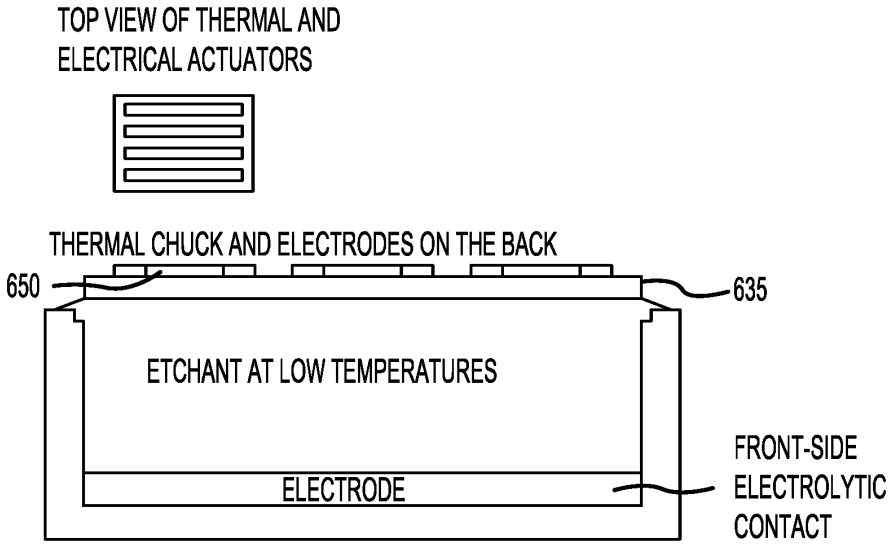
TOP VIEW OF THERMAL AND
ELECTRICAL ACTUATORS
THERMAL CHUCK AND ELECTRODES ON THE BACK
650
635
ETCHANT AT LOW TEMPERATURES
ELECTRODE
FRONT-SIDE
ELECTROLYTIC
CONTACT

FIG.6E

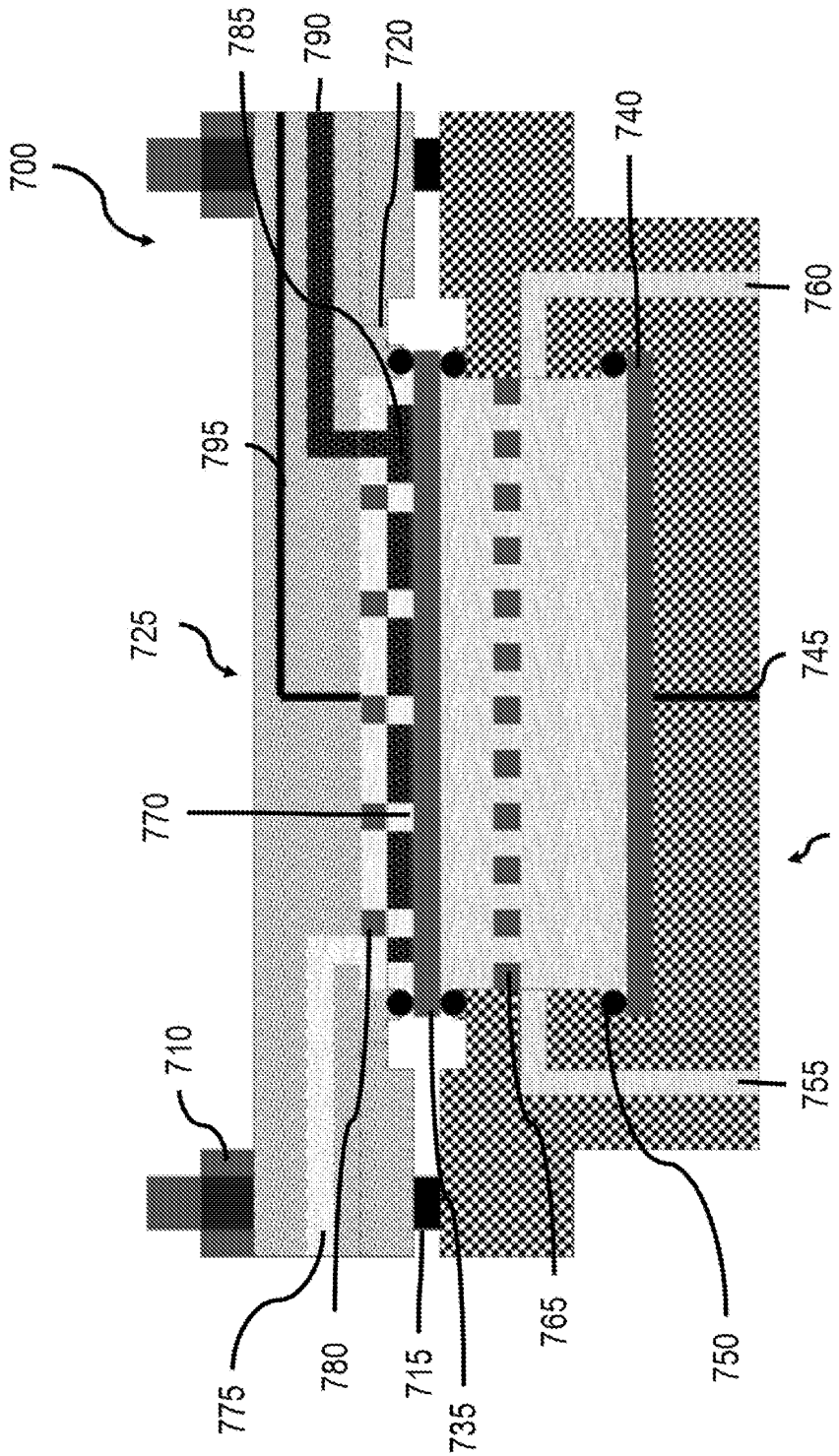
700
785
790
720
740
760
795
725
745
770
730
710
755
775
780
715
735
765
750

FIG. 7A

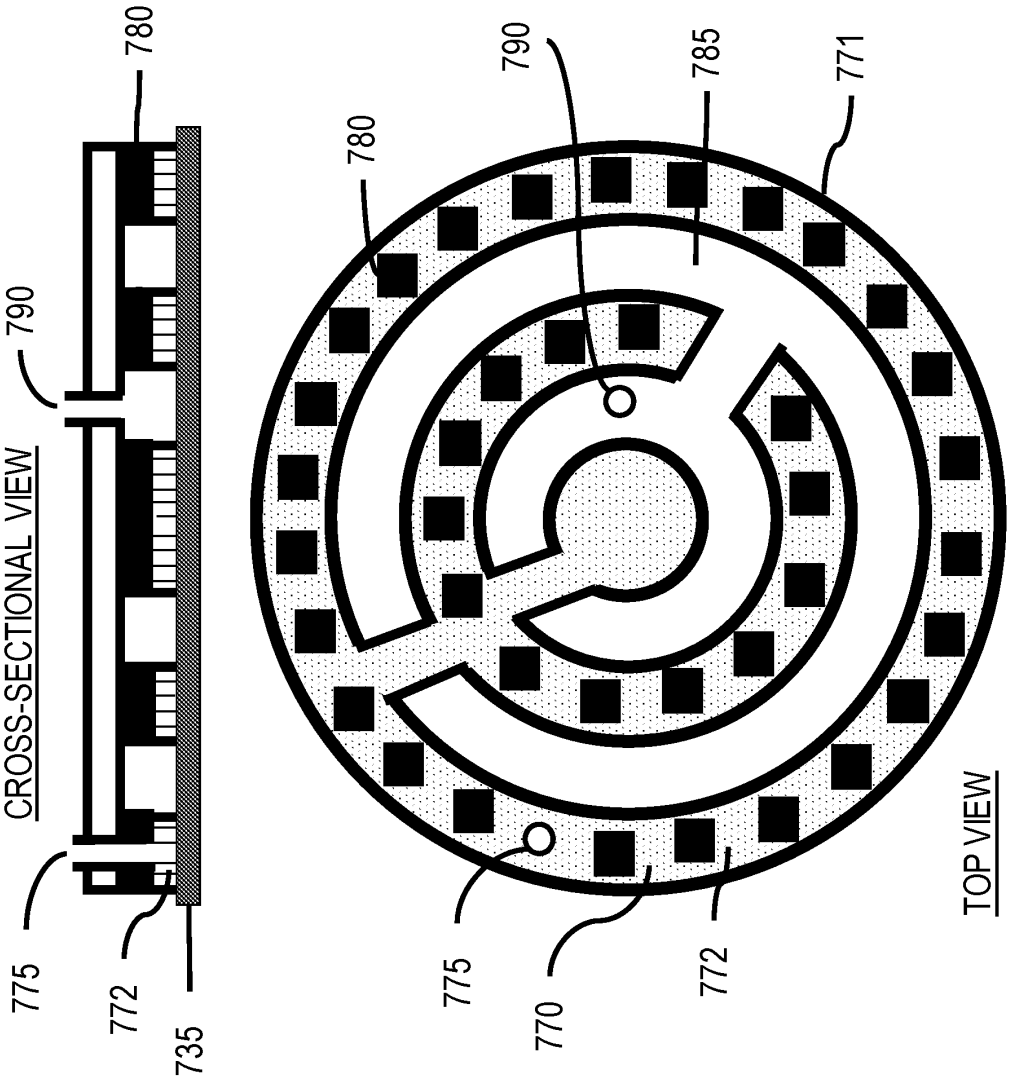
780
790
CROSS-SECTIONAL VIEW
775
772
735
780
790
785
771
775
770
772
TOP VIEW

FIG. 7B

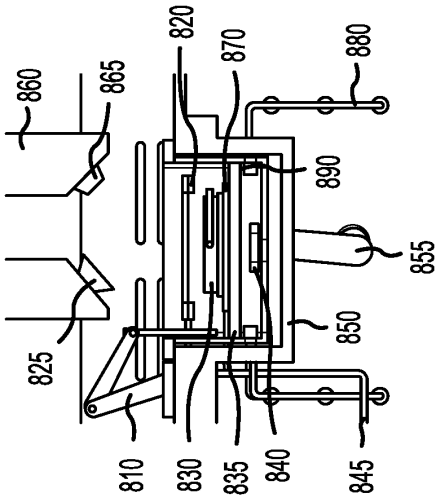
820
870
880
860
865
890
855
850
825
810
830
835
840
845

FIG.8B

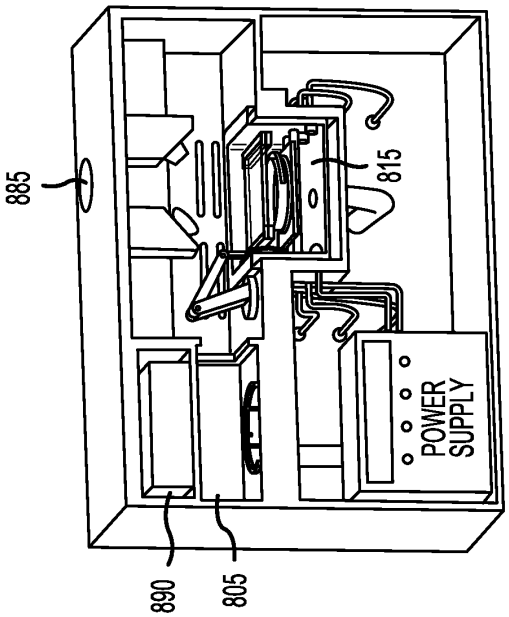
885
815
POWER SUPPLY
890
805

FIG.8A

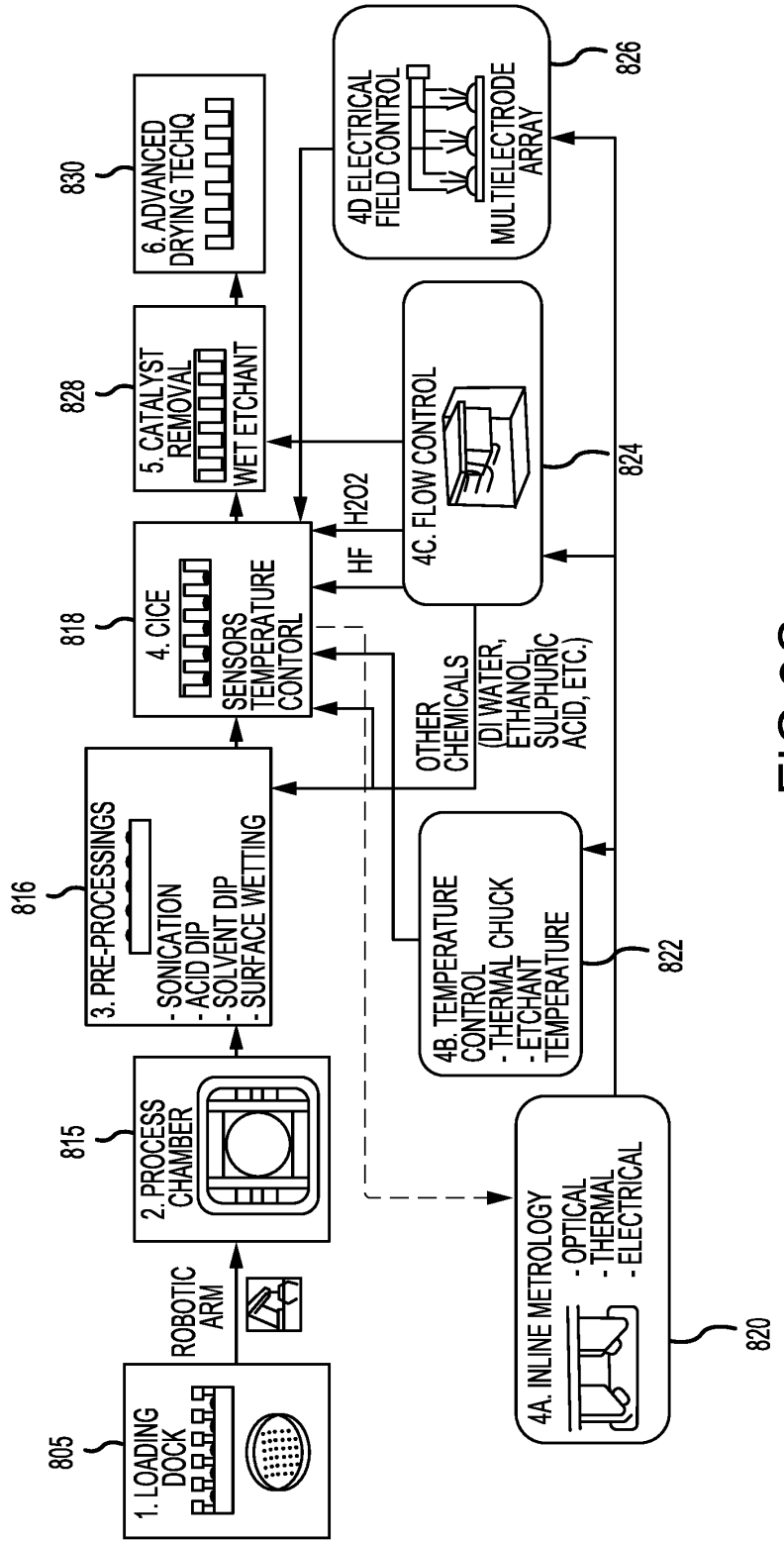
1. LOADING DOCK
805
ROBOTIC ARM
2. PROCESS CHAMBER
815
3. PRE-PROCESSINGS
- SONICATION
- ACID DIP
- SOLVENT DIP
- SURFACE WETTING
816
4. CICE
SENSORS TEMPERATURE CONTORL
818
5. CATALYST REMOVAL
WET ETCHANT
828
6. ADVANCED DRYING TECHQ
830
HF
H2O2
4C. FLOW CONTROL
824
4D ELECTRICAL FIELD CONTROL
MULTIELECTRODE ARRAY
826
OTHER CHEMICALS
(DI WATER, ETHANOL, SULPHURIC ACID, ETC.)
4B. TEMPERATURE CONTROL
- THERMAL CHUCK
- ETCHANT TEMPERATURE
822
4A. INLINE METROLOGY
- OPTICAL
- THERMAL
- ELECTRICAL
820

FIG.8C

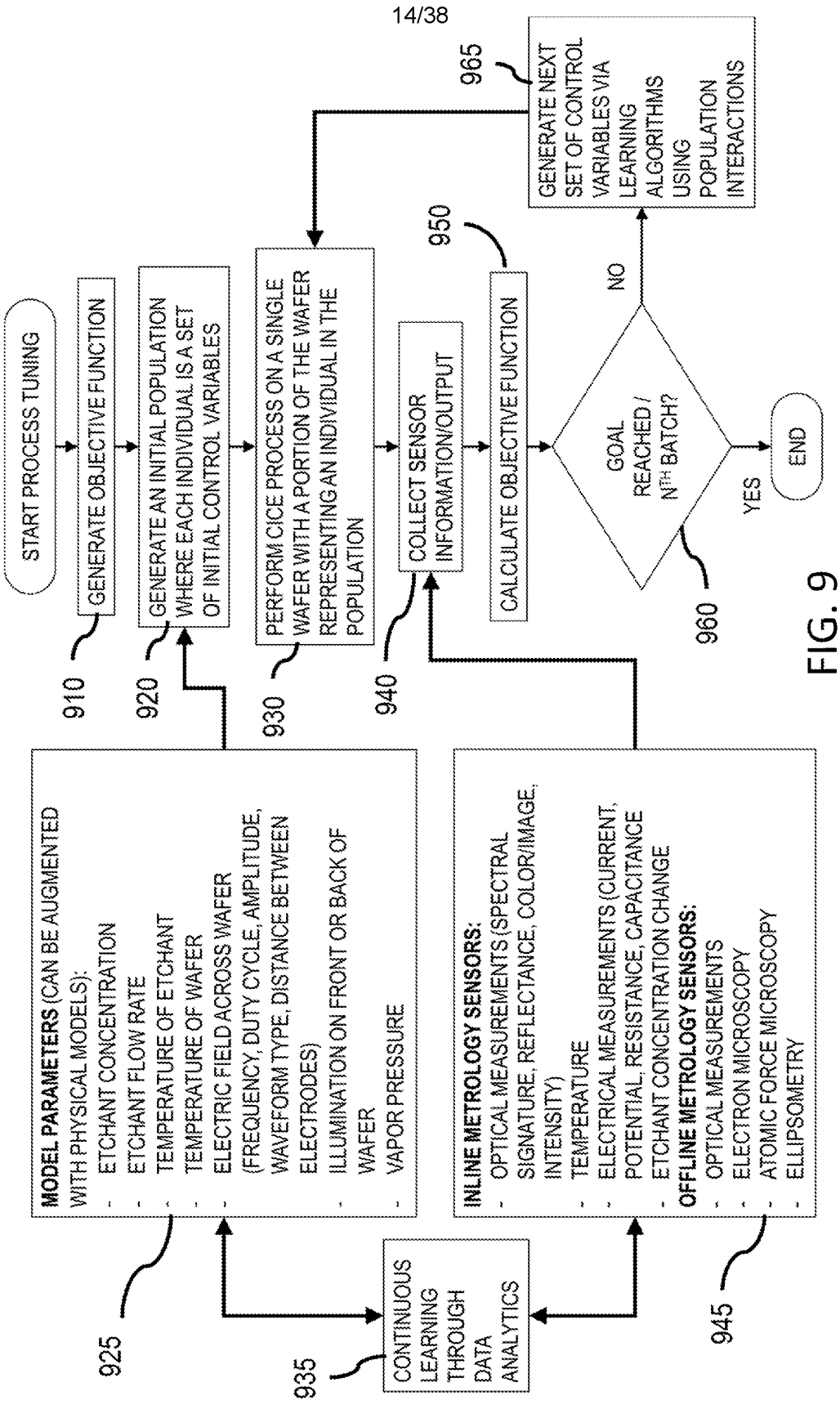
START PROCESS TUNING
GENERATE OBJECTIVE FUNCTION
GENERATE AN INITIAL POPULATION WHERE EACH INDIVIDUAL IS A SET OF INITIAL CONTROL VARIABLES
PERFORM CICE PROCESS ON A SINGLE WAFER WITH A PORTION OF THE WAFER REPRESENTING AN INDIVIDUAL IN THE POPULATION
COLLECT SENSOR INFORMATION/OUTPUT
CALCULATE OBJECTIVE FUNCTION
GOAL REACHED / NTH BATCH?
NO
YES
END
GENERATE NEXT SET OF CONTROL VARIABLES VIA LEARNING ALGORITHMS USING POPULATION INTERACTIONS
910
920
930
940
950
960
965
MODEL PARAMETERS (CAN BE AUGMENTED WITH PHYSICAL MODELS):
- ETCHANT CONCENTRATION
- ETCHANT FLOW RATE
- TEMPERATURE OF ETCHANT
- TEMPERATURE OF WAFER
- ELECTRIC FIELD ACROSS WAFER (FREQUENCY, DUTY CYCLE, AMPLITUDE, WAVEFORM TYPE, DISTANCE BETWEEN ELECTRODES)
- ILLUMINATION ON FRONT OR BACK OF WAFER
- VAPOR PRESSURE
925
CONTINUOUS LEARNING THROUGH DATA ANALYTICS
935
INLINE METROLOGY SENSORS:
- OPTICAL MEASUREMENTS (SPECTRAL SIGNATURE, REFLECTANCE, COLOR/IMAGE, INTENSITY)
- TEMPERATURE
- ELECTRICAL MEASUREMENTS (CURRENT, POTENTIAL, RESISTANCE, CAPACITANCE
- ETCHANT CONCENTRATION CHANGE
OFFLINE METROLOGY SENSORS:
- OPTICAL MEASUREMENTS
- ELECTRON MICROSCOPY
- ATOMIC FORCE MICROSCOPY
- ELLIPSOMETRY
945

FIG. 9

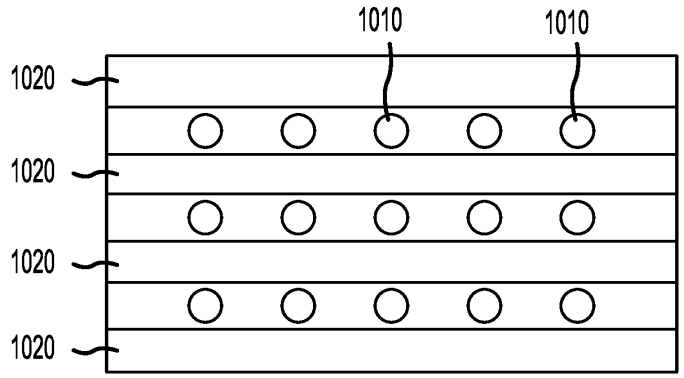


FIG.10A

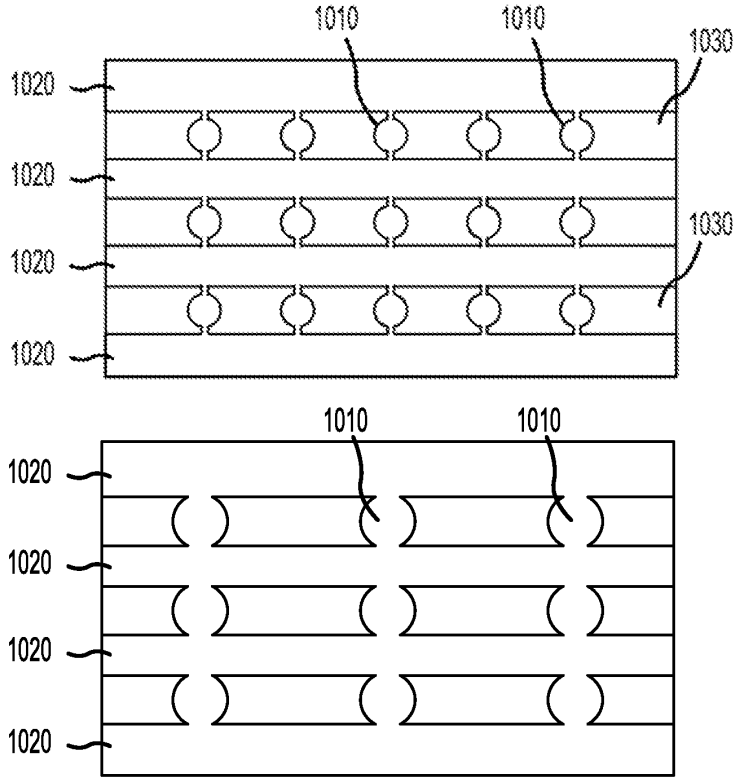


FIG.10B

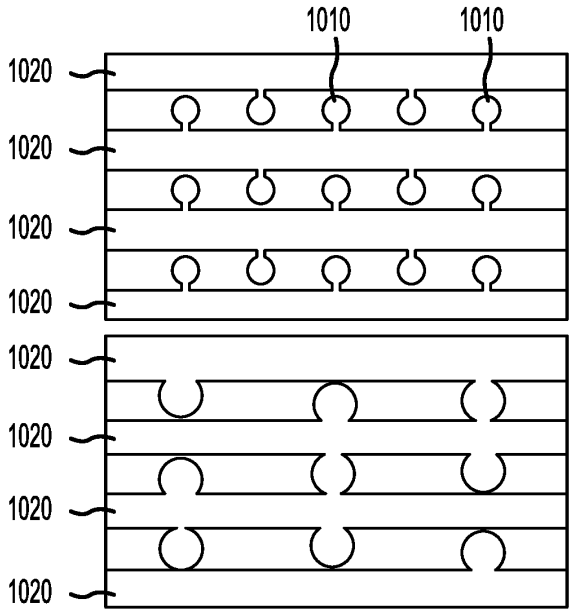


FIG.10C

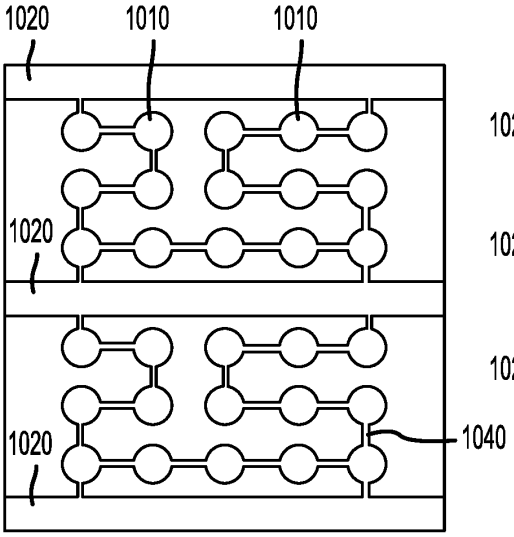


FIG.10D

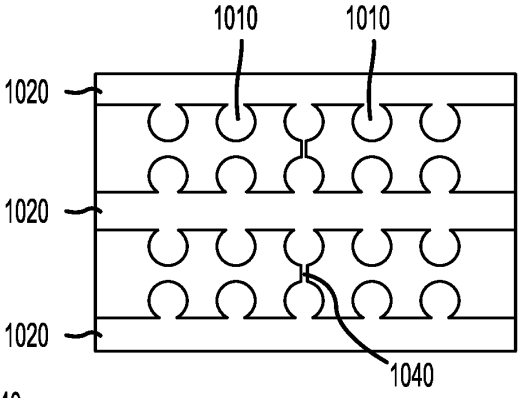


FIG.10E

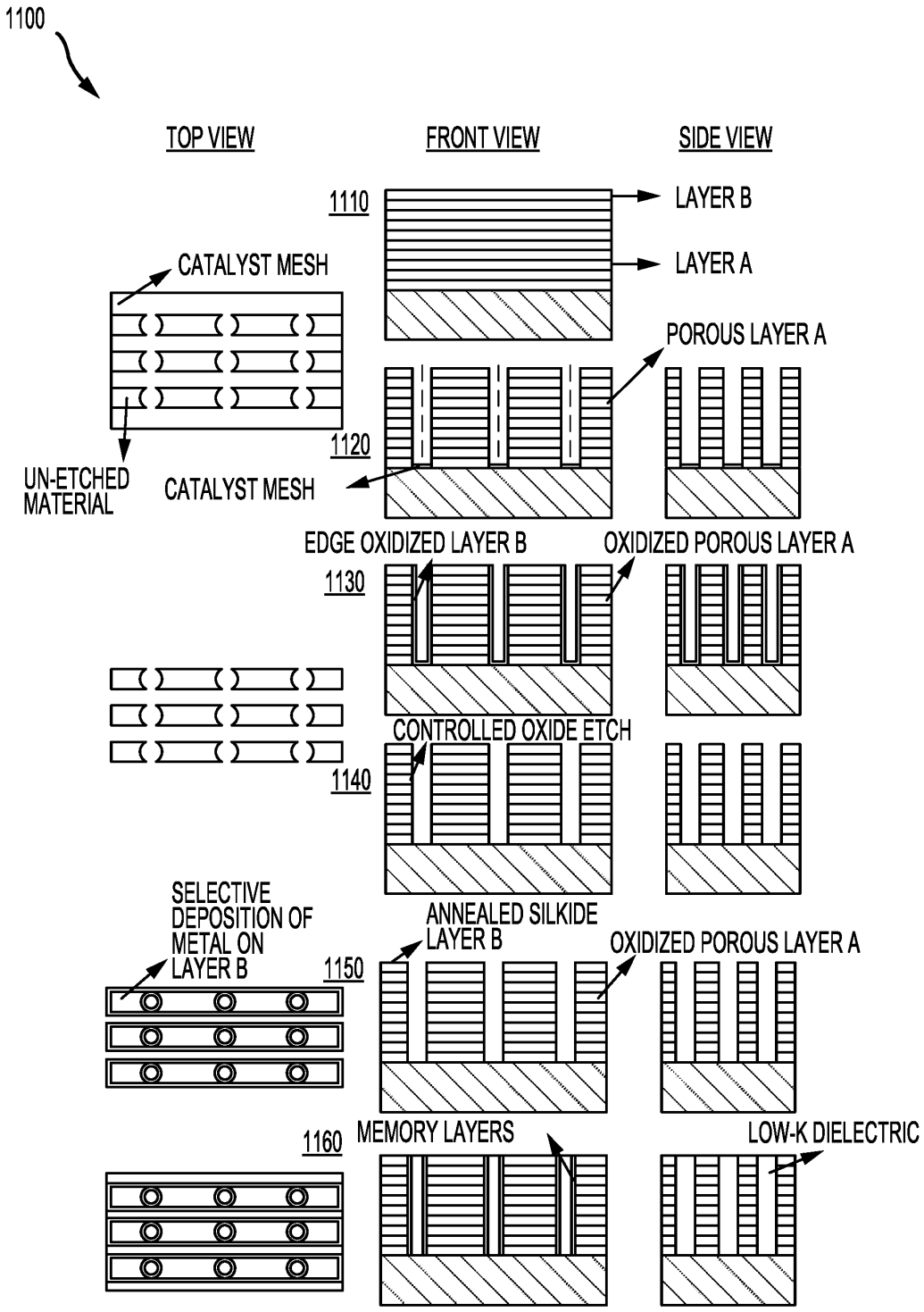
1100
TOP VIEW
FRONT VIEW
SIDE VIEW
1110
LAYER B
LAYER A
CATALYST MESH
POROUS LAYER A
1120
UN-ETCHED MATERIAL
CATALYST MESH
EDGE OXIDIZED LAYER B
OXIDIZED POROUS LAYER A
1130
CONTROLLED OXIDE ETCH
1140
SELECTIVE DEPOSITION OF METAL ON LAYER B
ANNEALED SILKIDE LAYER B
OXIDIZED POROUS LAYER A
1150
1160
MEMORY LAYERS
LOW-K DIELECTRIC

FIG.11

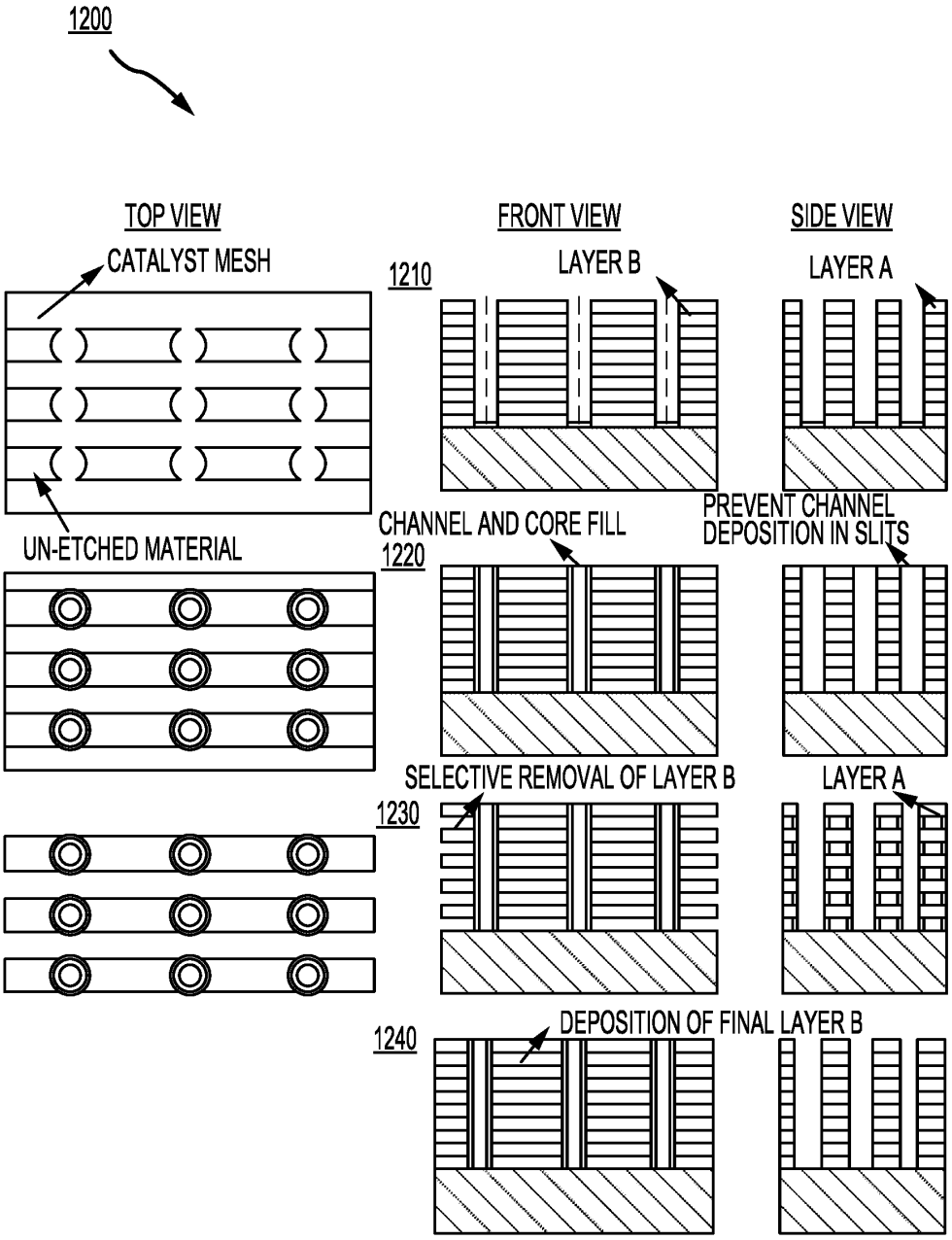
1200
TOP VIEW
FRONT VIEW
SIDE VIEW
CATALYST MESH
1210
LAYER B
LAYER A
UN-ETCHED MATERIAL
CHANNEL AND CORE FILL
1220
PREVENT CHANNEL DEPOSITION IN SLITS
SELECTIVE REMOVAL OF LAYER B
1230
LAYER A
1240
DEPOSITION OF FINAL LAYER B

FIG.12

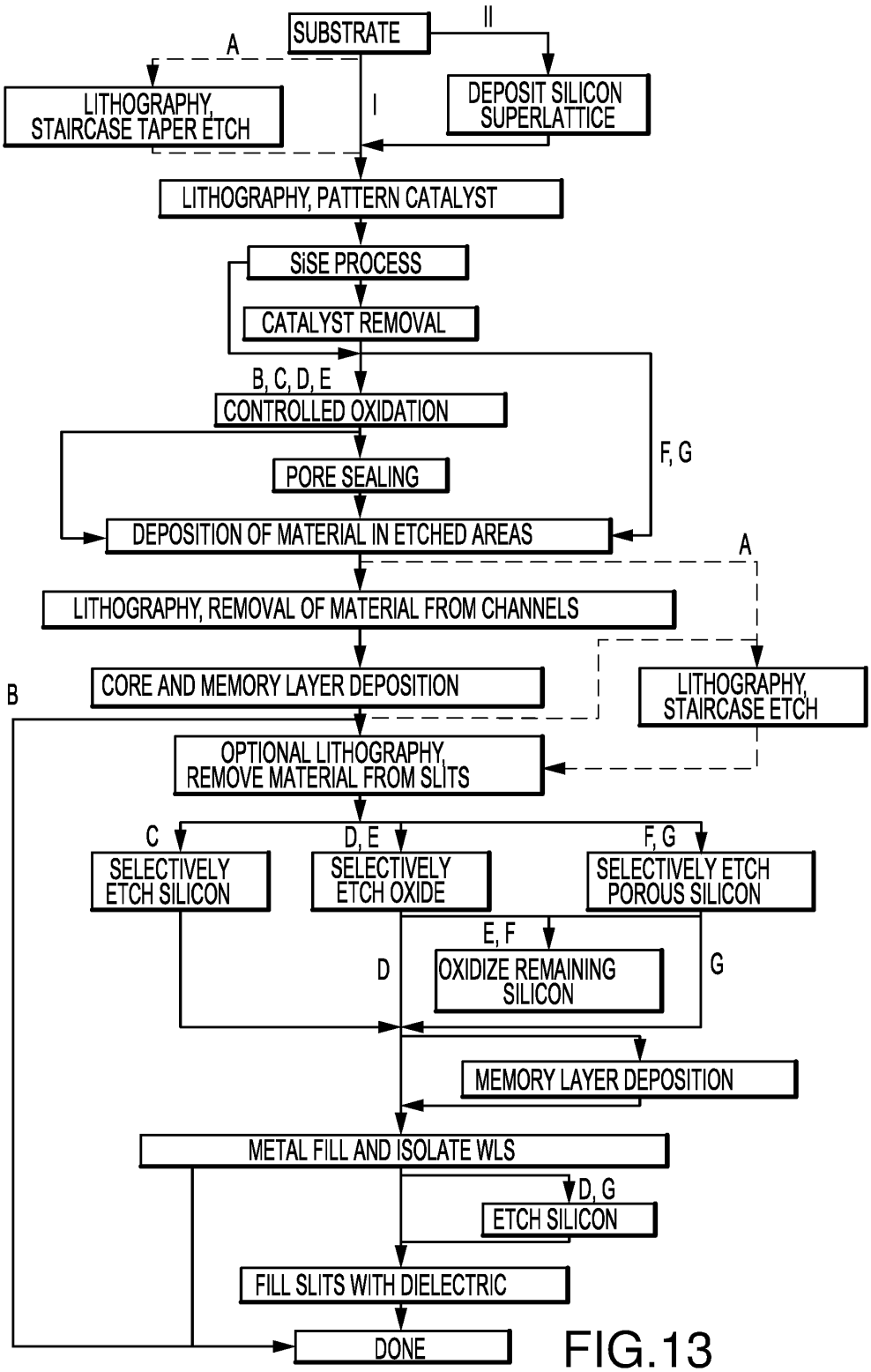
SUBSTRATE
II
A
I
LITHOGRAPHY, STAIRCASE TAPER ETCH
DEPOSIT SILICON SUPERLATTICE
LITHOGRAPHY, PATTERN CATALYST
SiSE PROCESS
CATALYST REMOVAL
B, C, D, E
CONTROLLED OXIDATION
PORE SEALING
F, G
DEPOSITION OF MATERIAL IN ETCHED AREAS
A
LITHOGRAPHY, REMOVAL OF MATERIAL FROM CHANNELS
B
CORE AND MEMORY LAYER DEPOSITION
LITHOGRAPHY, STAIRCASE ETCH
OPTIONAL LITHOGRAPHY, REMOVE MATERIAL FROM SLITS
C
D, E
F, G
SELECTIVELY ETCH SILICON
SELECTIVELY ETCH OXIDE
SELECTIVELY ETCH POROUS SILICON
E, F
D
OXIDIZE REMAINING SILICON
G
MEMORY LAYER DEPOSITION
METAL FILL AND ISOLATE WLS
D, G
ETCH SILICON
FILL SLITS WITH DIELECTRIC
DONE

FIG.13

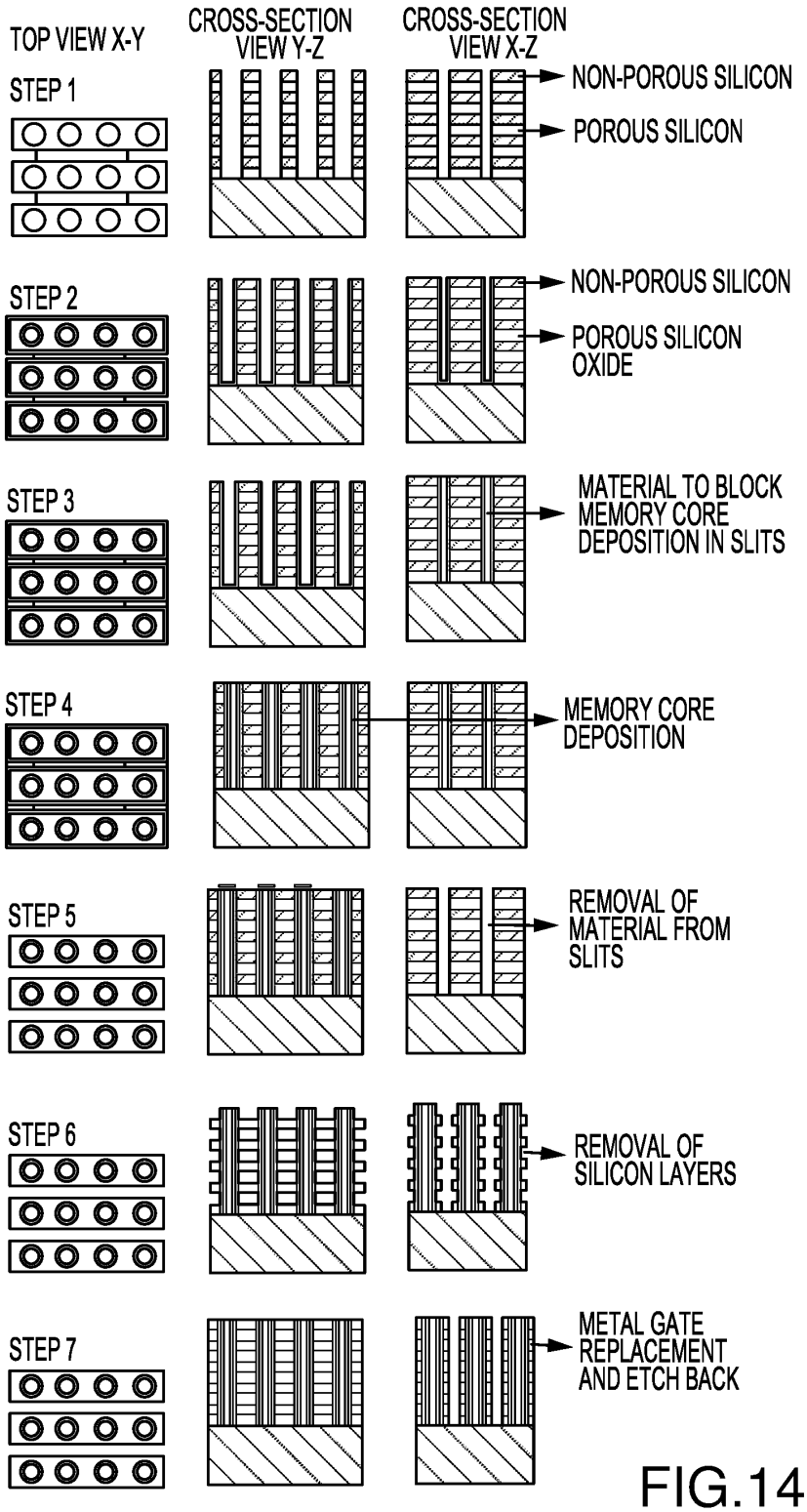
TOP VIEW X-Y
CROSS-SECTION VIEW Y-Z
CROSS-SECTION VIEW X-Z
STEP 1
NON-POROUS SILICON
POROUS SILICON
STEP 2
NON-POROUS SILICON
POROUS SILICON OXIDE
STEP 3
MATERIAL TO BLOCK MEMORY CORE DEPOSITION IN SLITS
STEP 4
MEMORY CORE DEPOSITION
STEP 5
REMOVAL OF MATERIAL FROM SLITS
STEP 6
REMOVAL OF SILICON LAYERS
STEP 7
METAL GATE REPLACEMENT AND ETCH BACK

FIG.14

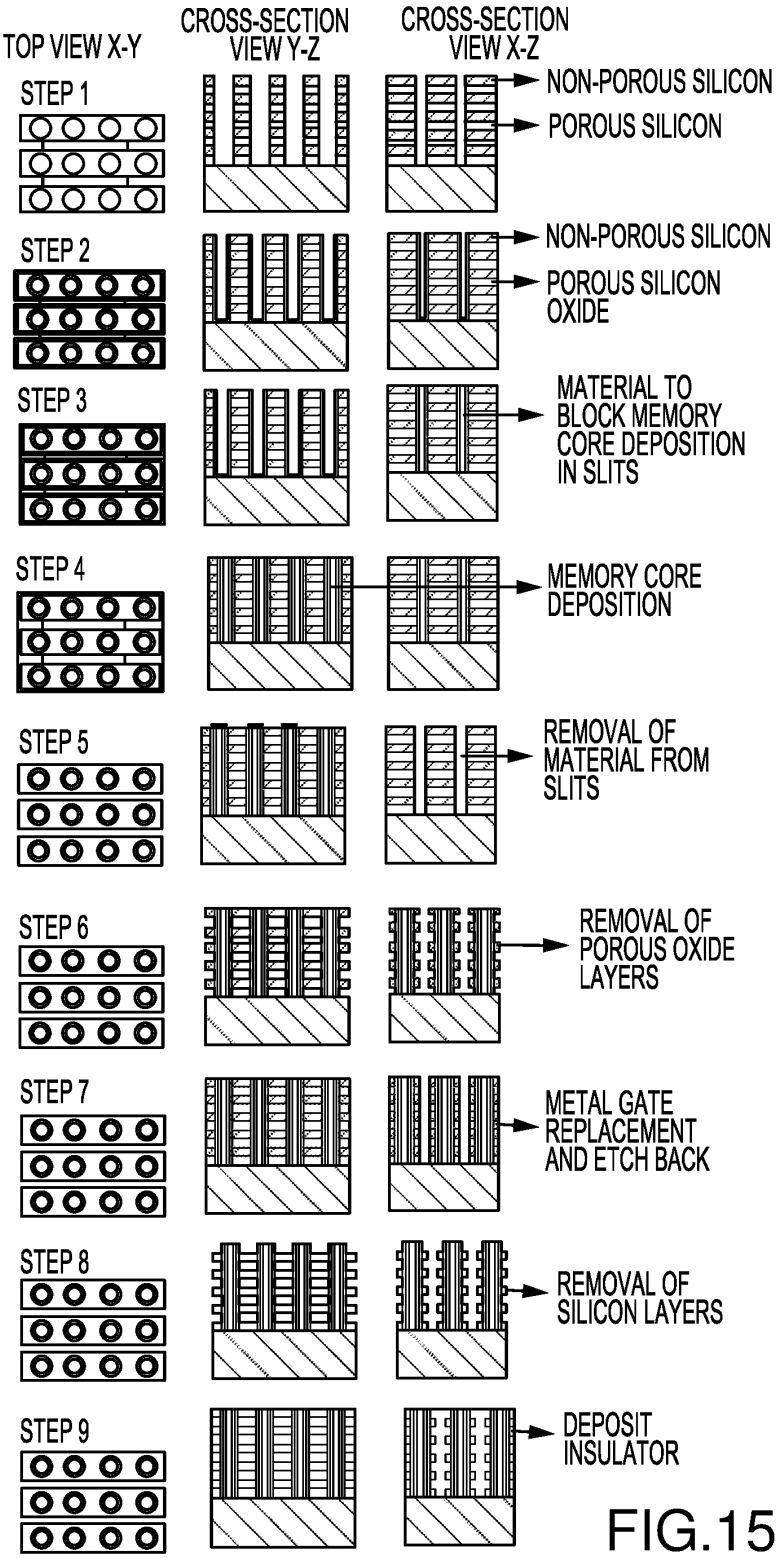
TOP VIEW X-Y
CROSS-SECTION VIEW Y-Z
CROSS-SECTION VIEW X-Z
STEP 1
NON-POROUS SILICON
POROUS SILICON
STEP 2
NON-POROUS SILICON
POROUS SILICON OXIDE
STEP 3
MATERIAL TO BLOCK MEMORY CORE DEPOSITION IN SLITS
STEP 4
MEMORY CORE DEPOSITION
STEP 5
REMOVAL OF MATERIAL FROM SLITS
STEP 6
REMOVAL OF POROUS OXIDE LAYERS
STEP 7
METAL GATE REPLACEMENT AND ETCH BACK
STEP 8
REMOVAL OF SILICON LAYERS
STEP 9
DEPOSIT INSULATOR

FIG.15

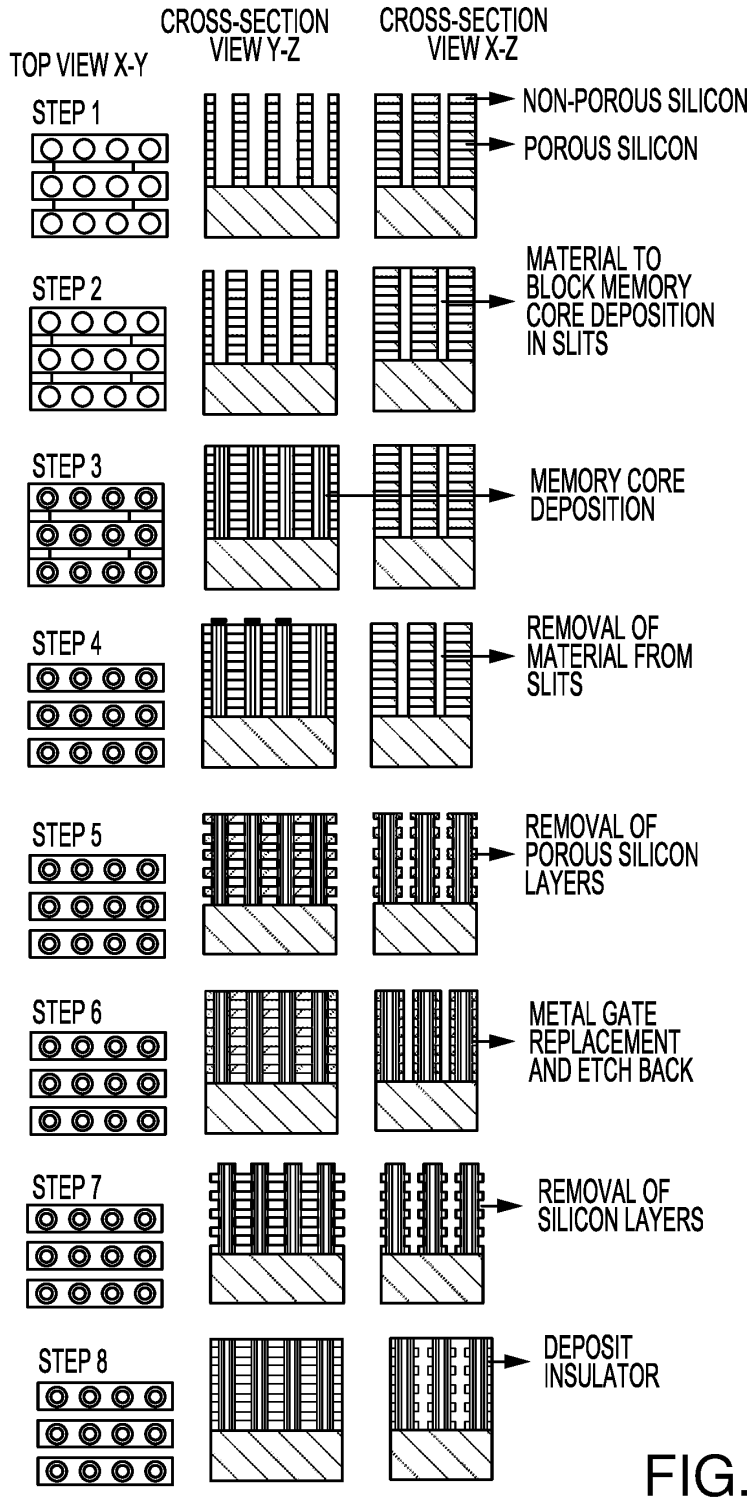
TOP VIEW X-Y
CROSS-SECTION VIEW Y-Z
CROSS-SECTION VIEW X-Z
STEP 1
NON-POROUS SILICON
POROUS SILICON
STEP 2
MATERIAL TO BLOCK MEMORY CORE DEPOSITION IN SLITS
STEP 3
MEMORY CORE DEPOSITION
STEP 4
REMOVAL OF MATERIAL FROM SLITS
STEP 5
REMOVAL OF POROUS SILICON LAYERS
STEP 6
METAL GATE REPLACEMENT AND ETCH BACK
STEP 7
REMOVAL OF SILICON LAYERS
STEP 8
DEPOSIT INSULATOR

FIG.16

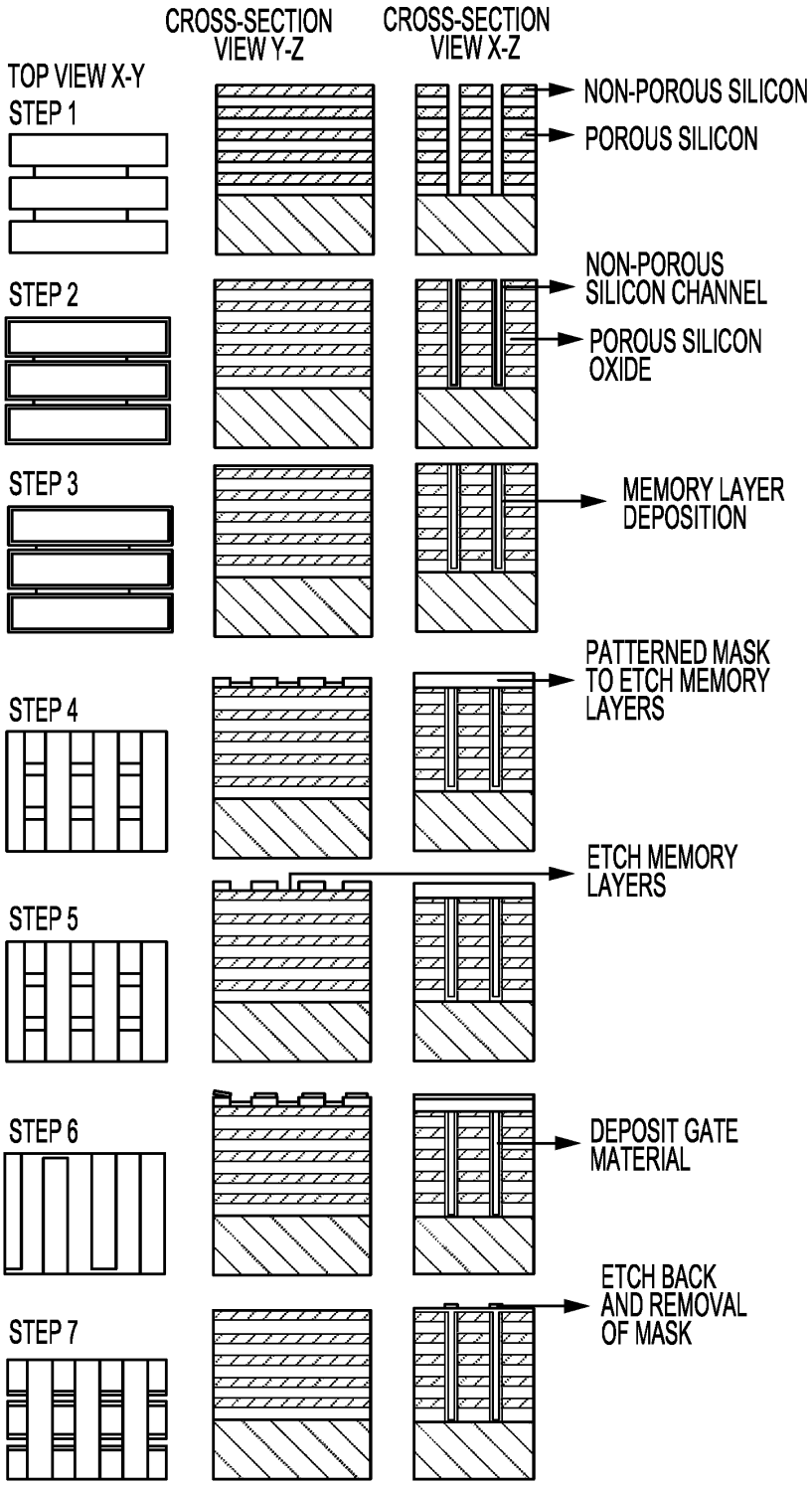
CROSS-SECTION VIEW Y-Z
CROSS-SECTION VIEW X-Z
TOP VIEW X-Y
STEP 1
NON-POROUS SILICON
POROUS SILICON
STEP 2
NON-POROUS SILICON CHANNEL
POROUS SILICON OXIDE
STEP 3
MEMORY LAYER DEPOSITION
STEP 4
PATTERNED MASK TO ETCH MEMORY LAYERS
STEP 5
ETCH MEMORY LAYERS
STEP 6
DEPOSIT GATE MATERIAL
STEP 7
ETCH BACK AND REMOVAL OF MASK

FIG.17

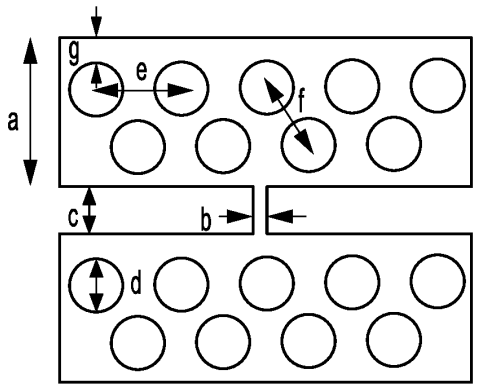


FIG.18A

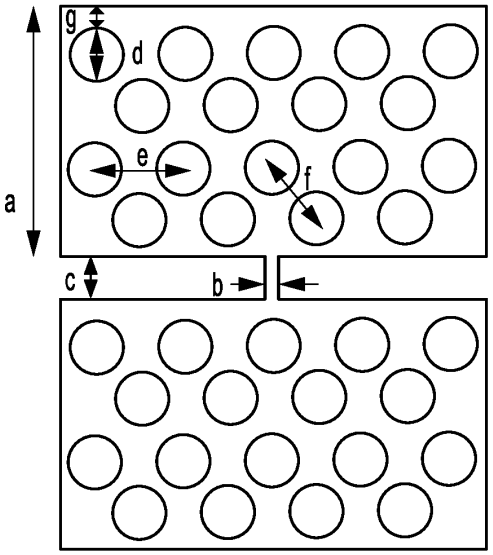


FIG.18B

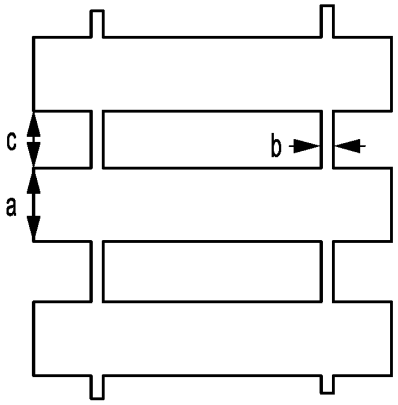


FIG.18C

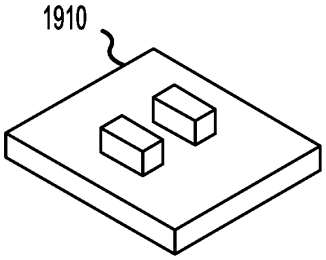


FIG.19A

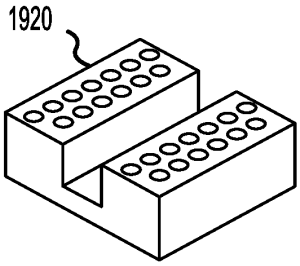


FIG.19B

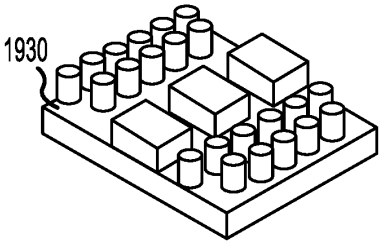


FIG.19C

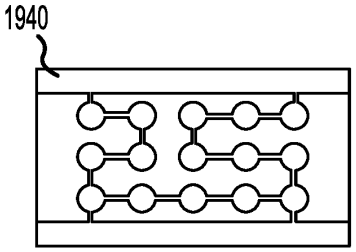


FIG.19D

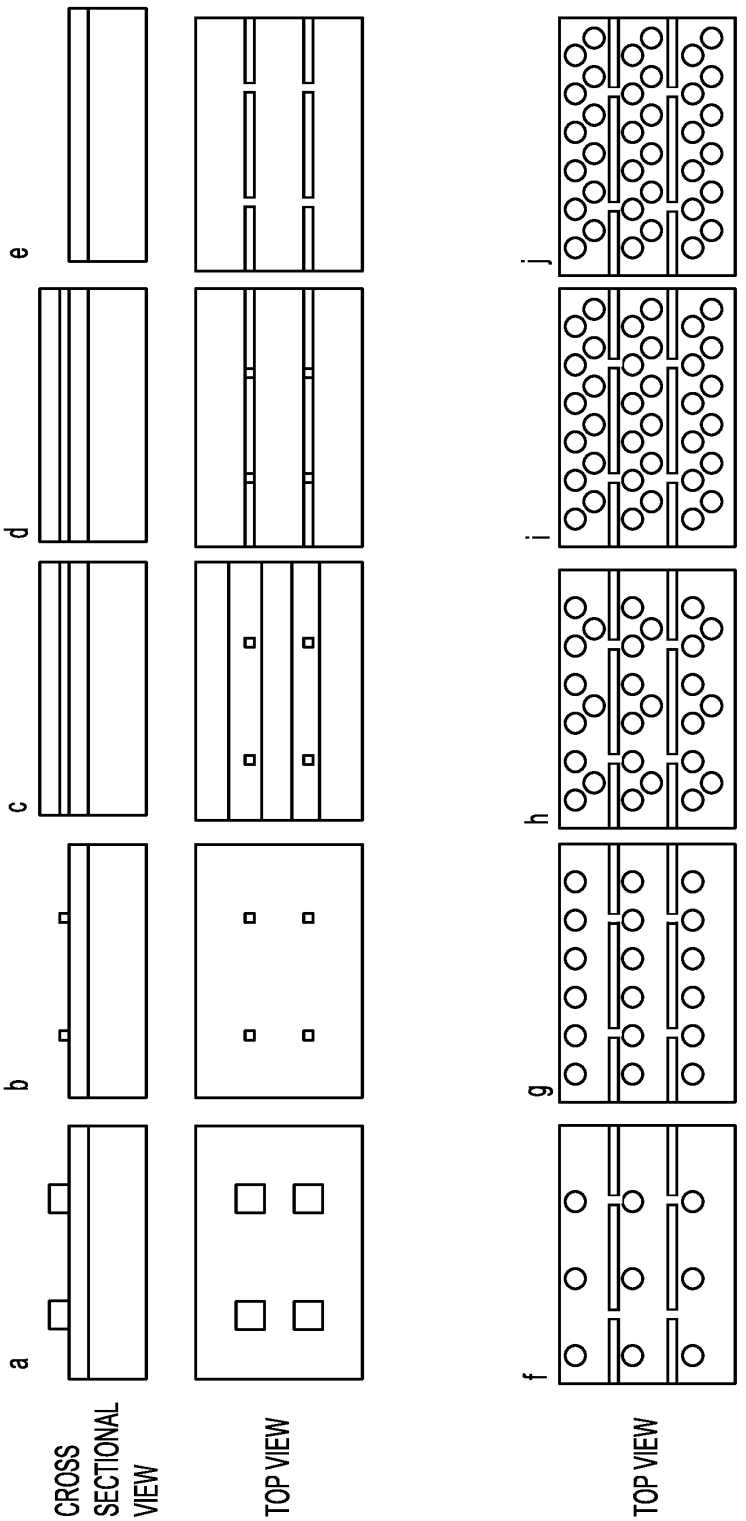


FIG.20

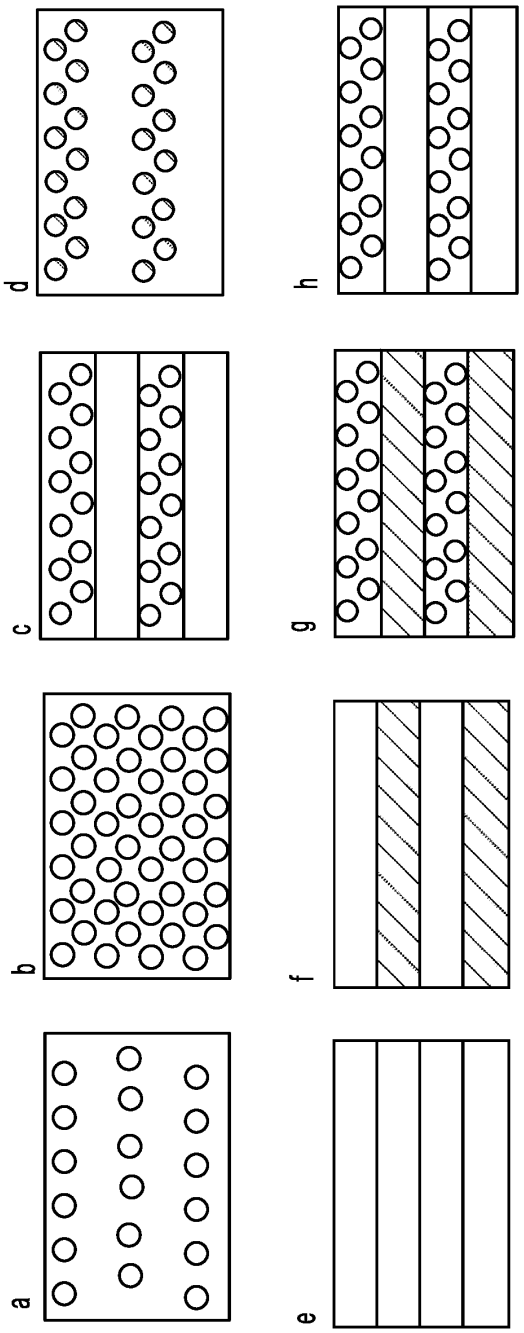


FIG.21

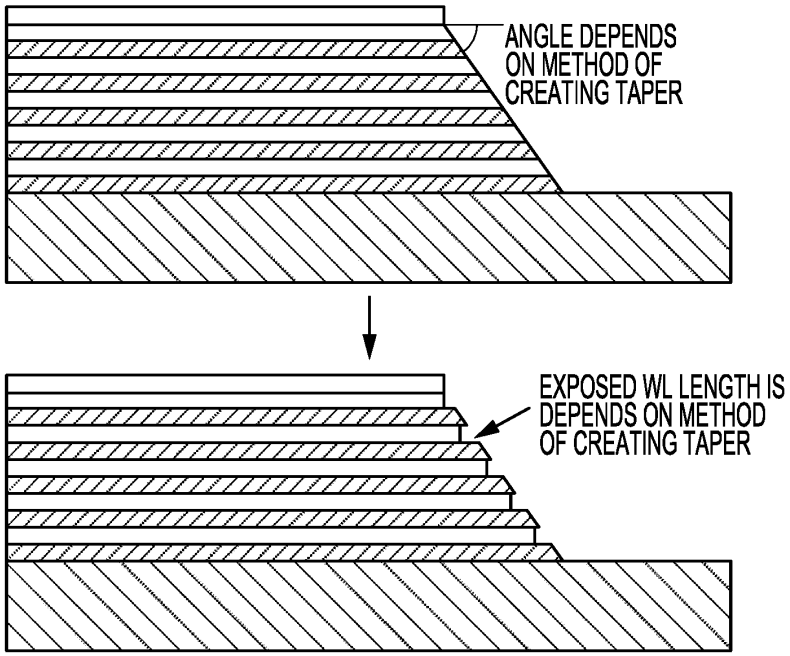
ANGLE DEPENDS ON METHOD OF CREATING TAPER
EXPOSED WL LENGTH IS DEPENDS ON METHOD OF CREATING TAPER

FIG.22

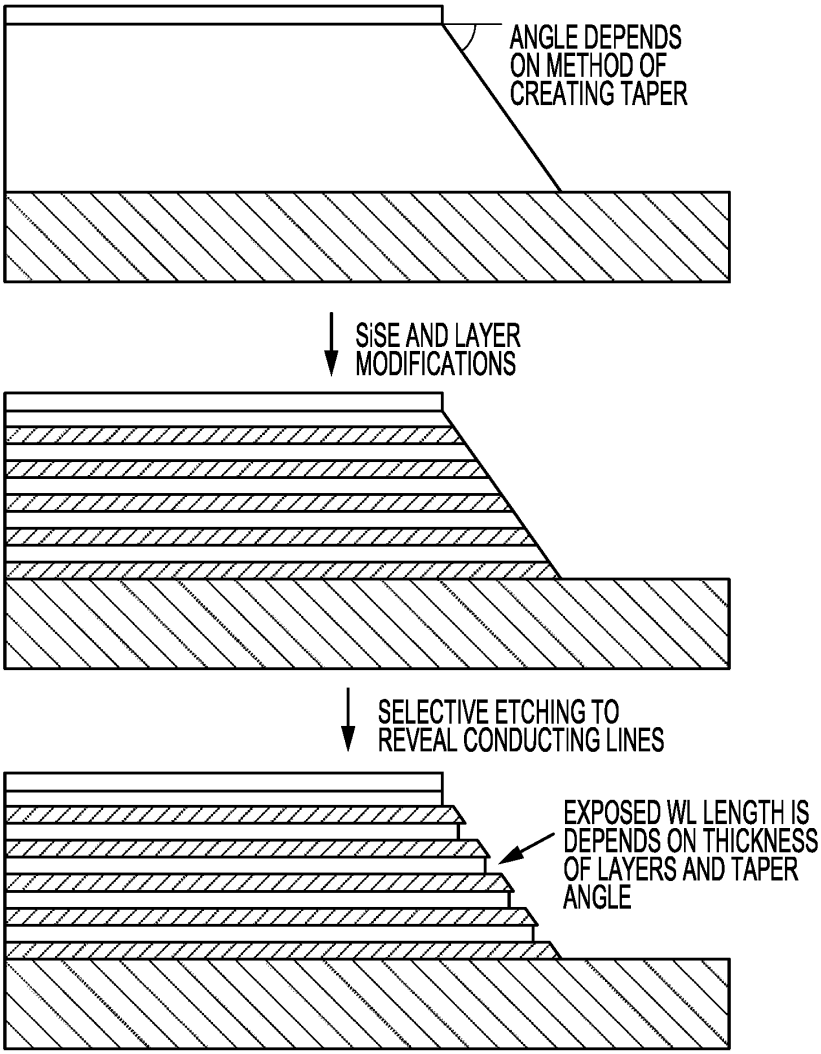
ANGLE DEPENDS ON METHOD OF CREATING TAPER
SiSE AND LAYER MODIFICATIONS
SELECTIVE ETCHING TO REVEAL CONDUCTING LINES
EXPOSED WL LENGTH IS DEPENDS ON THICKNESS OF LAYERS AND TAPER ANGLE

FIG.23

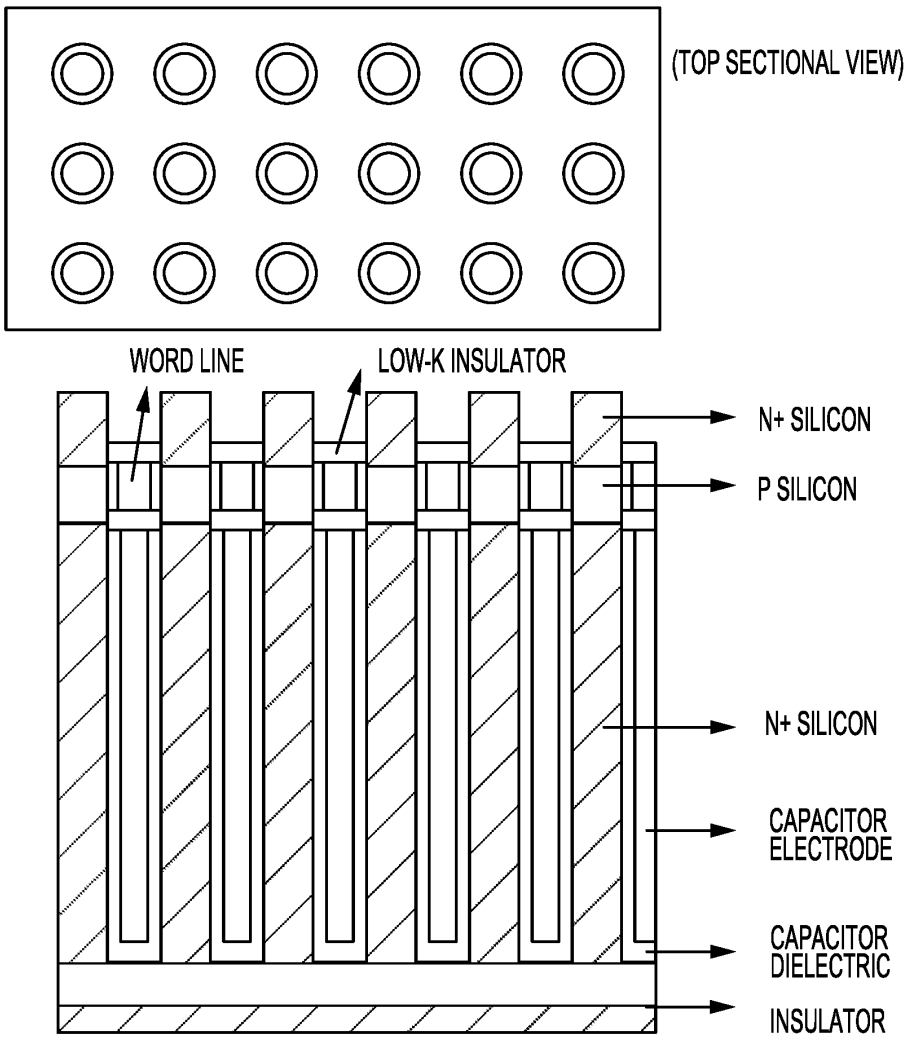
(TOP SECTIONAL VIEW)
WORD LINE
LOW-K INSULATOR
N+ SILICON
P SILICON
N+ SILICON
CAPACITOR ELECTRODE
CAPACITOR DIELECTRIC
INSULATOR

FIG.24

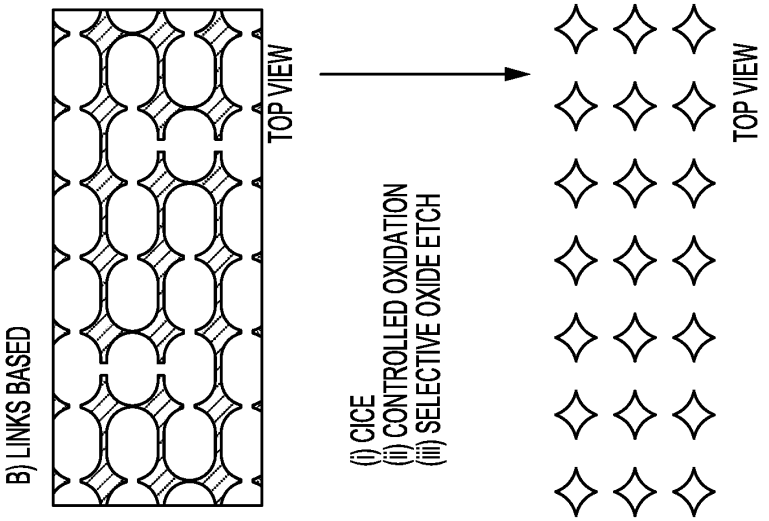


FIG.25B

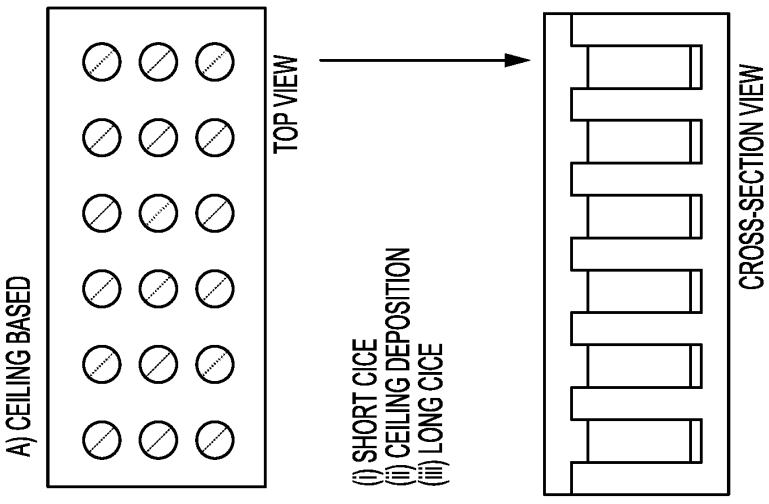


FIG.25A

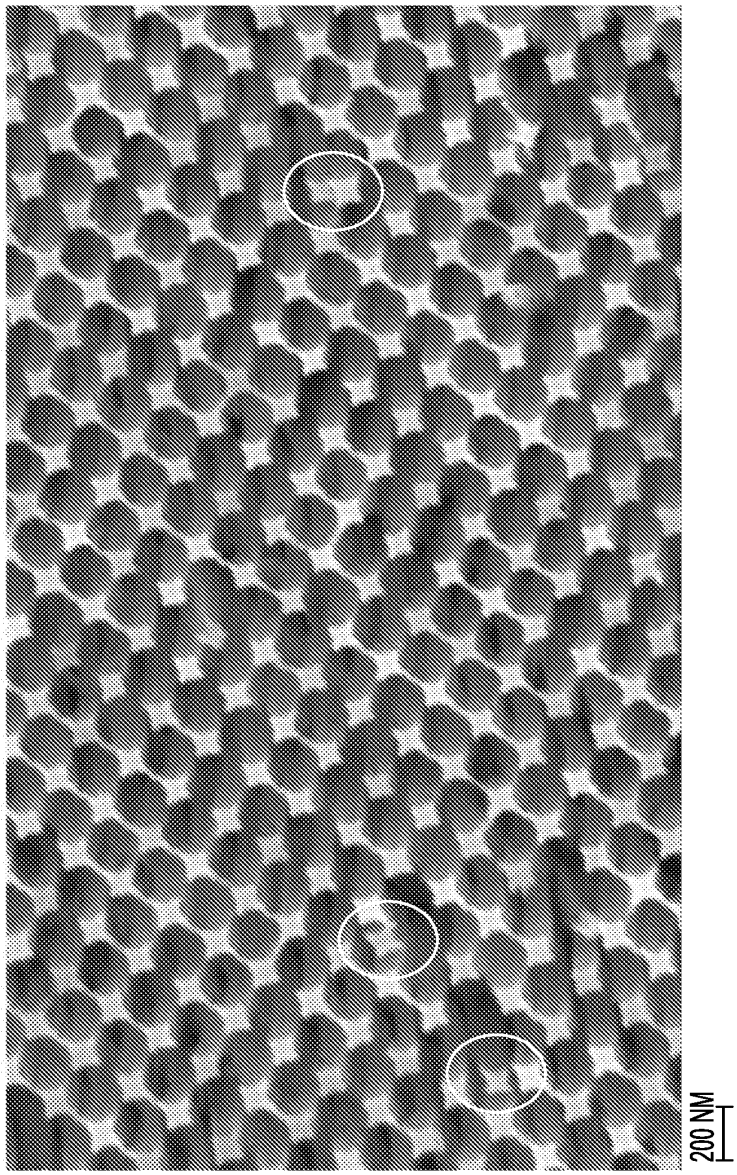


FIG.26

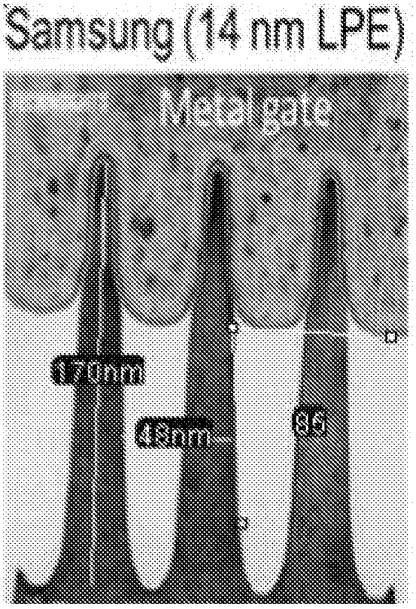


FIG.27A

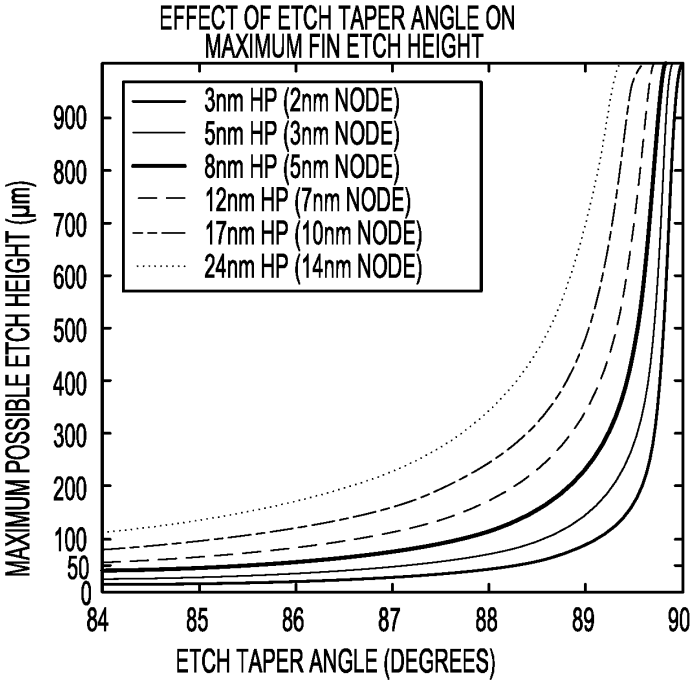


FIG.27B

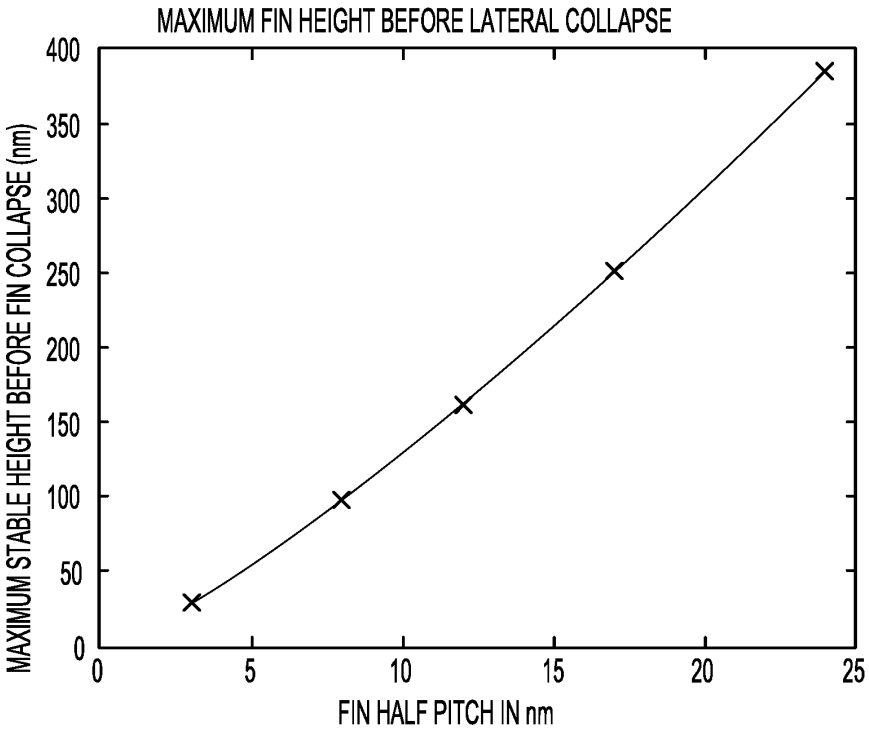
MAXIMUM FIN HEIGHT BEFORE LATERAL COLLAPSE
MAXIMUM STABLE HEIGHT BEFORE FIN COLLAPSE (nm)
400
350
300
250
200
150
100
50
0
0
5
10
15
20
25
FIN HALF PITCH IN nm

FIG.28

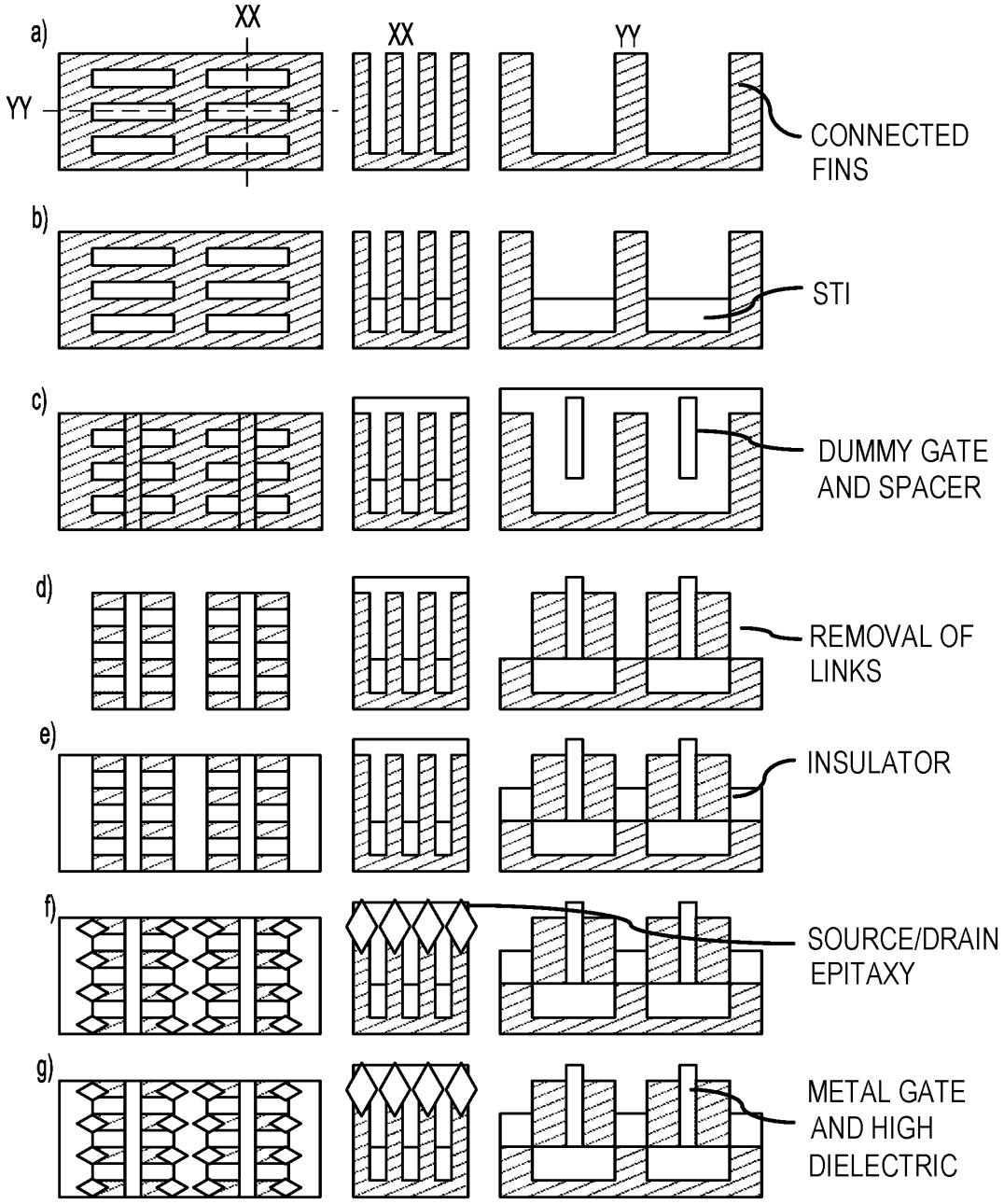
a)
XX
XX
YY
YY
CONNECTED FINS
b)
STI
c)
DUMMY GATE AND SPACER
d)
REMOVAL OF LINKS
e)
INSULATOR
f)
SOURCE/DRAIN EPITAXY
g)
METAL GATE AND HIGH DIELECTRIC

FIG.29

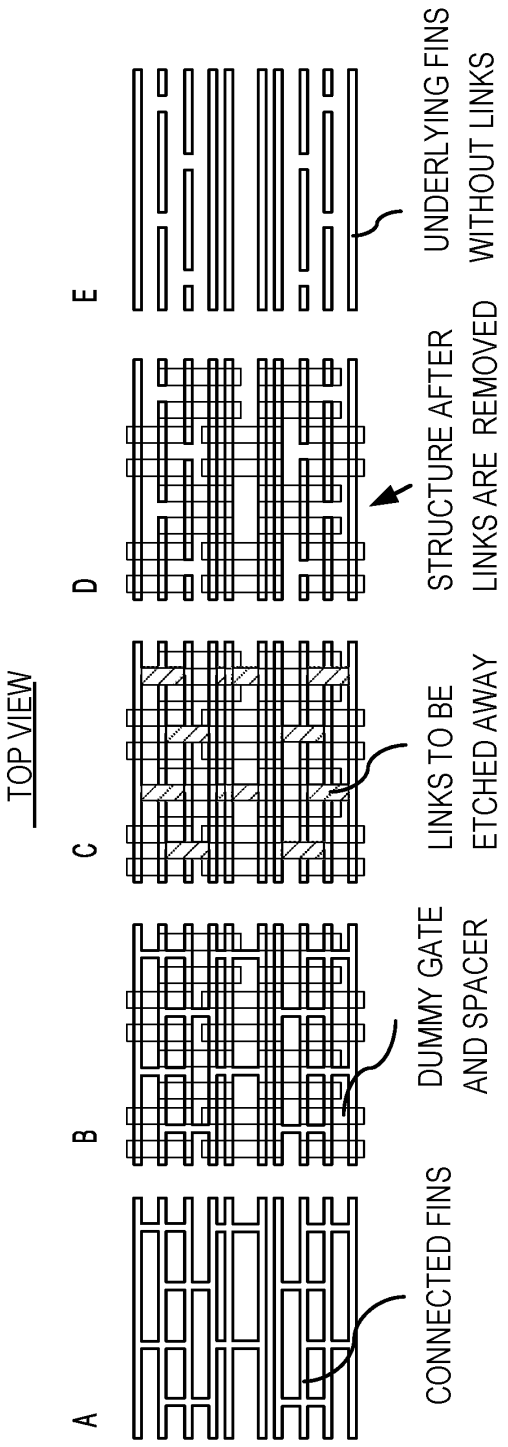
TOP VIEW
A
B
C
D
E
CONNECTED FINS
DUMMY GATE AND SPACER
LINKS TO BE ETCHED AWAY
STRUCTURE AFTER LINKS ARE REMOVED
UNDERLYING FINS WITHOUT LINKS

FIG.30

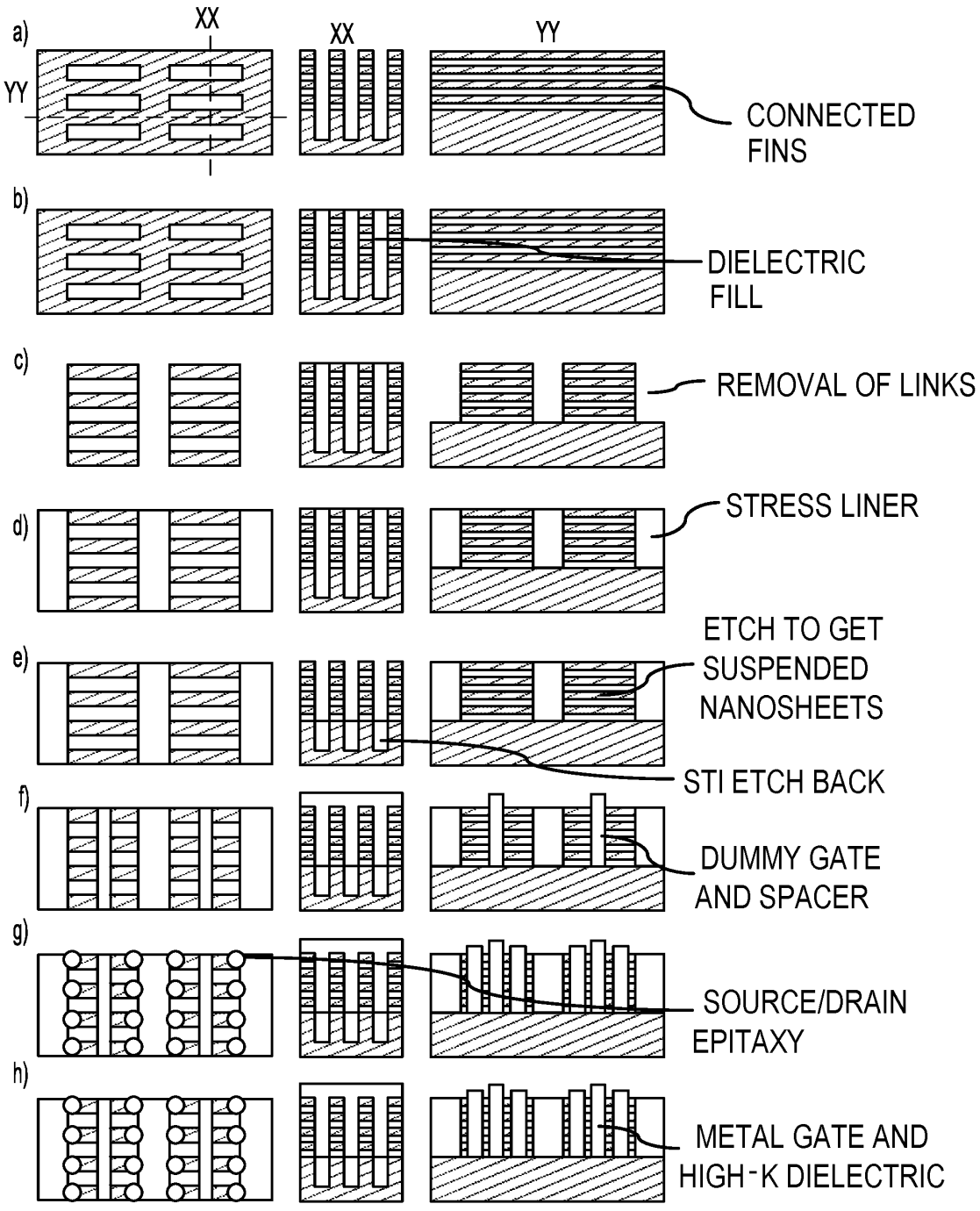
a)
XX
XX
YY
YY
CONNECTED FINS
b)
DIELECTRIC FILL
c)
REMOVAL OF LINKS
d)
STRESS LINER
e)
ETCH TO GET SUSPENDED NANOSHEETS
STI ETCH BACK
f)
DUMMY GATE AND SPACER
g)
SOURCE/DRAIN EPITAXY
h)
METAL GATE AND HIGH-K DIELECTRIC

FIG.31

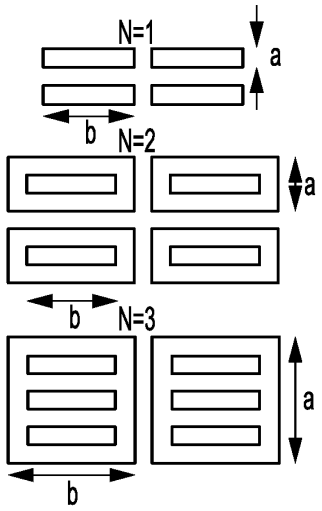


FIG.32A

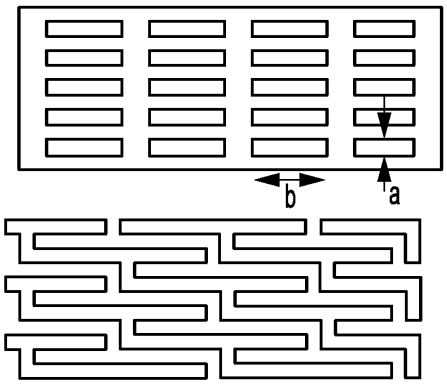


FIG.32B

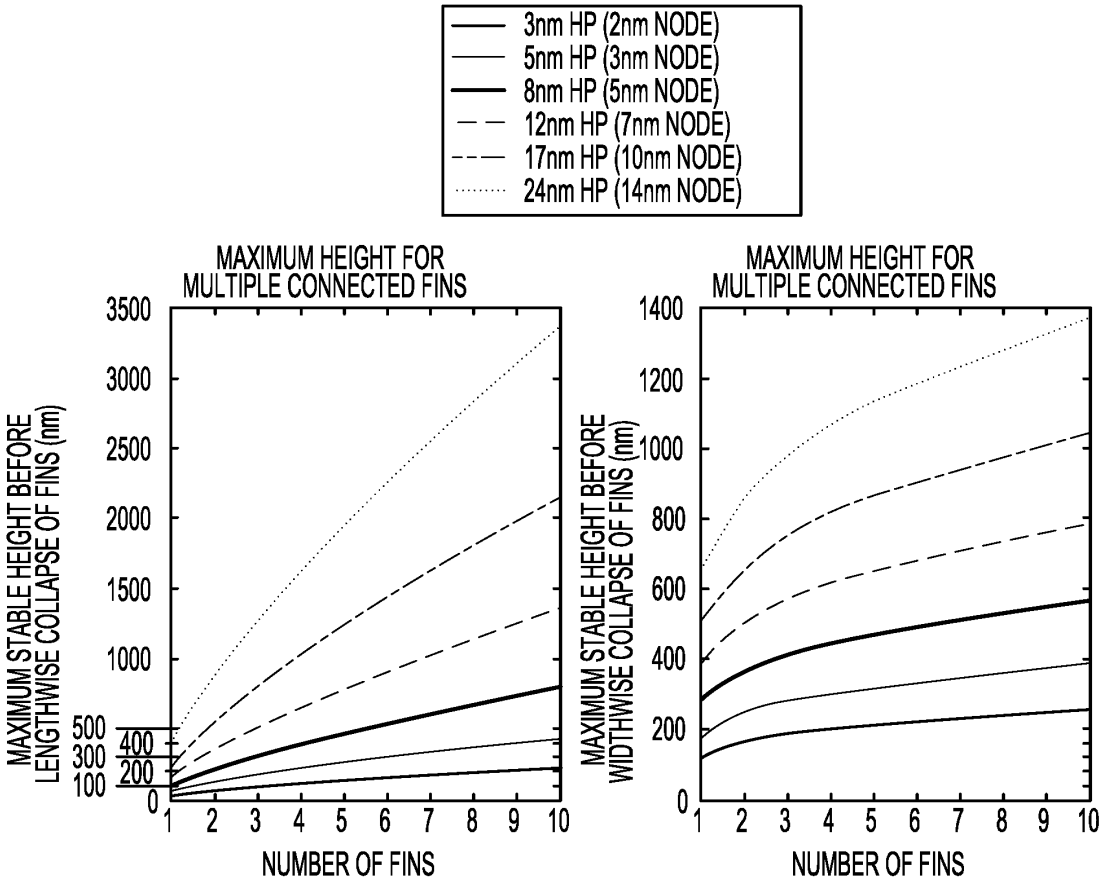


FIG.32C

FIG.32D