

APPARATUS AND METHOD FOR CONFIGURING SMALL SATELLITES

5 TECHNICAL FIELD

The present disclosure relates broadly to an apparatus and method for configuring small satellites.

10

BACKGROUND

Small satellites, particularly those that weigh below 50kg, have become popular in recent years. Small satellites based on the CubeSat standard are primarily developed for e.g. university research and provide an opportunity for low cost technology demonstration in space. In recent years, hundreds of small satellites that have been launched are based on the CubeSat standard.

The CubeSat standard was developed for satellites ranging from 1kg to 3kg with a form factor of 1U (approximately 10 cm x 10 cm x 10 cm) to 3U (approximately 10 cm x 10 cm x 30 cm). Each subsystem printed circuit board (PCB) follows the PC/104 form factor which defines a PCB having a dimension of 90.2 mm by 95.9 mm. A 104-pin CubeSat connector is provided along one side of the PCB. Four mounting holes are provided at the corners of the PCB to allow the boards to be fastened to each other using standoffs. Based on the defined mechanical dimensions, all subsystems can be stacked together and connected via the 104-pin CubeSat connector to form a complete satellite system. It has been recognized that small satellites based on the CubeSat standard have a robust design. The stackable bus connectors and the use of standoffs provide a rugged mounting configuration. The compact board size further contributes to the ruggedness of the form factor by reducing the possibility of PCB flexing under shock and vibration.

Since 2013, CubeSat has attracted much commercial interest and commercial companies have launched hundreds of 3U CubeSats into space. A number of the commercial companies have also attempted to launch larger size satellites having a form factor of 6U or 12U. The existing CubeSat standard serves well for educational purposes

and smaller scale commercial applications or simpler satellite missions using CubeSats with limited power and data rate requirements. However, there are limitations encountered as satellite missions become increasingly more complex and demanding.

5 In particular, the existing PC104 form factor PCB and 104-pin connector require the subsystems which are stacked together to be defined and assembled in a particular order. This limits flexibility in the arrangement of subsystems in the overall satellite bus. The stack-up connection of all the subsystems also poses a problem when any subsystem needs to be removed or added on, as the entire satellite may have to be dismantled in order to add or
10 remove a particular subsystem.

 The 104-pin connector also limits the number of pins available for interconnection. To cater for additional connections, additional connectors have to be mounted on the same PCB. Due to the small form factor (95.9 mm x 90.2 mm) of the PCB, the 104-pin connector
15 and additional connectors take up a significant portion of the available space on the PCB, thereby reducing the overall design flexibility and constraints. The real-estate available on each PCB is reduced further as cut-outs are made at the edges of the PCB to allow harnesses to run through the stack of subsystems.

20 In addition, the same 104-pin connector is used to carry both the signal and power lines. Consequently, this limits the current-carrying capability of the PCB. Furthermore, there will be a significant voltage drop between the first PCB to the last PCB of a stack, if the stack size is large.

25 Newer missions and larger scale small satellites that are larger than 3U require a better performing form factor that the existing standard based on PC104 may not be able to meet. With the satellite size growing beyond the initial 1U to 3U form factor, it becomes increasingly difficult to meet future needs in terms of satellite design and configuration, connectivity, power and signal requirements etc.

30 Thus, there is a need for an apparatus and a method for configuring small satellites that seek to address at least one of the above problems.

35

SUMMARY

According to one aspect, there is provided a satellite subsystem PCB comprising a first planar surface; a second planar surface opposite the first planar surface; at least a first pair of connectors on the first planar surface, each connector capable of electrically connecting a PC104 form factor PCB to the subsystem PCB; wherein the first pair of connectors are positioned on the first planar surface for allowing respective PC104 form factor PCBs to be spatially arranged in a side-by-side configuration when electrically connected to the subsystem PCB.

The satellite subsystem PCB may further comprise a further pair of connectors on the second planar surface, each connector capable of electrically connecting one PC104 form factor PCB to the subsystem PCB; wherein the further pair of connectors are positioned on the second planar surface for allowing respective PC104 form factor PCBs to be spatially arranged in a side-by-side configuration when electrically connected to the subsystem PCB.

The connectors may be positioned to allow respective planar surfaces of the PC104 form factor PCBs to be substantially parallel with the first and second planar surfaces of the satellite subsystem PCB.

The pair of connectors may be orientated in a substantially identical manner, for allowing respective PC104 form factor PCBs to be orientated on the subsystem PCB in a substantially identical manner, relative to the subsystem PCB, when electrically connected to the subsystem PCB.

The satellite subsystem PCB may further comprise one or more system connectors for electrically connecting to a main satellite system.

The one or more system connectors may be positioned at a first edge of the satellite subsystem PCB for allowing the satellite subsystem PCB to be installed on the main satellite system, such that the planar surface of the satellite subsystem PCB is substantially perpendicular to a backplane PCB of the main satellite system.

Each of the one or more system connectors may comprise a plurality of pins for transmission of power and/or signals.

One portion of the plurality of pins may be configured for transmission of power and another portion of the plurality of pins is configured for transmission of signals.

5 The satellite subsystem may comprise a first system connector configured for transmission of power; and a second system connector configured for transmission of signals.

10 The satellite subsystem PCB may further comprise additional connectors on the first planar surface and the second planar surface, wherein the additional connectors are positioned for receiving a customized PCB on each of the first and second planar surfaces, wherein the customized PCB is based on a different form factor from the PC104 form factor.

15 The satellite subsystem PCB may further comprise one or more external connectors positioned at a second edge of the satellite subsystem PCB, wherein the one or more external connectors are configured for connecting to respective one or more external modules.

20 The external modules may consist of one or more sensors selected from the group consisting of sun sensors, star tracker, fiber optic gyroscope, and magnetometer, one or more actuators selected from the group consisting of reaction wheels, magnetic torquers and thrusters, and one or more non-CubeSat based products selected from the group consisting of battery pack, high resolution camera, high gain antenna and remote sensing instrument.

25 The satellite subsystem PCB may further comprise one or more mounting holes for physically securing the PCB onto the subsystem PCB.

30 According to another aspect, there is provided a method for configuring a satellite subsystem PCB, the method comprising fabricating a PCB having a first planar surface and a second planar surface opposite the first planar surface; fabricating at least a first pair of connectors on the first planar surface, each connector capable of electrically connecting a PC104 form factor PCB to the subsystem PCB; wherein the first pair of connectors on the first planar surface are fabricated in respective positions for allowing respective PC104 form factor PCBs to be spatially arranged in a side-by-side configuration when electrically connected to the subsystem PCB.

The method may further comprise fabricating a further pair of connectors on the second planar surface, each connector capable of electrically connecting one PC104 form factor PCB to the subsystem PCB; wherein the further pair of connectors are fabricated in respective positions on the second planar surface for allowing respective PC104 form factor
5 PCBs to be spatially arranged in a side-by-side configuration when electrically connected to the subsystem PCB.

According to another aspect, there is provided a satellite system comprising, one or more subsystem PCBs as described herein; a backplane PCB for implementing a satellite
10 bus interface between the one or more subsystem PCBs, said backplane PCB comprising a planar surface; a plurality of slots provided on the planar surface of the backplane PCB, each slot for allowing a subsystem PCB to be installed thereon; wherein each of the one or more subsystems is installed with their respective planes being substantially perpendicular to the planar surface of the backplane PCB.

15

The satellite bus interface may comprise a main line and a redundant line.

The backplane PCB may be expandable to scale the form factor of the satellite
20 system.

20

The satellite bus interface may consist of one or more bus standards selected from the group consisting of CAN, I2C, SPI, SpaceWire, LVDS, RS-422, RS-232 and RS-485.

According to another aspect, there is provided a method for configuring a satellite
25 system, comprising providing a backplane PCB, said backplane PCB comprising a planar surface; a plurality of slots provided on the planar surface of the backplane PCB, each slot for allowing a subsystem PCB to be installed thereon; installing one or more subsystems as described herein to the backplane PCB via the plurality of slots; wherein the backplane PCB is configured to implement a satellite bus interface between the subsystem PCBs installed
30 thereon; and each of the one or more subsystems is positioned with its respective plane being substantially perpendicular to the planar surface of the backplane PCB.

35

BRIEF DESCRIPTION OF THE DRAWINGS

Exemplary embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of
5 example only, and in conjunction with the drawings, in which:

FIG. 1 is a plane view drawing of a satellite subsystem PCB in an exemplary embodiment.

10 FIG. 2A is a perspective view drawing of a satellite subsystem in an exemplary embodiment.

FIG. 2B is another perspective view drawing of the satellite subsystem in the exemplary embodiment.

15

FIG. 3A is a side view drawing of a satellite system in an exemplary embodiment.

FIG. 3B is a front view drawing of the satellite system when viewed from the direction as indicated on FIG. 3A.

20

FIG. 4 is a front view drawing of a satellite system having a first configuration in an exemplary embodiment.

25 FIG. 5 is a front view drawing of a satellite system having a second configuration in an exemplary embodiment.

FIG. 6A is a perspective view drawing of a satellite system in an exemplary embodiment.

30 FIG. 6B is another perspective view drawing of the satellite system in the exemplary embodiment.

FIG. 7 is a schematic overview of a satellite system in an exemplary embodiment.

35 FIG. 8 is a schematic flowchart for illustrating a method for configuring a satellite system in an exemplary embodiment.

FIG. 9 is a schematic flowchart for illustrating a method for configuring a satellite system.

5 FIG. 10 is a schematic drawing of a computer system suitable for implementing an exemplary embodiment.

FIG. 11 is a schematic drawing of a communication device suitable for implementing an exemplary embodiment.

10

FIG. 12A is a schematic diagram of a vertical flat-sat configuration of a satellite system and its external modules, when viewed from the side, in an exemplary embodiment.

FIG. 12B is a top view of the vertical flat-sat configuration of the satellite system and its external modules.

15

FIG. 12C is a schematic diagram of a horizontal flat-sat configuration, when viewed from the top, in a comparative example.

20

DETAILED DESCRIPTION

Exemplary, non-limiting embodiments may provide an apparatus and a method for configuring a satellite.

25

FIG. 1 is a plane view drawing of a satellite subsystem PCB 100 in an exemplary embodiment. The satellite subsystem may be part of a larger satellite system and performs specific action(s)/task(s) within the larger system. For example, the satellite subsystem may be an electrical power subsystem, attitude determination and control subsystem, communications subsystem, Global Navigation Satellite System (GNSS) subsystem, structure and thermal control subsystem, and onboard computer etc.

30

In the exemplary embodiment, the satellite subsystem PCB 100 has a substantially rectangular shape defined by two long edges 102, 104, two short edges 106, 108, a first planar surface 110 and a second planar surface 112 opposite the first planar surface 110. The satellite subsystem PCB 100 comprises a pair of connectors 114, 116 positioned on the

35

first planar surface 110. The pair of connectors 114, 116 are each capable of receiving a daughterboard PCB e.g. PC104 form factor CubeSat PCB which may be customized or commercial off-the-shelf (COTS) CubeSat products. In other words, up to two PC104 form factor CubeSat PCBs may be electrically connected to the first planar surface 110, via the
5 pair of connectors 114, 116.

In the exemplary embodiment, the pair of connectors 114, 116 are positioned on the first planar surface 110 for allowing respective PC104 form factor PCBs to be spatially arranged in a side-by-side configuration and parallel to the subsystem PCB 100, when
10 electrically connected to the subsystem PCB 100. The pair of connectors 114, 116 are orientated in a substantially identical manner for allowing respective daughterboard PCBs e.g. PC104 form factor CubeSat PCB to be orientated on the subsystem PCB 100 in a substantially identical manner relative to the subsystem PCB 100, when electrically
15 connected to the subsystem PCB 100. Such a configuration provides space saving and facilitates the design of wire pathways on the PCB. In other exemplary embodiments, the pair of connectors 114, 116 may be orientated differently from each other, e.g. one positioned along a long edge and one positioned along a short edge of the PCB, to suit specific requirements of a subsystem.

It would be appreciated that the configuration/ arrangement of connectors e.g. 114, 116 on the first planar surface 110 may be replicated on the second planar surface 112 such that the motherboard PCB 100 is capable of receiving up to four CubeSat boards (i.e. two CubeSat boards on each side of the motherboard PCB 100). The satellite subsystem PCB 100 may also further comprise additional connectors e.g. 118, 120 which are configured for
20 electrically coupling to daughterboard PCBs of other form factors, e.g. customized non-CubeSat based PCBs as well as a front/external connector 122 for electrically connecting to an external module and components.

FIG. 2A is a perspective view drawing of a satellite subsystem 200 in an exemplary
30 embodiment. FIG. 2B is another perspective view drawing of the satellite subsystem 200 in the exemplary embodiment.

The satellite subsystem 200 comprises a subsystem PCB 202 having a rectangular shape defined by two long edges 204, 206, two short edges 208, 210, a first planar surface
35 212 and a second planar surface 214 opposite the first planar surface 212. The subsystem PCB 202 is substantially similar in structure and function to the satellite subsystem PCB 100

of FIG. 1. The subsystem PCB 202 comprises a pair of connectors e.g. 104-pin connectors 216, 218 disposed on the first planar surface 212. The 104-pin connectors 216, 218 are positioned on the first planar surface 212 such that each 104-pin connector is capable of electrically connecting/coupling a daughterboard PCB 220 to the subsystem PCB 202. In the
5 exemplary embodiment, the subsystem PCB 202 comprises mounting holes e.g. 222 disposed at the four corners of the subsystem PCB 202 where each mounting hole 222 is configured for receiving a standoff (not shown) to physically secure/ support a daughterboard PCB.

10 The daughterboard PCB 220 may be a customized or commercial off-the-shelf (COTS) PCB, e.g. PC104 form factor PCB 220. In the exemplary embodiment, the connectors 216, 218 are each positioned to receive a respective PC104 form factor PCB 220 such that the planar surface of the PC104 form factor PCB 220 is substantially parallel to the first planar surface 212 and second planar surface 214 of the subsystem PCB 202. For the
15 purpose of illustration, FIG. 2A and 2B show only one PC104 form factor PCB 220 electrically connected to the subsystem PCB 202 via connector 218 while connector 216 is not shown to be connected to a daughterboard PCB. The PC104 form factor PCB 220 comprises a connector e.g. 104-pin connector 224 for electrically connecting to another daughterboard e.g. PC104 form factor PCB, such that additional daughterboard(s) may be
20 stacked on the PC104 form factor PCB 220.

In the exemplary embodiment, the subsystem PCB 202 is capable of receiving up to two daughterboard PCBs on one side, i.e. the first planar surface 212. Alternatively, the motherboard PCB can also receive a customized PCB which may be based on a different
25 form factor from the PC104 form factor. For example, the customized PCB may be twice the size of a standard PC104 form factor PCB (compare embodiment shown in e.g., FIG. 5). Additional connectors e.g. 226 may be provided to facilitate the coupling of the customized PCB. Such a configuration may advantageously remove the constraint of the current PC104 form factor approach in CubeSat satellites and allow flexible PCB sizes for the
30 daughterboards/ add-on modules, up to 211.8 mm in length by 90.2 mm in breadth for subsystem PCB 202.

The subsystem PCB 202 further comprises two system connectors/ backplane connectors 228, 230 disposed at an edge of the subsystem PCB 202 along the long edge
35 204, having a coupling direction which is substantially parallel to the planar surface of the subsystem PCB 202. The system connectors 228, 230 are configured for connecting/

installing the subsystem PCB 202 to a main satellite system and may be selected from the group consisting of CAN, I2C, SPI, SpaceWire, LVDS, RS-422, RS232 and RS-485 etc. By having dual system connectors on the subsystem PCB 202, the satellite subsystem 200 may be designed such that one system connector e.g. 228 is reserved for power supplies while
5 the other system connector e.g. 230 is reserved for the signal lines, or both backplane connectors can be used for mixed power and signal lines. For example, each backplane connector may comprise a first set of pins configured for transmitting power and a second set of pins configured for transmitting signals. In another example, each backplane connector may comprise a plurality of pins which are configured for transmitting power only,
10 or signals only. It would be appreciated that the number of system connectors is not limited to two connectors. Other exemplary embodiments may comprise one system connector, or more than two system connectors.

The subsystem PCB 202 further comprises external connectors 232, 234 for coupling
15 to one or more external modules e.g. sensors, actuators and non-CubeSat based products. External modules may include, but are not limited to both sensors and actuators. Sensors may include, but are not limited to, sun sensors, star trackers, fiber optic gyroscopes, and magnetometers. Actuators may include, but are not limited to, reaction wheels, magnetic torquers and thrusters. The non-CubeSat based products (or payload) may include, but are
20 not limited to, the battery pack, high resolution camera, high gain antenna and remote sensing instrument. The external connectors 232, 234 are disposed on a plate 236 coupled to an edge of the subsystem PCB 202 along the long edge 206 opposite to the system connectors 228, 230. The plate 236 is coupled to the subsystem PCB 202 such that the planar surface of the plate 236 is substantially perpendicular to the planar surface of the
25 subsystem PCB 202. The plate 236 is dimensioned such that when a plurality of subsystem PCBs are stacked together, the respective plates 236 of each subsystem may be joined together to collectively form a top plate of a complete satellite system.

In the exemplary embodiment, the configuration of connectors on the first planar
30 surface 212 may be replicated on the second planar surface 214 such that the motherboard PCB 202 is capable of receiving up to four CubeSat boards (i.e. two CubeSat boards on each side of the motherboard PCB 202). In some exemplary embodiments, the second planar surface may have the same configuration/ arrangement of connectors as the first planar surface for receiving daughterboard PCB(s) with the same form factor. In other
35 exemplary embodiments, the second planar surface may have different configuration/

arrangement of connectors from the first planar surface for receiving daughterboard PCB(s) with the same or different form factor(s).

FIG. 3A is a side view drawing of a satellite system 300 in an exemplary embodiment.

5 The satellite system 300 comprises a backplane PCB 302 having a planar surface. The backplane PCB 302 is a printed circuit board having a planar surface and a plurality of connectors/ slots e.g. substantially parallel slots provided on the planar surface of the backplane PCB, each slot configured for allowing a subsystem PCB to be installed thereon. The backplane PCB 302 further comprises circuitry for providing communication between a

10 plurality of subsystem PCBs that are electrically connected to the plurality of connectors.

In the exemplary embodiment, the plurality of substantially parallel connectors is in the form of a satellite bus interface 304 disposed on the planar surface of the backplane PCB 302. The satellite bus interface 304 comprises a plurality of subsystem connectors e.g.

15 306 disposed at pre-defined intervals on the planar surface of the backplane PCB 302 such that a plurality of subsystems e.g. 310, 312 can be arranged in a stacked formation and can be connected in parallel via the backplane PCB 302. The plurality of subsystem connectors e.g. 306 is configured for coupling to complementary system/backplane connectors e.g. 308 disposed on one or more satellite subsystems PCBs e.g. 310, 312 (compare 100 of FIG. 1)

20 which are installed with its respective plane being substantially perpendicular to the planar surface of the backplane PCB 302. Such a configuration may result in a compact satellite system which is amenable to adjustments, as individual subsystem PCBs can be removed or added to the backplane PCB without affecting the neighboring subsystem PCBs.

25 The satellite system 300 is configured to have satellite subsystems with varying configurations. For example, satellite subsystem 310 comprises a subsystem motherboard PCB 314 having a planar surface and a connector 316 disposed on one side of the motherboard PCB 314, said connector 316 configured for coupling to a daughterboard PCB 318. In another example, satellite subsystem 312 comprises a subsystem motherboard PCB

30 320 having a planar surface and connectors 322, 324 disposed on both sides of the subsystem motherboard PCB 320. The connectors 322, 324 are each configured for coupling to a daughterboard PCB 326, 328, respectively. The daughterboard PCB 326, 328 may be a PC104 form factor PCB or a PCB which is based on another suitable form factor.

35 FIG. 3B is a front view drawing of the satellite system 300 when viewed from the direction 330 of FIG. 3A. The backplane PCB 302 comprises a pair of subsystem connectors

306A, 306B which are configured for coupling to complementary system/backplane connectors 308A, 308B of the satellite subsystem motherboard PCB 314. The pair of subsystem connectors 306A, 306B are positioned along the same edge e.g. long edge of the satellite subsystem motherboard PCB 314 and are configured for allowing the PCB 314 to be mounted/ installed with its planar surface substantially perpendicular to the backplane PCB 302 of the satellite system 300. In the exemplary embodiment, the satellite subsystem motherboard PCB 314 has a dimension of 211.8 mm by 90.2 mm. This provides sufficient space for the satellite subsystem motherboard PCB 314 to accommodate up to either four PC104 form factor CubeSat PCBs (measuring 90.2 mm by 95.9 mm) or two PCBs with maximum dimension of 211.8mm by 90.2mm on both sides of the satellite subsystem motherboard PCB 314.

To configure the satellite system 300, the satellite subsystem motherboard PCBs of the various satellite subsystems are interconnected through the backplane PCB 302. The backplane PCB 302 may be designed to serve different bus standards such as CAN, SPI, SpaceWire, LVDS, RS-422, RS232, RS485, I2C, etc. Such a configuration removes the constraint of the PC104 form factor approach used in CubeSat satellites because subsystems may be placed in any order and there is no requirement for all the subsystems to be stacked up one over the other. With this configuration, it is possible for any subsystem to be removed or added to the satellite system 300 without the need to dismantle the existing assembled satellite. This advantageously circumvents the current CubeSat standard which limits a satellite to use only subsystems and payloads based on the PC104 form factor. Advantageously, it is possible for a manufacturer to interface the satellite system to other COTS products which are not based on the CubeSat standard, while maintaining backward compatibility to existing CubeSat-based subsystems

FIG. 4 is a front view drawing of a satellite system 400 having a first configuration in an exemplary embodiment. The satellite system 400 comprises a backplane PCB 402 having a pair of subsystem connectors 404A, 404B disposed on its planar surface. The satellite system 400 further comprises a subsystem PCB 406 coupled to the backplane PCB 402 via a pair of complementary system/ backplane connectors 408A, 408B. The system/ backplane connectors 404, 408 may be designed based on bus standards such as CAN, SPI, SpaceWire, LVDS, RS-422, RS232, RS485, I2C, etc.

In the exemplary embodiment, the subsystem PCB 406 comprises two sets of connectors e.g. 104-pin connectors 410A, 410B and mounting holes e.g. 412A, 412B that

conform to the CubeSat standard. Each set of connectors and mounting holes are configured for receiving a CubeSat subsystem daughterboard PCB, each daughterboard PCB conforming to PC104 form factor having a dimension of 90.2 mm in length by 95.9 mm in width. For example, connector 410A and mounting holes e.g. 412A are coupled to a first
5 CubeSat subsystem daughterboard 414, while connector 410B and mounting holes e.g. 412B are coupled to a second CubeSat subsystem daughterboard 416. Respective planar surfaces of the CubeSat subsystem daughterboard PCBs 414 and 416 are arranged to be substantially parallel to the planar surface of the subsystem PCB 406, when the CubeSat subsystem daughterboard PCBs 414 and 416 are electrically connected to the subsystem
10 PCB 406.

FIG. 5 is a front view drawing of a satellite system 500 having a second configuration in an exemplary embodiment. The satellite system 500 comprises a backplane PCB 502 having a pair of system connectors 504A, 504B disposed on its planar surface. The satellite
15 system 500 further comprises a subsystem PCB 506 coupled to the backplane PCB 502 via a pair of complementary system connectors 508A, 508B. The system connectors 504, 508 may be designed based on bus standards such as CAN, SPI, SpaceWire, LVDS, RS-422, RS232, RS485, I2C, etc.

20 In the exemplary embodiment, the subsystem 506 comprises two sets of connectors 510A, 510B. The connectors are configured for coupling to a customized PCB/ add-on module 512 which does not conform to the CubeSat standard. The planar surface of the customized PCB 512 is arranged to be substantially parallel to the planar surface of the subsystem PCB 506, when the customized PCB 512 is electrically connected to the
25 subsystem PCB 506. In various exemplary embodiments, the customized PCB may be configured to conform to a form factor selected from the group consisting of ESM (149 mm × 71 mm), Pico-ITX (100 mm × 72 mm), PC/104 (-Plus) (96 mm × 90 mm), ESMini (95 mm × 55 mm), SMARC (82 mm × 80 mm), Qseven (70 mm × 70 mm), mobile-ITX (60 mm × 60 mm) and CoreExpress (58 mm × 65 mm). As compared to FIG. 4, the 104-pin CubeSat
30 connector and standoffs are omitted from the planar surface of the subsystem PCB 506 for receiving the customized motherboard design to provide even more PCB real estate. This provides greater flexibility and less constraint in the design of the PCB.

FIG. 6A is a perspective view drawing of a satellite system 600 in an exemplary
35 embodiment. FIG. 6B is another perspective view drawing of the satellite system 600 in the exemplary embodiment. The satellite system 600 comprises a backplane PCB 602, a

plurality of subsystems e.g. 604, 606 installed to the backplane PCB 602 via connectors e.g. 608, 610 disposed on one planar surface of the backplane PCB 602. On a side of the satellite system 600 opposite the backplane PCB 602, a top plate 612 which is a composite structure formed from a plurality of component top plates e.g. 614, 616. Each component top plate e.g. 614, 616 is coupled to a subsystem PCB e.g. 604, 606 such that the planar surface of the component top plate is substantially perpendicular to the planar surface of the subsystem PCB. Each component top plate is also dimensioned such that multiple component top plates can be joined to one another to form a top plate. One or more external/interface connectors e.g. 618, 620 are provided on each component top plates e.g. 614, 616 on a side opposite to the backplane PCB 602. The interface connectors e.g. 618, 620 may be configured to allow for easy harnessing/ coupling to satellite sensors and actuators as well as non-CubeSat based products.

In the exemplary embodiment, the entire subsystem/payload system is housed in an aerospace-grade aluminium structure and the top plate is made of stainless steel. The satellite system 600 has a scalable configuration which allows the scaling up of the satellite size easily by expanding the backplane PCB and enclosure, such that the area of the backplane PCB is sufficiently large to accommodate the desired number of subsystem motherboard PCBs. The same design approach can be used for a 6U satellite and extended to larger satellites (e.g. 12U, 27U, etc.).

FIG. 7 is a schematic overview of a satellite system 700 in an exemplary embodiment. The satellite system 700 (compare 300 of FIG. 3) comprises a satellite bus interface 702 (compare 304 of FIG. 3) which is coupled to a backplane PCB (compare 302 of FIG. 3) and interconnects various subsystems (compare 310, 312 of FIG. 3) of the satellite system 700. The various subsystems comprise a GNSS subsystem 704, a structure and thermal control subsystem 706, and an attitude determination and control subsystem 708 which are connected to the satellite bus interface 702 via satellite bus power and interface (as shown by the arrow 710). The various subsystems further comprise a communications subsystem 712, an onboard computer 714, and an electrical power subsystem 716 which are connected to the satellite bus interface 702 via payload power and interface (as shown by the arrow 718). The onboard computer 714 and electrical power subsystem 716 are further connected to a payload 720 (as shown by the arrow 718), while the communications subsystem 712 is optionally connected to the payload 720 (as shown by the arrow 718 in dotted line 722). Each of the various subsystems may be configured on a subsystem PCB e.g. 314, 320 of FIG. 3.

In the exemplary embodiment, the GNSS subsystem 704 provides positional information of the satellite system 700 and comprises a GPS receiver 724 coupled to a GPS (Global Positioning System) antenna 726, and optionally, a high precision oscillator or
5 miniaturized atomic clock 728 component, to provide high stability clock signals to various subsystems and payloads.

The structure and thermal control subsystem 706 mechanically supports all other subsystems and functions to keep the subsystems within acceptable temperature ranges
10 during operation. The structure and thermal control subsystem 706 comprises deployment mechanisms 730 and a thermal control component 732.

The attitude determination and control subsystem 708 functions to stabilize the satellite system 700 in orbit and ensures that the satellite system 700 points in the direction it
15 is supposed to point in. The attitude determination and control subsystem 708 comprises a control algorithm 734 which is coupled to and receives input information from fine and coarse sun sensors 736, a fiber optic gyroscope 738 (optional), star trackers 740 (optional), and magnetometers and gyroscope 742. The control algorithm 734 processes the input information and provides output signals to three reaction wheels 744, three magnetic torquer
20 746, and a thruster 748.

The communication subsystem 712 provide a link to relay data findings and send commands to and from the satellite system 700. The communication subsystem 712
25 comprises a X-band 750 coupled to an antenna 752 (optional), a S-band 754 coupled to an antenna 756, and backup communication components 758.

The onboard computer 714 functions as a bridge connecting the other subsystems, supervises tasks that are done by the different subsystems and performs housekeeping and monitoring to ensure the health and status of those subsystems. The onboard computer 714
30 comprises a flight software 760, universal payload interface 762, and optionally, data storage 764.

The electrical power subsystem 716 functions to harness, store and distribute power required by the satellite system 700. The electrical power subsystem 716 comprises a
35 PCDM (power conditioning and distribution module) 766, an Array Optimizer Module (AOM) 768, a battery module 770, and is further coupled to a photovoltaic array/ solar array 772.

During normal operation, the on-board computer 714 communicates with other subsystems through the satellite bus interface 702. In the event of a fault, a user can bypass the on-board computer 714 and send command directly to any subsystem. In addition, each subsystem contains a memory device (e.g., flash or EEPROM (Electrically Erasable Programmable Read-Only Memory)) to house the subsystem default firmware. Newer firmware can be uploaded to the subsystem and stored in the memory. When required, a command is executed that allows any subsystem to perform in-orbit firmware update. Any payload 720 can be interfaced to the satellite bus through the universal payload interface 762. The interface acts as a plug and play connection. This advantageously reduces the need to redesign the interface protocol for different type of payloads resulting in reduced development time.

FIG. 8 is a schematic flowchart 800 for illustrating a method for configuring a satellite system in an exemplary embodiment. At step 802, a PCB is fabricated, said PCB having a first planar surface and a second planar surface opposite the first planar surface. At step 804, at least a first pair of connectors is fabricated on the first planar surface, each connector capable of electrically connecting a PC104 form factor PCB to the subsystem PCB, wherein the first pair of connectors on the first planar surface are fabricated in respective positions for allowing respective PC104 form factor PCBs to be spatially arranged in a side-by-side configuration when electrically connected to the subsystem PCB.

FIG. 9 is a schematic flowchart 900 for illustrating a method for configuring a satellite system. At step 902, a backplane PCB is provided, said backplane PCB comprising a planar surface; and a plurality of slots provided on the planar surface of the backplane PCB, each slot for allowing a subsystem PCB to be installed thereon. At step 904, one or more subsystems are installed to the backplane PCB via the plurality of slots; wherein the backplane PCB is configured to implement a satellite bus interface between the subsystem PCBs installed thereon; and each of the one or more subsystems is positioned with its respective plane being substantially perpendicular to the planar surface of the backplane PCB.

Before assembling the flight model of a satellite, a flat-satellite (flat-sat) is typically required for system functional testing. A flat-sat is a 2D model of the satellite where every subsystem is integrated and tested on a lab bench. In exemplary embodiments of the satellite system described herein, the flat-sat is arranged in a vertical position such that

subsystems are positioned on top of each other via the backplane PCB, instead of a horizontal position due to the special arrangement of the satellite subsystems and the use of the backplane PCB. This advantageously results in a more compact system that saves the setup space as illustrated in FIG. 12A, FIG. 12B and FIG. 12C.

5

FIG. 12A is a schematic diagram of a vertical flat-sat configuration of a satellite system 1201 and its external modules, when viewed from the side, in an exemplary embodiment. FIG. 12B is a top view of the vertical flat-sat configuration of the satellite system 1201 and its external modules when viewed from direction 1230.

10

The satellite system 1201 comprises an attitude determination and control subsystem 1202, a power conditioning and distribution module 1203, an array optimizer module 1204, a structure and thermal control subsystem 1205, an onboard computer 1206, a GNSS subsystem 1207, a communication subsystem 1208, and a commercial off-the-shelf S-band transceiver 1209. The external modules comprising reaction wheels 1210, magnetic torquers 1211, communication antenna 1212, battery pack 1213 are coupled with the satellite system 1201 via the front panel connector (compare 618 of FIG. 6B). Arrow 1214 represents a physical cable connection between the satellite system 1201 and an external module.

20

FIG. 12C is a schematic diagram of a horizontal flat-sat configuration, when viewed from the top, in a comparative example. In the horizontal flat-sat configuration, each of the attitude determination and control subsystem 1202, power conditioning and distribution module 1203 / array optimizer module 1204, structure and thermal control subsystem 1205, an onboard computer 1206 / GNSS subsystem 1207, and communication subsystem 1208 / commercial off-the-shelf S-band transceiver 1209 are lying substantially flat on a test bench together with external modules reaction wheels 1210, magnetic torquers 1211, communication antenna 1212 and battery pack 1213. Each of the satellite subsystems are interconnected via physical cable connection 1215. Each of the satellite subsystems is coupled with its respective external module via the physical cable connection 1214.

30

A comparison between the vertical flat-sat configuration as shown in FIG. 12B and the horizontal flat-sat configuration as shown in FIG. 12C shows that the vertical flat-sat configuration advantageously requires fewer physical cable connections. In particular, physical cable connections 1215 are not required in the vertical flat-sat configuration as shown in FIG. 12A and 12B.

35

Further, as may be observed from FIG. 12B and 12C, the vertical flat-sat configuration as shown in FIG. 12B takes up a smaller surface area or occupies a smaller footprint, when compared with the horizontal flat-sat configuration.

5 In the described exemplary embodiments, a configuration for satellites that are larger than 3U, in particular those that are 6U and larger, is provided. To configure a satellite, the motherboards of the various satellite subsystems are interconnected through a backplane PCB.

10 In the described exemplary embodiments, each subsystem may comprise a motherboard which can accommodate at least a pair of PC104 form factor CubeSat PCBs or two PCBs with maximum dimension of 211.8mm by 90.2mm on both sides of the motherboard. Such a configuration may overcome several limitations of existing CubeSat standards. For example, it is not required for all the subsystems to be stacked up one over
15 the other. This addresses the subsystem placement problems of small satellites that are based on the CubeSat standards, and allows any subsystems to be added or removed without having to dismantle the entire satellite.

In addition, such a configuration may allow the satellite to interface/use other non-
20 CubeSat based subsystems that have been used by other larger satellites. At the same time, it provides backward compatibility to use existing CubeSat based subsystems. This advantageously provides more flexibility for system configuration and testing.

Exemplary embodiments of the satellite system described herein also provides
25 scalability and is particularly useful for satellites that are designed for 6U or larger sized satellites (e.g. 27U). The size of a backplane PCB may be increased to allow for more PCBs (compare 314, 320 of FIG. 3) to be installed. For example, the size of a backplane PCB may be increased to allow multiple PCDM (compare 766 of FIG. 7) and AOM (compare 768 of FIG. 7) to be simultaneously installed in a satellite system to meet high power operation
30 requirement, and/or to allow additional onboard computer (compare 714 to FIG. 7) for additional system redundancy. It would be appreciated that the expansion is not limited in multiples of 3U, such that the satellite system may be expanded for 12U, 16U, 24U up to 27U satellite size.

35 Intra-satellite communication among various satellite subsystems are performed through the satellite bus interface which comprises a main and a redundant line to enhance

the reliability. In addition, data may be simultaneously sent through both the main and redundant lines to increase the communication bandwidth between subsystems. To ease the interface of the satellite bus to other actuators or sensors, the PCB of each subsystem are designed with another set of connectors mounted on an opposite edge as the backplane connectors. This allows every subsystem to have the further capability to connect to external modules.

In the described exemplary embodiments, dual backplane connectors are used to connect a backplane PCB to a subsystem PCB mounted/ installed with up to two CubeSat daughter boards side-by-side. The dual backplane connectors can be designed such that one backplane connector is reserved for power supplies while the other backplane connector is reserved for the signal lines, or both backplane connectors can be used for mixed power and signal lines. Power and signal lines are routed from the subsystem PCB to the backplane PCB. This advantageously allows the power lines to have larger conducting path, thereby reducing the power loss. The subsystem PCB design also allows two or more CubeSat subsystems to be used simultaneously. For other customized subsystem PCBs, the two 104-pin connectors and eight mounting holes can be omitted to provide more PCB real estate.

The terms "coupled" or "connected" as used in this description are intended to cover both directly connected or connected through one or more intermediate means, unless otherwise stated.

The term "form factor" as used herein describes the size, shape, and/ or component arrangement of a particular device.

The term "payload" as used herein is a general term used in the aerospace industry to describe the measurement or scientific and experimental instruments used by the satellite. For example, a payload may refer to non-CubeSat based products such as, but not limited to, a battery pack, high resolution camera, high gain antenna and remote sensing instrument.

The description herein may be, in certain portions, explicitly or implicitly described as algorithms and/or functional operations that operate on data within a computer memory or an electronic circuit. These algorithmic descriptions and/or functional operations are usually used by those skilled in the information/data processing arts for efficient description. An algorithm is generally relating to a self-consistent sequence of steps leading to a desired

result. The algorithmic steps can include physical manipulations of physical quantities, such as electrical, magnetic or optical signals capable of being stored, transmitted, transferred, combined, compared, and otherwise manipulated.

5 Further, unless specifically stated otherwise, and would ordinarily be apparent from the following, a person skilled in the art will appreciate that throughout the present specification, discussions utilizing terms such as “scanning”, “calculating”, “determining”, “replacing”, “generating”, “initializing”, “outputting”, and the like, refer to action and processes of an instructing processor/computer system, or similar electronic circuit/device/component,
10 that manipulates/processes and transforms data represented as physical quantities within the described system into other data similarly represented as physical quantities within the system or other information storage, transmission or display devices etc.

The description also discloses relevant device/apparatus for performing the steps of
15 the described methods. Such apparatus may be specifically constructed for the purposes of the methods, or may comprise a general purpose computer/processor or other device selectively activated or reconfigured by a computer program stored in a storage member. The algorithms and displays described herein are not inherently related to any particular computer or other apparatus. It is understood that general purpose devices/machines may
20 be used in accordance with the teachings herein. Alternatively, the construction of a specialized device/apparatus to perform the method steps may be desired.

In addition, it is submitted that the description also implicitly covers a computer program, in that it would be clear that the steps of the methods described herein may be put
25 into effect by computer code. It will be appreciated that a large variety of programming languages and coding can be used to implement the teachings of the description herein. Moreover, the computer program if applicable is not limited to any particular control flow and can use different control flows without departing from the scope of the invention.

30 Furthermore, one or more of the steps of the computer program if applicable may be performed in parallel and/or sequentially. Such a computer program if applicable may be stored on any computer readable medium. The computer readable medium may include storage devices such as magnetic or optical disks, memory chips, or other storage devices suitable for interfacing with a suitable reader/general purpose computer. In such instances,
35 the computer readable storage medium is non-transitory. Such storage medium also covers all computer-readable media e.g. medium that stores data only for short periods of time

and/or only in the presence of power, such as register memory, processor cache and Random Access Memory (RAM) and the like. The computer readable medium may even include a wired medium such as exemplified in the Internet system, or wireless medium such as exemplified in bluetooth technology. The computer program when loaded and executed
5 on a suitable reader effectively results in an apparatus that can implement the steps of the described methods.

The example embodiments may also be implemented as hardware modules. A module is a functional hardware unit designed for use with other components or modules.
10 For example, a module may be implemented using digital or discrete electronic components, or it can form a portion of an entire electronic circuit such as an Application Specific Integrated Circuit (ASIC). A person skilled in the art will understand that the example embodiments can also be implemented as a combination of hardware and software modules.

15 Additionally, when describing some embodiments, the disclosure may have disclosed a method and/or process as a particular sequence of steps. However, unless otherwise required, it will be appreciated the method or process should not be limited to the particular sequence of steps disclosed. Other sequences of steps may be possible. The particular order of the steps disclosed herein should not be construed as undue limitations. Unless
20 otherwise required, a method and/or process disclosed herein should not be limited to the steps being carried out in the order written. The sequence of steps may be varied and still remain within the scope of the disclosure.

Further, in the description herein, the word "substantially" whenever used is
25 understood to include, but not restricted to, "entirely" or "completely" and the like. In addition, terms such as "comprising", "comprise", and the like whenever used, are intended to be non-restricting descriptive language in that they broadly include elements/components recited after such terms, in addition to other components not explicitly recited. For an example, when "comprising" is used, reference to a "one" feature is also intended to be a reference to
30 "at least one" of that feature. Terms such as "consisting", "consist", and the like, may, in the appropriate context, be considered as a subset of terms such as "comprising", "comprise", and the like. Therefore, in embodiments disclosed herein using the terms such as "comprising", "comprise", and the like, it will be appreciated that these embodiments provide teaching for corresponding embodiments using terms such as "consisting", "consist", and the
35 like. Further, terms such as "about", "approximately" and the like whenever used, typically means a reasonable variation, for example a variation of +/- 5% of the disclosed value, or a

variance of 4% of the disclosed value, or a variance of 3% of the disclosed value, a variance of 2% of the disclosed value or a variance of 1% of the disclosed value.

Furthermore, in the description herein, certain values may be disclosed in a range.
5 The values showing the end points of a range are intended to illustrate a preferred range. Whenever a range has been described, it is intended that the range covers and teaches all possible sub-ranges as well as individual numerical values within that range. That is, the end points of a range should not be interpreted as inflexible limitations. For example, a description of a range of 1% to 5% is intended to have specifically disclosed sub-ranges 1%
10 to 2%, 1% to 3%, 1% to 4%, 2% to 3% etc., as well as individually, values within that range such as 1%, 2%, 3%, 4% and 5%. The intention of the above specific disclosure is applicable to any depth/breadth of a range.

Different example embodiments can be implemented in the context of data structure,
15 program modules, program and computer instructions executed in a computer implemented environment. A general purpose computing environment is briefly disclosed herein. One or more example embodiments may be embodied in one or more computer systems, such as is schematically illustrated in FIG. 10.

20 One or more example embodiments may be implemented as software, such as a computer program being executed within a specially configured computer system 1000, and instructing the computer system 1000 to conduct a method of an example embodiment.

The computer system 1000 comprises a computer unit 1002, input modules such as
25 a keyboard 1004 and a pointing device 1006 and a plurality of output devices such as a display 1008, and printer 1010. A user can interact with the computer unit 1002 using the above devices. The pointing device can be implemented with a mouse, track ball, pen device or any similar device. One or more other input devices (not shown) such as a joystick, game pad, satellite dish, scanner, touch sensitive screen or the like can also be connected to the
30 computer unit 1002. The display 1008 may include a cathode ray tube (CRT), liquid crystal display (LCD), field emission display (FED), plasma display or any other device that produces an image that is viewable by the user.

The computer unit 1002 can be connected to a computer network 1012 via a suitable
35 transceiver device 1014, to enable access to e.g. the Internet or other network systems such as Local Area Network (LAN) or Wide Area Network (WAN) or a personal network. The

network 1012 can comprise a server, a router, a network personal computer, a peer device or other common network node, a wireless telephone or wireless personal digital assistant. Networking environments may be found in offices, enterprise-wide computer networks and home computer systems etc. The transceiver device 1014 can be a modem/router unit
5 located within or external to the computer unit 1002, and may be any type of modem/router such as a cable modem or a satellite modem.

It will be appreciated that network connections shown are exemplary and other ways of establishing a communications link between computers can be used. The existence of any
10 of various protocols, such as TCP/IP, Frame Relay, Ethernet, FTP, HTTP and the like, is presumed, and the computer unit 1002 can be operated in a client-server configuration to permit a user to retrieve web pages from a web-based server. Furthermore, any of various web browsers can be used to display and manipulate data on web pages.

15 The computer unit 1002 in the example comprises a processor 1018, a Random Access Memory (RAM) 1020 and a Read Only Memory (ROM) 1022. The ROM 1022 can be a system memory storing basic input/ output system (BIOS) information. The RAM 1020 can store one or more program modules such as operating systems, application programs and program data.

20 The computer unit 1002 further comprises a number of Input/Output (I/O) interface units, for example I/O interface unit 1024 to the display 1008, and I/O interface unit 1026 to the keyboard 1004. The components of the computer unit 1002 typically communicate and interface/couple connectedly via an interconnected system bus 1028 and in a manner known
25 to the person skilled in the relevant art. The bus 1028 can be any of several types of bus structures including a memory bus or memory controller, a peripheral bus, and a local bus using any of a variety of bus architectures.

It will be appreciated that other devices can also be connected to the system bus
30 1028. For example, a universal serial bus (USB) interface can be used for coupling a video or digital camera to the system bus 1028. An IEEE 1394 interface may be used to couple additional devices to the computer unit 1002. Other manufacturer interfaces are also possible such as FireWire developed by Apple Computer and i.Link developed by Sony. Coupling of devices to the system bus 1028 can also be via a parallel port, a game port, a
35 PCI board or any other interface used to couple an input device to a computer. It will also be appreciated that, while the components are not shown in the figure, sound/audio can be

recorded and reproduced with a microphone and a speaker. A sound card may be used to couple a microphone and a speaker to the system bus 1028. It will be appreciated that several peripheral devices can be coupled to the system bus 1028 via alternative interfaces simultaneously.

5

An application program can be supplied to the user of the computer system 1000 being encoded/stored on a data storage medium such as a CD-ROM or flash memory carrier. The application program can be read using a corresponding data storage medium drive of a data storage device 1030. The data storage medium is not limited to being portable and can include instances of being embedded in the computer unit 1002. The data storage device 1030 can comprise a hard disk interface unit and/or a removable memory interface unit (both not shown in detail) respectively coupling a hard disk drive and/or a removable memory drive to the system bus 1028. This can enable reading/writing of data. Examples of removable memory drives include magnetic disk drives and optical disk drives. The drives and their associated computer-readable media, such as a floppy disk provide nonvolatile storage of computer readable instructions, data structures, program modules and other data for the computer unit 1002. It will be appreciated that the computer unit 1002 may include several of such drives. Furthermore, the computer unit 1002 may include drives for interfacing with other types of computer readable media.

20

The application program is read and controlled in its execution by the processor 1018. Intermediate storage of program data may be accomplished using RAM 1020. The method(s) of the example embodiments can be implemented as computer readable instructions, computer executable components, or software modules. One or more software modules may alternatively be used. These can include an executable program, a data link library, a configuration file, a database, a graphical image, a binary data file, a text data file, an object file, a source code file, or the like. When one or more computer processors execute one or more of the software modules, the software modules interact to cause one or more computer systems to perform according to the teachings herein.

30

The operation of the computer unit 1002 can be controlled by a variety of different program modules. Examples of program modules are routines, programs, objects, components, data structures, libraries, etc. that perform particular tasks or implement particular abstract data types. The example embodiments may also be practiced with other computer system configurations, including handheld devices, multiprocessor systems, microprocessor-based or programmable consumer electronics, network PCs, minicomputers,

35

mainframe computers, personal digital assistants, mobile telephones and the like. Furthermore, the example embodiments may also be practiced in distributed computing environments where tasks are performed by remote processing devices that are linked through a wireless or wired communications network. In a distributed computing environment,
5 program modules may be located in both local and remote memory storage devices.

Different example embodiments can be implemented in the context of data structure, program modules, program and computer instructions executed in a specially configured communication device. An exemplary communication device is briefly disclosed herein. One
10 or more example embodiments may be embodied in one or more communication devices e.g. 1100, such as is schematically illustrated in FIG. 11.

One or more example embodiments may be implemented as software, such as a computer program being executed within a communication device 1100, and instructing the
15 communication device 1100 to conduct a method of an example embodiment.

The communication device 1100 comprises a processor module 1102, an input module such as a touchscreen interface or a keypad 1104 and an output module such as a display 1106 on a touchscreen.
20

The processor module 1102 is coupled to a first communication unit 1108 for communication with a cellular network 1110. The first communication unit 1108 can include, but is not limited to, a subscriber identity module (SIM) card loading bay. The cellular network 1110 can, for example, be a 3G or 4G network.
25

The processor module 1102 is further coupled to a second communication unit 1112 for connection to a network 1114. For example, the second communication unit 1112 can enable access to e.g. the Internet or other network systems such as Local Area Network (LAN) or Wide Area Network (WAN) or a personal network. The network 1114 can comprise
30 a server, a router, a network personal computer, a peer device or other common network node, a wireless telephone or wireless personal digital assistant. Networking environments may be found in offices, enterprise-wide computer networks and home computer systems etc. The second communication unit 1112 can include, but is not limited to, a wireless network card or an ethernet network cable port. The second communication unit 1112 can
35 also be a modem/router unit and may be any type of modem/router such as a cable-type modem or a satellite-type modem.

It will be appreciated that network connections shown are exemplary and other ways of establishing a communications link between computers can be used. The existence of any of various protocols, such as TCP/IP, Frame Relay, Ethernet, FTP, HTTP and the like, is presumed, and the communication device 1100 can be operated in a client-server configuration to permit a user to retrieve web pages from a web-based server. Furthermore, any of various web browsers can be used to display and manipulate data on web pages.

The processor module 1102 in the example includes a processor 1116, a Random Access Memory (RAM) 1118 and a Read Only Memory (ROM) 1120. The ROM 1120 can be a system memory storing basic input/ output system (BIOS) information. The RAM 1118 can store one or more program modules such as operating systems, application programs and program data.

The processor module 1102 also includes a number of Input/Output (I/O) interfaces, for example I/O interface 1122 to the display 1106, and I/O interface 1124 to the keypad 1104.

The components of the processor module 1102 typically communicate and interface/couple connectedly via an interconnected bus 1126 and in a manner known to the person skilled in the relevant art. The bus 1126 can be any of several types of bus structures including a memory bus or memory controller, a peripheral bus, and a local bus using any of a variety of bus architectures.

It will be appreciated that other devices can also be connected to the system bus 1126. For example, a universal serial bus (USB) interface can be used for coupling an accessory of the communication device, such as a card reader, to the system bus 1126.

The application program is typically supplied to the user of the communication device 1100 encoded on a data storage medium such as a flash memory module or memory card/stick and read utilising a corresponding memory reader-writer of a data storage device 1128. The data storage medium is not limited to being portable and can include instances of being embedded in the communication device 1100.

The application program is read and controlled in its execution by the processor 1116. Intermediate storage of program data may be accomplished using RAM 1118. The

method(s) of the example embodiments can be implemented as computer readable instructions, computer executable components, or software modules. One or more software modules may alternatively be used. These can include an executable program, a data link library, a configuration file, a database, a graphical image, a binary data file, a text data file,
5 an object file, a source code file, or the like. When one or more processor modules execute one or more of the software modules, the software modules interact to cause one or more processor modules to perform according to the teachings herein.

The operation of the communication device 1100 can be controlled by a variety of
10 different program modules. Examples of program modules are routines, programs, objects, components, data structures, libraries, etc. that perform particular tasks or implement particular abstract data types.

The example embodiments may also be practiced with other computer system
15 configurations, including handheld devices, multiprocessor systems/servers, microprocessor-based or programmable consumer electronics, network PCs, minicomputers, mainframe computers, personal digital assistants, mobile telephones and the like. Furthermore, the example embodiments may also be practiced in distributed computing environments where tasks are performed by remote processing devices that are linked
20 through a wireless or wired communications network. In a distributed computing environment, program modules may be located in both local and remote memory storage devices.

In the described exemplary embodiments, each subsystem PCB is shown to have two system/backplane connectors. It will be appreciated that the number of
25 system/backplane connectors is not limited to two and there may be one or more than two system/backplane connectors.

In the described exemplary embodiments, the subsystem PCB is described as having dimensions of 211.8 mm in length by 90.2 mm in breadth. It will be appreciated that
30 the dimension of the subsystem PCB is not limited to such dimensions, as the dimensions are based on the specific requirements of each satellite system.

In the described exemplary embodiments, the pair of connectors for receiving daughterboard PCBs are described as being orientated in a substantially identical manner
35 for allowing respective daughterboard PCBs to be orientated on the subsystem PCB in a substantially identical manner relative to the subsystem PCB, when electrically connected to

the subsystem PCB. It will be appreciated that the arrangement of connectors is not limited as such, as the pair of connectors may be orientated differently from each other, e.g. one positioned along a long edge and one positioned along a short edge of the PCB, to suit specific requirements of a subsystem.

5

It will be appreciated by a person skilled in the art that other variations and/or modifications may be made to the specific embodiments without departing from the scope of the invention as broadly described. For example, in the description herein, features of different exemplary embodiments may be mixed, combined, interchanged, incorporated, adopted, modified, included etc. or the like across different exemplary embodiments. The present embodiments are, therefore, to be considered in all respects to be illustrative and not restrictive.

15

CLAIMS

1. A satellite subsystem PCB comprising
5 a first planar surface;
a second planar surface opposite the first planar surface;
at least a first pair of connectors on the first planar surface, each connector capable
of electrically connecting a PC104 form factor PCB to the subsystem PCB;
wherein the first pair of connectors are positioned on the first planar surface for
10 allowing respective PC104 form factor PCBs to be spatially arranged in a side-by-side
configuration when electrically connected to the subsystem PCB.
2. The satellite subsystem PCB according to claim 1, further comprising
a further pair of connectors on the second planar surface, each connector capable of
15 electrically connecting one PC104 form factor PCB to the subsystem PCB;
wherein the further pair of connectors are positioned on the second planar surface for
allowing respective PC104 form factor PCBs to be spatially arranged in a side-by-side
configuration when electrically connected to the subsystem PCB.
- 20 3. The satellite subsystem PCB according to claim 1 or 2, wherein the
connectors are positioned to allow respective planar surfaces of the PC104 form factor
PCBs to be substantially parallel with the first and second planar surfaces of the satellite
subsystem PCB.
- 25 4. The satellite subsystem PCB according to any one of claims 1 to 3, wherein
the pair of connectors are orientated in a substantially identical manner, for allowing
respective PC104 form factor PCBs to be orientated on the subsystem PCB in a
substantially identical manner, relative to the subsystem PCB, when electrically connected to
the subsystem PCB.
30
5. The satellite subsystem PCB according to any one of claims 1 to 4, further
comprising one or more system connectors for electrically connecting to a main satellite
system.
- 35 6. The satellite subsystem PCB according to claim 5,

wherein the one or more system connectors are positioned at a first edge of the satellite subsystem PCB for allowing the satellite subsystem PCB to be installed on the main satellite system, such that the planar surface of the satellite subsystem PCB is substantially perpendicular to a backplane PCB of the main satellite system.

5

7. The satellite subsystem PCB according to claim 5 or 6,
wherein each of the one or more system connectors comprises a plurality of pins for transmission of power and/or signals.

10

8. The satellite subsystem PCB according to claim 7,
wherein one portion of the plurality of pins is configured for transmission of power and another portion of the plurality of pins is configured for transmission of signals.

15

9. The satellite subsystem PCB according to claim 6 or 7, wherein the satellite subsystem comprises a first system connector configured for transmission of power; and a second system connector configured for transmission of signals.

20

10. The satellite subsystem PCB according to any one of claims 1 to 9, further comprising additional connectors on the first planar surface and the second planar surface,
wherein the additional connectors are positioned for receiving a customized PCB on each of the first and second planar surfaces,
wherein the customized PCB is based on a different form factor from the PC104 form factor.

25

11. The satellite subsystem PCB according to any one of claims 6 to 10,
further comprising one or more external connectors positioned at a second edge of the satellite subsystem PCB,
wherein the one or more external connectors are configured for connecting to respective one or more external modules.

30

12. The satellite subsystem PCB of claim 11, wherein the external modules consist of

35

one or more sensors selected from the group consisting of sun sensors, star tracker, fiber optic gyroscope, and magnetometer;
one or more actuators selected from the group consisting of reaction wheels, magnetic torquers and thrusters; and

one or more non-CubeSat based products selected from the group consisting of battery pack, high resolution camera, high gain antenna and remote sensing instrument.

13. The satellite subsystem PCB according to any one of claims 1 to 12, further
5 comprising one or more mounting holes for physically securing the PCB onto the subsystem PCB.

14. A method for configuring a satellite subsystem PCB, the method comprising
fabricating a PCB having a first planar surface and a second planar surface opposite
10 the first planar surface;

fabricating at least a first pair of connectors on the first planar surface, each
connector capable of electrically connecting a PC104 form factor PCB to the subsystem
PCB;

wherein the first pair of connectors on the first planar surface are fabricated in
15 respective positions for allowing respective PC104 form factor PCBs to be spatially arranged
in a side-by-side configuration when electrically connected to the subsystem PCB.

15. The method according to claim 14,
fabricating a further pair of connectors on the second planar surface, each connector
20 capable of electrically connecting one PC104 form factor PCB to the subsystem PCB;

wherein the further pair of connectors are fabricated in respective positions on the
second planar surface for allowing respective PC104 form factor PCBs to be spatially
arranged in a side-by-side configuration when electrically connected to the subsystem PCB.

25 16. A satellite system comprising,
one or more subsystem PCBs as claimed in any one of claims 1 to 13;
a backplane PCB for implementing a satellite bus interface between the one or more
subsystem PCBs, said backplane PCB comprising

a planar surface;
30 a plurality of slots provided on the planar surface of the backplane PCB, each
slot for allowing a subsystem PCB to be installed thereon;

wherein each of the one or more subsystems is installed with their respective planes
being substantially perpendicular to the planar surface of the backplane PCB.

35 17. The satellite system according to claim 16, wherein the satellite bus interface
comprises a main line and a redundant line.

18. The satellite system according to claim 16 or 17, wherein the backplane PCB is expandable to scale the form factor of the satellite system.

5 19. The satellite system according to any one of claims 16 to 18, wherein the satellite bus interface consists of one or more bus standards selected from the group consisting of CAN, I2C, SPI, SpaceWire, LVDS, RS-422, RS-232 and RS-485.

10 20. A method for configuring a satellite system, comprising
providing a backplane PCB, said backplane PCB comprising
a planar surface;
a plurality of slots provided on the planar surface of the backplane PCB, each
slot for allowing a subsystem PCB to be installed thereon;
installing one or more subsystems as claimed in any one of claims 1 to 13 to the
15 backplane PCB via the plurality of slots;
wherein the backplane PCB is configured to implement a satellite bus interface
between the subsystem PCBs installed thereon; and each of the one or more subsystems is
positioned with its respective plane being substantially perpendicular to the planar surface of
the backplane PCB.

20