INTEGRATED CIRCUITS HAVING PLACE-EFFICIENT CAPACITORS AND METHODS FOR FABRICATING THE SAME

FIELD OF THE INVENTION

[0001] The present invention generally relates to integrated circuits and methods for fabricating integrated circuits, and more particularly relates to integrated circuits having place-efficient capacitors and methods for fabricating the same.

BACKGROUND OF THE INVENTION

[0002] During front end-of-the-line processing, a plurality of semiconductor devices (e.g., transistors, resistors, and the like) are formed on a semiconductor wafer. During back end-of-the-line (BEOL) processing, a plurality of semiconductor devices are interconnected to form a plurality of integrated circuits on the wafer, which are subsequently separated into individual die during wafer dicing. Interconnection of the semiconductor devices is accomplished via the formation of a plurality of BEOL layers, which include, in part, a number of metallization layers and a number of interlayer dielectric layers (ILD layers).

[0003] Capacitors are used in many electrical and electronic devices to implement a wide variety of functions. Capacitors may be fabricated as part of the back-end-of-the-line (BEOL) process. BEOL begins when a first metallization layer is deposited on the semiconductor wafer. Back end capacitors typically require a large amount of chip area and often compete for available chip area in which transistors can be formed.

[0004] There is a continual interest in the integration density of semiconductor devices, such as capacitors, etc. on the integrated circuit. High capacitance is desired for capacitors, including DRAM storage capacitors. "Capacitance" refers to the capacity of the device for storing electric charge. One approach to increase the capacitance is to increase the area of the capacitor electrodes. Capacitance is directly proportional to the surface area of the electrodes. However, this approach results in an increase in the actual area occupied by the capacitor on the integrated circuit or an increase in the size of the chip (the integrated circuit). Neither of these options is desirable as increasing the actual area occupied by the capacitor excludes other semiconductor devices and an increase in the chip size undermines the interest toward integration density.

[0005] Accordingly, it is desirable to provide integrated circuits having a capacitor with increased capacitance per unit area (i.e., a "place-efficient capacitor") and methods for

fabricating the same. It is also desired to increase the capacitance of the capacitor without occupying more chip space or increasing the size of the integrated circuit to enable an increase in the number of semiconductor devices integrated on a given area of the integrated circuit. Furthermore, other desirable features and characteristics of the present invention will become apparent from the subsequent detailed description of the invention and the appended claims, taken in conjunction with the accompanying drawings and this background of the invention.

BRIEF SUMMARY OF THE INVENTION

[0006] Methods for fabricating integrated circuits having place-efficient capacitors are provided. In accordance with one exemplary embodiment, the method includes forming a dielectric layer overlying a conductive feature on a semiconductor substrate. A via opening is formed into the dielectric layer to expose a portion of the conductive feature. A partial opening is etched into the dielectric layer and positioned over the conductive feature. Etch resistant particles are deposited overlying the dielectric layer and in the partial opening. The dielectric layer is further etched using the etch resistant particles as an etch mask to extend the partial opening. A first conductive layer is formed overlying the extended partial opening and electrically contacting the conductive feature. A capacitor insulating layer is formed overlying the first conductive layer. A second conductive layer is formed overlying the insulating layer.

[0007] Methods for fabricating integrated circuits having place-efficient capacitors are provided in accordance with yet another exemplary embodiment of the present invention. The method includes forming a dielectric layer overlying a conductive feature on a semiconductor substrate. A via opening is formed in the dielectric layer to expose a portion of the conductive feature. The via opening is filled with an organic planarization layer (OPL) material. The dielectric layer is etched to form a partial opening positioned over the conductive feature. Etch-resistant particles are deposited over the dielectric layer in the partial opening. The dielectric layer is further etched around the etch-resistant particles to extend the partial opening forming an extended partial opening. The etch-resistant particles and the OPL material within the via opening are removed. A lower capacitor electrode is formed, for example from a metal liner, within the via opening and the extended partial opening. A capacitor insulating layer is formed overlying the metal liner. An upper

capacitor electrode is formed filling the via opening and the extended partial opening with a metal fill material.

[0008] Integrated circuits having a place-efficient capacitor are provided in accordance with yet another exemplary embodiment of the present invention. The integrated circuit includes a lower capacitor electrode having a surface area that includes an inner surface area of an extended partial opening and a via opening formed in a patterned dielectric layer on a semiconductor substrate. A capacitor insulating layer overlies the lower capacitor electrode. An upper capacitor electrode metal fill material fills the extended partial opening and the via opening and has a surface area that includes the inner surface area of the extended partial opening and via opening.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The present invention will hereinafter be described in conjunction with the following drawing figures, wherein like numerals denote like elements, and

[0010] FIG. 1 is a flow diagram of a method for fabricating an integrated circuit, according to exemplary embodiments of the present invention;

[0011] FIG. 2 illustrates, in cross-section, a portion of an exemplary initial integrated circuit; and

[0012] FIGS. 3 to 14 illustrate, in cross section, the initial integrated circuit matriculating through various stages of forming a place-efficient capacitor in a back end of line phase of an integrated circuit fabrication process.

DETAILED DESCRIPTION OF THE INVENTION

[0013] The following detailed description of the invention is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. Furthermore, there is no intention to be bound by any theory presented in the preceding background of the invention or the following detailed description of the invention.

[0014] Various embodiments are directed to integrated circuits having place-efficient capacitors and methods for fabricating the same. As used herein and noted previously, "place-efficient capacitors" are capacitors with increased capacitance per unit area. Etch-resistant particles are used as patterning agents to introduce porosity to a dielectric layer of the integrated circuit to increase the effective area between capacitor electrodes, thereby increasing the capacitor capacitance, without the capacitor occupying more area on the

integrated circuit or increasing the size of the integrated circuit. A place-efficient capacitor frees up available space on the integrated circuit for other semiconductor devices, thereby improving the economics of integrated circuit fabrication.

[0015] Referring now to FIG. 1, a method 10 for fabricating an integrated circuit having a place-efficient capacitor begins by providing an integrated circuit 12 (step 20). The initial integrated circuit is made using standard semiconductor processing that is well known in the art. FIG. 2 illustrates an exemplary initial integrated circuit including a semiconductor substrate 14, a dielectric layer 16 on the semiconductor substrate (dielectric layer 16 is an interlayer dielectric (ILD)), at least one conductive feature 18 formed in the dielectric layer with the dielectric layer formed overlying the conductive feature, and a first photoresist layer 22 overlying a top surface of the dielectric layer for purposes as hereinafter described. The dielectric layer is formed of dielectric materials as well known in the art. For ease of illustration, the dielectric layer and first photoresist layer are each shown as a single layer, but it is to be understood that there may be additional dielectric and/or photoresist layers as well as other layers (not shown) such as, for example, anti-reflective coating (ARC) layers, organic planarization layers (OPL), or the like. The semiconductor substrate is made of a semiconductor material such as monocrystalline silicon, polycrystalline silicon, silicon-germanium, or the like and may include insulating layers, diffusion barrier layers, conductive layers, and the like as well as circuitry and other structures including one or more semiconductor devices such as transistors, capacitors, resistors, and the like (not shown). For simplicity, the semiconductor substrate will not be shown in subsequent drawings. The conductive feature may be formed from a metal such as copper, tungsten, aluminum, silver, gold, or other conductive metal, and the like. The conductive feature may be connected to other underlying features (not shown), such as other metal lines, vias, contact plugs, or silicide regions of MOS devices.

[0016] Referring to FIGS. 3 and 4, using known lithography processes, the first photoresist layer 22 is formed and patterned for a first opening 24 for an interconnect structure (e.g., a via) in the dielectric layer. A via opening 26 is formed in the dielectric layer where the place-efficient capacitor 48 (FIG. 14) is to be formed and to expose the conductive feature. The via opening is formed by etching the dielectric layer using an etching process such as, for example, a reactive ion etch (RIE). An etch stop layer, not illustrated, may be used to facilitate the etching of the via opening. Still referring to FIG. 4, the first photoresist layer is removed and the substrate is re-cleaned.

[0017] Referring now to FIGS. 5 through 7, an organic planarization layer (OPL) 28 is formed overlying the dielectric layer including filling the via opening 26. The OPL layer planarizes the top surface of the integrated circuit for a second photoresist layer 32 to be formed over a top surface of the organic planarization layer. Using known lithography processes, a second opening 34 is formed and patterned in the second photoresist and OPL layers (FIG. 6), thereby removing OPL material in an upper portion of the via opening. The OPL layer may be formed of known OPL materials.

[0018] Referring specifically to FIG. 7, a partial opening (e.g., a trench) 36 is etched into the dielectric layer and positioned over the conductive feature (step 25 in FIG. 1). The dielectric layer 16 is partially etched stopping just below the top surface of the dielectric layer to form the partial opening 36. The partial opening is formed at the top of the via opening and transverse thereto. The partial opening is formed where a subsequently-formed first conductive layer serves as a bottom capacitor electrode, as hereinafter described. The partial opening is anisotropically etched using, for example, $C_4F_6/Ar/O_2$ etch chemistry.

[0019] Referring now to FIG. 8, method 10 continues by depositing etch resistant particles 38 overlying the second photoresist layer 32 and the dielectric layer in the partial opening (step 30 in FIG. 1). The etch-resistant particles serve as a non-continuous etch resistant mask (i.e., a porosity mask) leaving space on the exposed top surface of the dielectric layer in the partial opening corresponding to locations where the underlying dielectric material is to be etched, as hereinafter described. In all other regions, the etch-resistant particles physically block the etchant. As used herein, the term "etch-resistant particles" refers to an etch-resistant porous layer or distributed particles. The etch-resistant porous layer may be a porous polymer layer (e.g., OPL-like materials with open porosity induced by methods well known in the art). The distributed particles may be organic or inorganic particles such as, for example, platinum (Pt), gold (Au), carbon (C), or combinations thereof. The organic and inorganic particles may be self-assembling. The organic and inorganic particles have a size range between about 2 nm to about 150 nm, preferably about 5 to about 70 nm. The organic and inorganic particles are deposited in a manner to distribute them substantially equally over about 20% to about 60% of the area. As used herein, "distribute" refers to spreading out or scattering. The pores of the porous layer are similarly distributed.

[0020] Referring to FIGS. 9 and 10, method 10 continues by further etching the dielectric layer using the etch resistant particles and the second photoresist layer as an etch mask to extend the partial opening deeper into the dielectric layer 16 forming an extended partial

opening 52 (step 40 in FIG. 1). By etching the dielectric layer using the etch resistant particles as an etch mask, an irregular surface of increased surface area is created. The extended partial opening 52, as illustrated, includes at least first and second portions 54 and 56, separated by the via opening 26. Of course, depending on the density of the deposited etch resistant particles, other portions similar to portions 54 and 56 can be created forming an etch pattern. The etch-resistant particles can be smaller than the resolution limit of normal photolithography and consequently create an etched pattern having greater resolution than could be obtained by conventional photolithography. Etching around the etch-resistant particles is performed utilizing a wet etchant to extend the partial opening and increase the area thereof forming the extended partial opening, thereby increasing the effective area for metallization as hereinafter described. The material for the OPL layer in the via opening is selected to be substantially etch-resistant to the etchant selected to etch the dielectric layer. After completing the further etching step, the integrated circuit appears as illustrated in FIG. 9. The regions below the etch-resistant particles (i.e., in their shadow) are either not etched, or etched less intensively. The dielectric layer is etched around the etch-resistant particles to introduce porosity into the surface of the dielectric layer increasing the effective capacitor area without occupying more space on the integrated circuit. The etch pattern may be ideal, as shown in FIG. 9, or chaotic.

[0021] After the further etching step is completed, the etch-resistant particles, the residual second photoresist layer, and the OPL layer including within the via opening are removed to leave a patterned dielectric layer 42 that is roughened with increased surface area as illustrated in FIG. 10. As noted previously, the patterned dielectric layer has increased porosity and roughness and therefore an increased active area in the extended partial opening 52 and via opening relative to the pre-etched dielectric layer.

[0022] Referring now to FIG. 11, method 10 continues by forming a first conductive layer 44 overlying the dielectric layer including within the extended partial opening 52 and via opening 26 and contacting conductive feature 18 (step 50 in FIG. 1). The first conductive layer may be a diffusion barrier layer. The first conductive layer simultaneously serves as a metal liner for the partial opening (e.g., a trench) and via opening and will constitute a lower capacitor electrode 58 (See FIG. 14). The metal liner has a thickness of about 5 nm to about 20 nm, and is formed of a conductive material such as, for example, titanium, titanium-nitride, or the like. The surface area of the lower capacitor electrode includes the irregular surface area of the extended partial opening and the inner surface area of the via opening.

[0023] Referring to FIG. 12, method 10 continues with forming a capacitor insulating layer 46 overlying the first conductive layer 44 including within the extended partial opening and via opening (step 60 in FIG. 1). The capacitor insulating layer may be formed from insulators as known in the art. The place-efficient capacitor 48 (FIG. 14) includes the lower capacitor electrode and an upper capacitor electrode separated by the capacitor insulating layer, as hereinafter described.

[0024] Referring to FIGS. 13 and 14, method 10 continues with forming a second conductive layer 49 overlying the capacitor insulating layer 46 including filling the extended partial opening and via opening (step 70 in FIG. 1). The second conductive layer is a metal layer formed of a metal fill material such as, for example, copper, tungsten, aluminum, silver, gold, and the like. For ease of illustration, the second conductive layer 49 is shown as a single layer, but it is to be understood that there may be additional metal layers that may be formed in multiple steps. The metal fill material in the extended partial opening and the via opening forms the upper plate of the capacitor (i.e., an upper capacitor electrode 62). The excess metal is removed, for example, by a chemical mechanical planarization (CMP) process as known in the art to remove metal overfill forming the upper capacitor electrode 62 of the place-efficient capacitor 48 (FIG. 14). As the surface area of the partial opening has been increased by use of the etch-resistant particles, the metallization area within the extended partial opening has been increased, thereby increasing the surface area of the lower and upper capacitor electrodes and increasing capacitor capacitance. The surface area of the upper capacitor electrode includes the inner surface area of the extended partial opening and via opening. The integrated circuit having the place-efficient capacitor can be integrated into a multi-level metallization package. Thereafter, standard processes may be used to complete fabrication and packaging of the integrated circuit.

[0025] From the foregoing, it is to be appreciated that the integrated circuit having a place-efficient capacitor fabricated in accordance with exemplary embodiments achieves significantly higher capacitance per unit area on the integrated circuit. The effective area between the capacitor electrodes is increased, enabling more efficient use of the chip area, particularly useful for high density DRAM arrays. The effective capacitor area is increased without occupying more chip space by increasing the surface area of the dielectric layer between the capacitor electrodes. A higher number of semiconductor devices may be integrated on a given area of the integrated circuit or higher capacitance can be achieved for a single semiconductor device.

[0026] While at least one exemplary embodiment has been presented in the foregoing detailed description of the invention, it should be appreciated that a vast number of variations exist. It should also be appreciated that the exemplary embodiment or exemplary embodiments are only examples, and are not intended to limit the scope, applicability, or configuration of the invention in any way. Rather, the foregoing detailed description will provide those skilled in the art with a convenient road map for implementing an exemplary embodiment of the invention, it being understood that various changes may be made in the function and arrangement of elements described in an exemplary embodiment without departing from the scope of the invention as set forth in the appended claims and their legal equivalents.

CLAIMS

What is claimed is:

1. A method for fabricating an integrated circuit having a place-efficient capacitor comprising:

forming a dielectric layer overlying a conductive feature on a semiconductor substrate;

forming a via opening into the dielectric layer to expose a portion of the conductive feature;

etching a partial opening into the dielectric layer and positioned over the conductive feature;

depositing etch resistant particles overlying the dielectric layer and in the partial opening;

further etching the dielectric layer using the etch resistant particles as an etch mask to extend the partial opening;

forming a first conductive layer overlying the extended partial opening and electrically contacting the conductive feature;

forming a capacitor insulating layer overlying the first conductive layer; and

forming a second conductive layer overlying the insulating layer.

2. The method of claim 1, wherein forming a via opening into the dielectric layer comprises:

forming and patterning an opening in a first photoresist layer; and

etching the via opening.

3. The method of claim 1, further comprising after the forming a via opening and before etching a partial opening:

forming an organic planarization layer (OPL) overlying the dielectric layer including filling the via opening;

forming a second photoresist layer on the organic planarization layer (OPL); and

forming and patterning a second opening in the second photoresist layer and OPL layer.

4. The method of claim 1, wherein depositing etch resistant particles comprises depositing etch resistant particles from the group selected from porous polymers, organic or inorganic particles, and combinations thereof.

5. The method of claim 1, wherein depositing etch resistant particles comprises depositing etch resistant particles to distribute the etch resistant particles overlying the dielectric layer and in the partial opening.

6. The method of claim 1, wherein further etching comprises further etching an ideal or chaotic etch pattern into the dielectric layer.

7. The method of claim 1, wherein forming a first conductive layer comprises forming a metal liner.

8. The method of claim 7, wherein forming a first conductive layer comprises forming a lower capacitor electrode having an irregular surface area of the extended partial opening and via opening.

9. The method of claim 1, wherein forming a second conductive layer overlying the insulating layer comprises forming a metal layer overlying the insulating layer including filling the extended partial opening with a metal fill material.

10. A method for fabricating an integrated circuit having a place-efficient capacitor comprising:

forming a dielectric layer overlying a conductive feature on a semiconductor substrate;

forming a via opening into the dielectric layer to expose a portion of the conductive feature;

filling the via opening with an organic planarization layer (OPL) material;

etching the dielectric layer to form a partial opening positioned over the conductive feature;

depositing etch-resistant particles over the dielectric layer in the partial opening;

further etching the dielectric layer around the etch-resistant particles to extend the partial opening forming an extended partial opening;

removing the etch-resistant particles and the OPL material within the via opening;

forming a lower capacitor electrode comprising a metal liner within the via opening and the extended partial opening;

forming a capacitor insulating layer overlying the metal liner; and

forming an upper capacitor electrode comprising filling the via opening and the extended partial opening with a metal fill material.

11. The method of claim 10, wherein forming a via opening into the dielectric layer comprises:

forming and patterning an opening in a first photoresist layer; and

etching the via opening.

12. The method of claim 10, further comprising after filling the via opening and before etching the dielectric layer:

forming a second photoresist layer on the OPL material; and

forming and patterning a second opening in the second photoresist layer and OPL layer, the partial opening extending the second opening.

13. The method of claim 10, wherein etching the dielectric layer to form a partial opening comprises etching to form a partial opening transverse to the via opening.

14. The method of claim 10, wherein depositing etch resistant particles comprises depositing etch resistant particles from the group selected from porous polymers, organic or inorganic particles, and combinations thereof.

15. The method of claim 14, wherein depositing etch resistant particles comprises depositing etch-resistant inorganic particles selected from the group consisting of platinum, gold, carbon, and combinations thereof.

16. The method of claim 14, wherein depositing etch resistant particles comprises depositing etch resistant particles with an area coverage of about 20% to about 60%.

17. The method of claim 10, wherein further etching comprises further etching an ideal or chaotic etch pattern into the dielectric layer.

18. The method of claim 10, wherein forming a lower capacitor electrode comprises forming the lower capacitor electrode having an irregular surface area of the extended partial opening and via opening.

19. The method of claim 10, wherein forming an upper capacitor electrode comprises forming a metal layer overlying the capacitor insulating layer including filling the via opening and the extended partial opening with the metal fill material of the metal layer.

20. An integrated circuit having a place-efficient capacitor comprising:

a lower capacitor electrode having a surface area comprised of an inner surface area of a extended partial opening and a via opening formed in a patterned dielectric layer on a semiconductor substrate;

a capacitor insulating layer overlying the lower capacitor electrode; and

an upper capacitor electrode comprising a metal fill material filling the extended partial opening and the via opening and having a surface area comprised of the inner surface area of the extended partial opening and via opening.