CLAIMS

1. A quantizer device, the quantizer device comprising,

a plurality of comparators for coupling to an integrator output of an integrator stage of a signal modulator, the plurality of comparators to perform multi-bit quantization of the integrator output;

a feedback loop connection coupled to outputs of the plurality of comparators and coupled to an input of the integrator stage, the feedback loop connection for transmitting quantized outputs of the plurality of comparators as a comparator feedback signal to the input of the integrator stage;

a digital-to-analog converter disposed within the feedback loop connection to perform digital-to-analog conversion of the quantized outputs of the plurality of comparators to generate the comparator feedback signal; and

a gain stage disposed within the feedback loop connection to provide a gain to the comparator feedback signal.

2. The quantizer device as claimed in claim 1, the quantizer device further comprising a digital logic component coupled to the plurality of comparators, the digital logic component to receive the quantized outputs of the plurality of comparators and the digital logic component disposed to provide a final output of the quantizer device.

3. The quantizer device as claimed in claim 2, wherein the digital logic component comprises one or more state-machine based digital logic gates and the digital logic component is capable of utilising the quantized outputs of the plurality of comparators to change a state of the one or more state-machine based digital logic gates to perform digital integration and dynamic element matching (DEM) within the digital logic component.

4. The quantizer device as claimed in claim 3, wherein the DEM is based on CLA (Clocked Level Averaging), and wherein the digital logic component comprises a plurality of cyclic shift registers each clocked by a gated clock, the gated clock based on the quantized outputs of the plurality of comparators.

5. The quantizer device as claimed in claim 4, wherein the digital logic component further comprises a digital member to process a state difference of the plurality of cyclic shift registers to produce a final N-bit output of the quantizer device.

6. The quantizer device as claimed in claim 5, wherein the digital member is a XOR gate.

7. The quantizer device as claimed in claim 3, wherein the DEM is based on DWA (Data Weighted Averaging), and wherein the digital logic component comprises a plurality of unit cells, each unit cell coupled to the quantized outputs of the plurality of comparators and each unit cell clocked based on a system clock signal, wherein data in the unit cells undergo digital integration based on the quantized outputs of the plurality of comparators.

8. The quantizer device as claimed in claim 7, wherein the unit cells are coupled to each other in an ordered manner, each unit cell capable of outputting data from a previous-ordered unit cell or from a next-ordered unit cell or its own data, each unit cell output being dependent on the quantized outputs of the plurality of comparators.

9. The quantizer device as claimed in claim 8, wherein the digital logic component further comprises a DWA-DEM generation element that is disposed to generate a DEM pattern based on a current/present state of the each unit cell output.

10. The quantizer device as claimed in claim 9, wherein the DWA-DEM generation element comprises a plurality of multiplexer units connected in series.

11. The quantizer device as claimed in claim 1, wherein the plurality of comparators each have an input coupled to a single voltage reference and the multi-bit quantization of the integrator output is performed based on the single voltage reference.

12. A method of quantizing a signal, the method comprising,

inputting a signal into a sigma delta modulator;

coupling a plurality of comparators to an integrator output of an integrator stage of the modulator;

performing multi-bit quantization of the integrator output using the plurality of comparators;

providing a feedback of quantized outputs of the plurality of comparators to an input of the integrator stage, the quantized outputs of the plurality of comparators being a comparator feedback signal to the input of the integrator stage;

performing digital-to-analog conversion of the quantized outputs of the plurality of comparators to generate the comparator feedback signal; and

providing a gain to the comparator feedback signal.

13. The method as claimed in claim 12, the method further comprising coupling a digital logic component to the plurality of comparators, receiving the quantized outputs of the plurality of comparators into the digital logic component and using the digital logic component to provide a final output of the quantizer device.

14. The method as claimed in claim 13, the method further comprising utilising the quantized outputs of the plurality of comparators to change a state of one or more state-machine based digital logic gates of the digital logic component to perform digital integration and dynamic element matching (DEM) within the digital logic component.

15. The method as claimed in claim 14, wherein the DEM is based on CLA (Clocked Level Averaging), and the method further comprises clocking a plurality of cyclic shift registers of the digital logic component, with each clocked by a gated clock, the gated clock based on the quantized outputs of the plurality of comparators.

16. The method as claimed in claim 15, the method further comprising processing a state difference of the plurality of cyclic shift registers to produce a final N-bit output of the quantizer device using a digital member of the digital logic component.

17. The method as claimed in claim 14, wherein the DEM is based on DWA (Data Weighted Averaging), and the method further comprises coupling a plurality of unit cells of the digital logic component, each coupled to the quantized outputs of the plurality of comparators; clocking each unit cell based on a system clock signal, wherein data in the unit cells undergo digital integration based on the quantized outputs of the plurality of comparators.

18. The method as claimed in claim 17, further comprising coupling the unit cells to each other in an ordered manner, each unit cell capable of outputting data from a previous-ordered unit cell or from a next-ordered unit cell or its own data, each unit cell output being dependent on the quantized outputs of the plurality of comparators.

19. The method as claimed in claim 18, further comprising using a DWA-DEM generation element of the digital logic component to generate a DEM pattern based on a current/present state of the each unit cell output.

20. The method as claimed in claim 12, further comprising coupling an input of each of the plurality of comparators to a single voltage reference and performing the multi-bit quantization of the integrator output based on the single voltage reference.

5