

(21) International Application Number: PCT/US94/04304

(22) International Filing Date: 19 April 1994 (19.04.94)

(30) Priority Data:
9308141.2 20 April 1993 (20.04.93) GB
9311560.8 4 June 1993 (04.06.93) GB

(71) Applicant (for all designated States except US): RCA THOMSON LICENSING CORPORATION [US/US]; CN 5312, Two Independence Way, Princeton, NJ 08540 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): SAUER, Donald, Jon [US/US]; 8 Twan Drive, Allentown, NJ 08501 (US). RODDA, William [US/US]; 10 Surrey Drive, Trenton, NJ 08690 (US). CAMPBELL, Edward, Richard, III [US/US]; 356 Tuckerton Road, Tabernacle, NJ 08088 (US).

(74) Agents: TRIPOLI, Joseph, S. et al.; GE & RCA Licensing Management Operation, Inc., CN 5312, Princeton, NJ 08540 (US).

(81) Designated States: AT, AU, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, ES, FI, GB, HU, JP, KP, KR, KZ, LK, LU, LV, MG, MN, MW, NL, NO, NZ, PL, PT, RO, RU, SD, SE, SK, UA, US, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published

Without international search report and to be republished upon receipt of that report.

REPLACED SHEETS SG

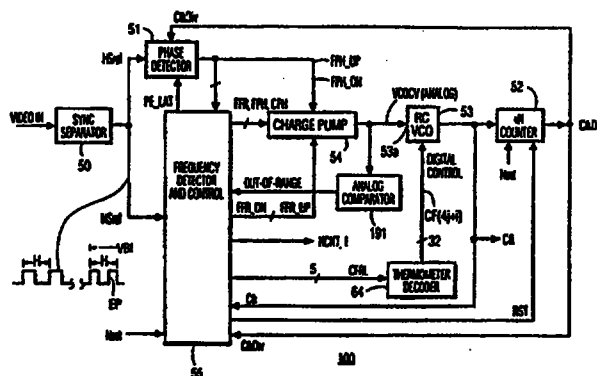
☒ Description : paged ...1... to paged ...24...
☒ Claim(s) : paged ...27... to paged ...28...
☒ Drawing(s) : paged ...4/5... to paged ...6/6...
☒ Abstract : paged ...4/1... to paged ...4/1...

DATE OF RECEIPT

(54) Title: A PHASE LOCK LOOP WITH IDLE MODE OF OPERATION DURING VERTICAL BLANKING

(57) Abstract

A frequency detector of a phase-lock-loop circuit is used for measuring a frequency error between a frequency of an output signal of an oscillator and a frequency of a synchronizing signal. When the frequency error in each of 32 periods of the synchronizing signal exceeds a predetermined magnitude, the phase-lock-loop circuit begins operating in a coarse frequency correction mode. As long as the 32 periods have not lapsed, the phase-lock-loop circuit operates in an idle mode of operation and the oscillator is not corrected. As a result, during vertical retrace, when equalizing pulses occur, the phase-lock-loop circuit is not disturbed by a large frequency error.



This Sheet Has Been Replaced

