FIG. 1

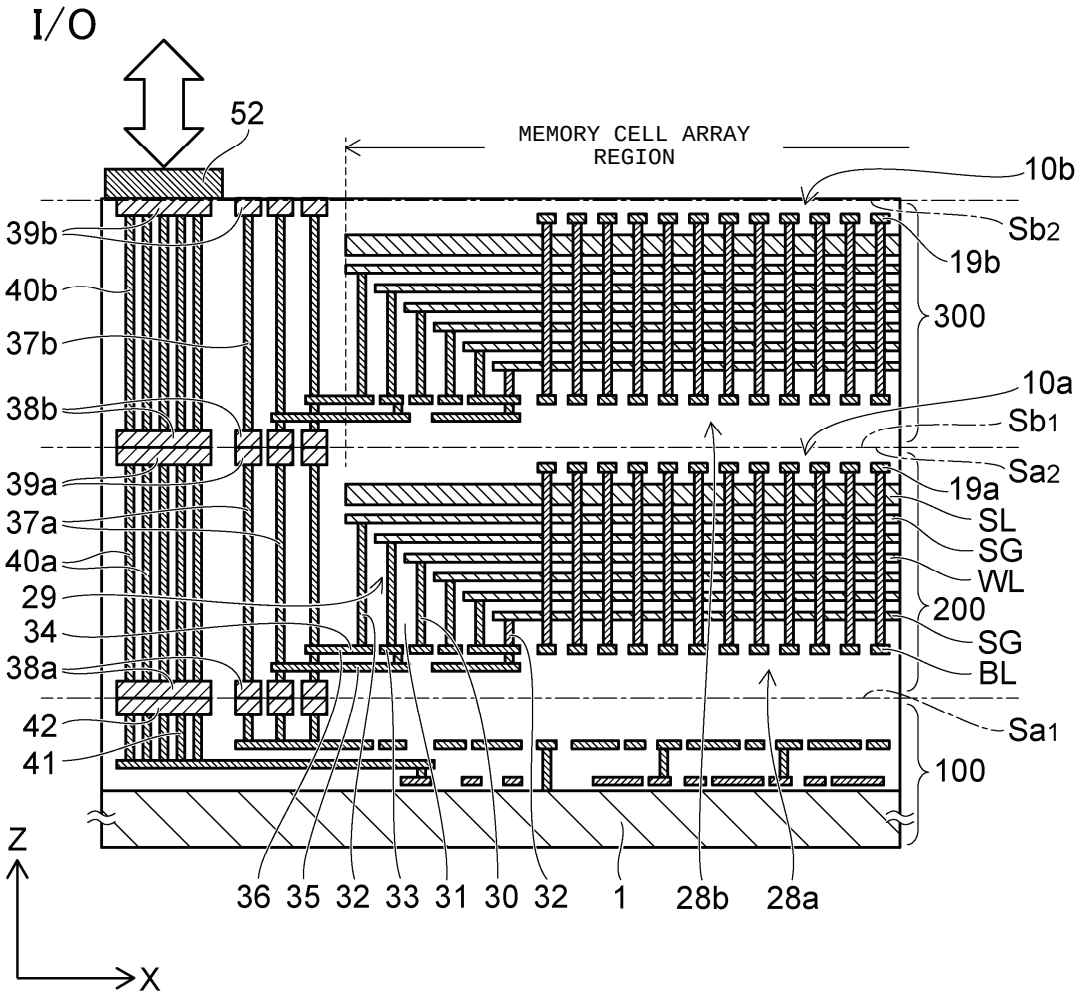

I/O
52
MEMORY CELL ARRAY REGION
10b
Sb2
19b
300
10a
Sb1
Sa2
19a
SL
SG
WL
200
SG
BL
Sa1
100
39b
40b
37b
38b
39a
37a
40a
29
34
38a
42
41
36
35
32
33
31
30
32
1
28b
28a
Z
X

FIG. 2

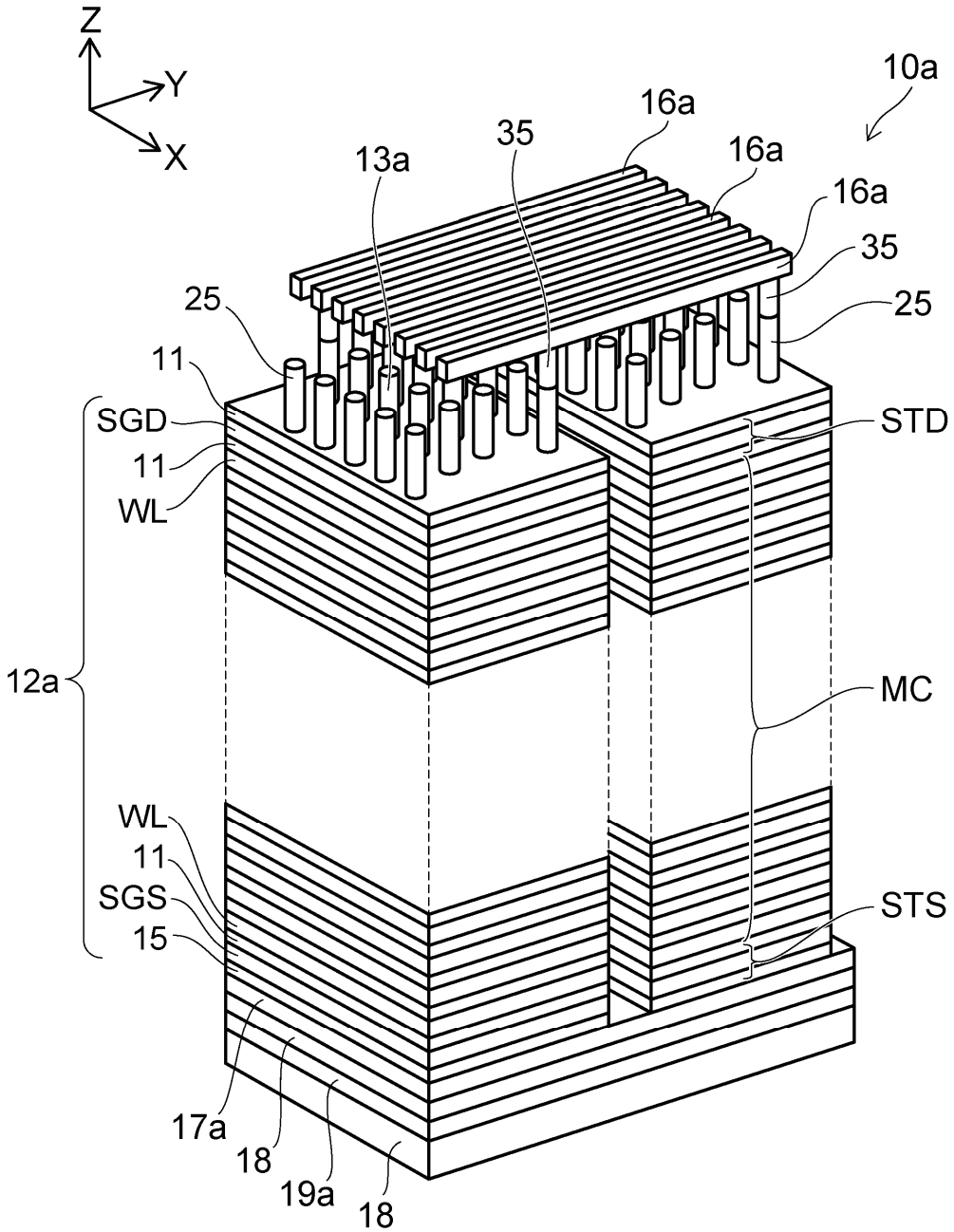

Z
Y
X
10a
16a
35
13a
16a
16a
35
25
25
11
SGD
STD
11
WL
12a
MC
WL
11
SGS
STS
15
17a
18
19a
18

FIG. 3

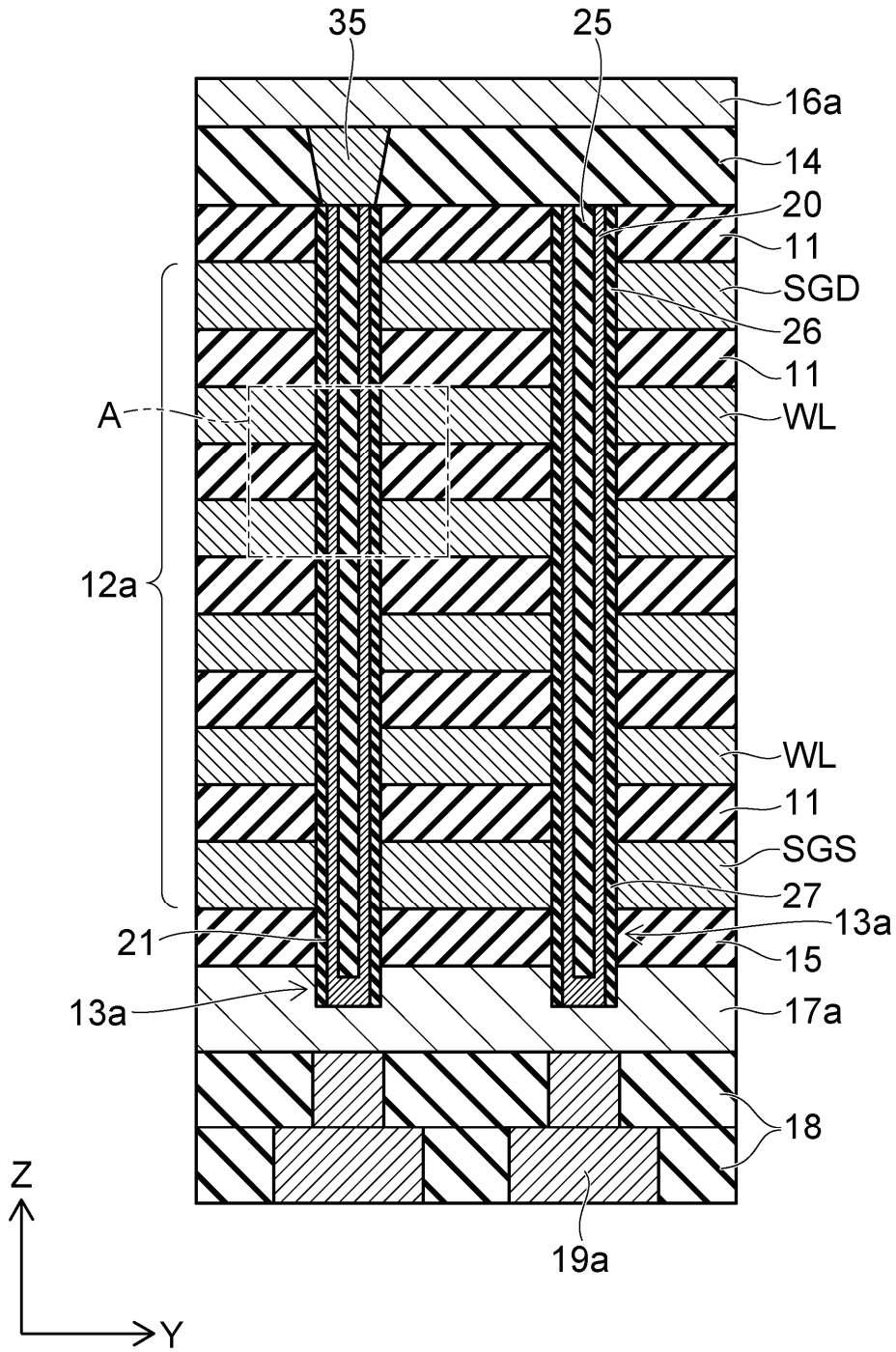

35
25
16a
14
20
11
SGD
26
11
A
WL
12a
WL
11
SGS
27
13a
21
15
13a
17a
18
19a
Z
Y

FIG. 4

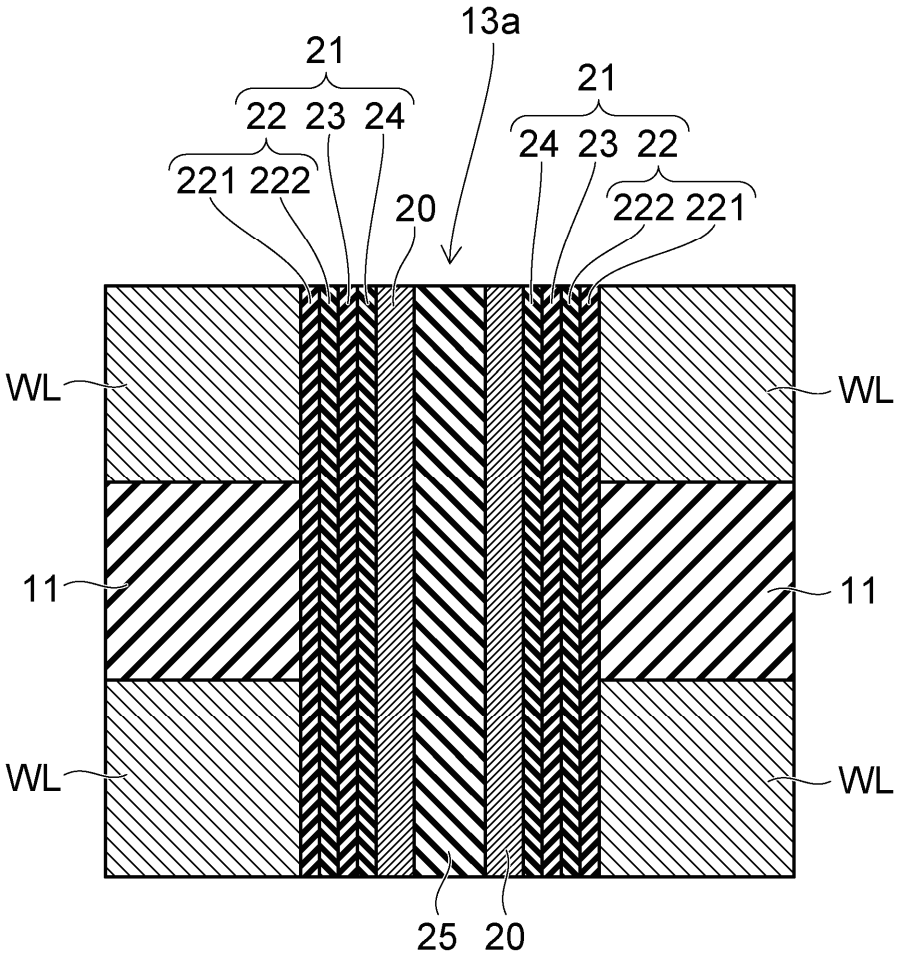


FIG. 5

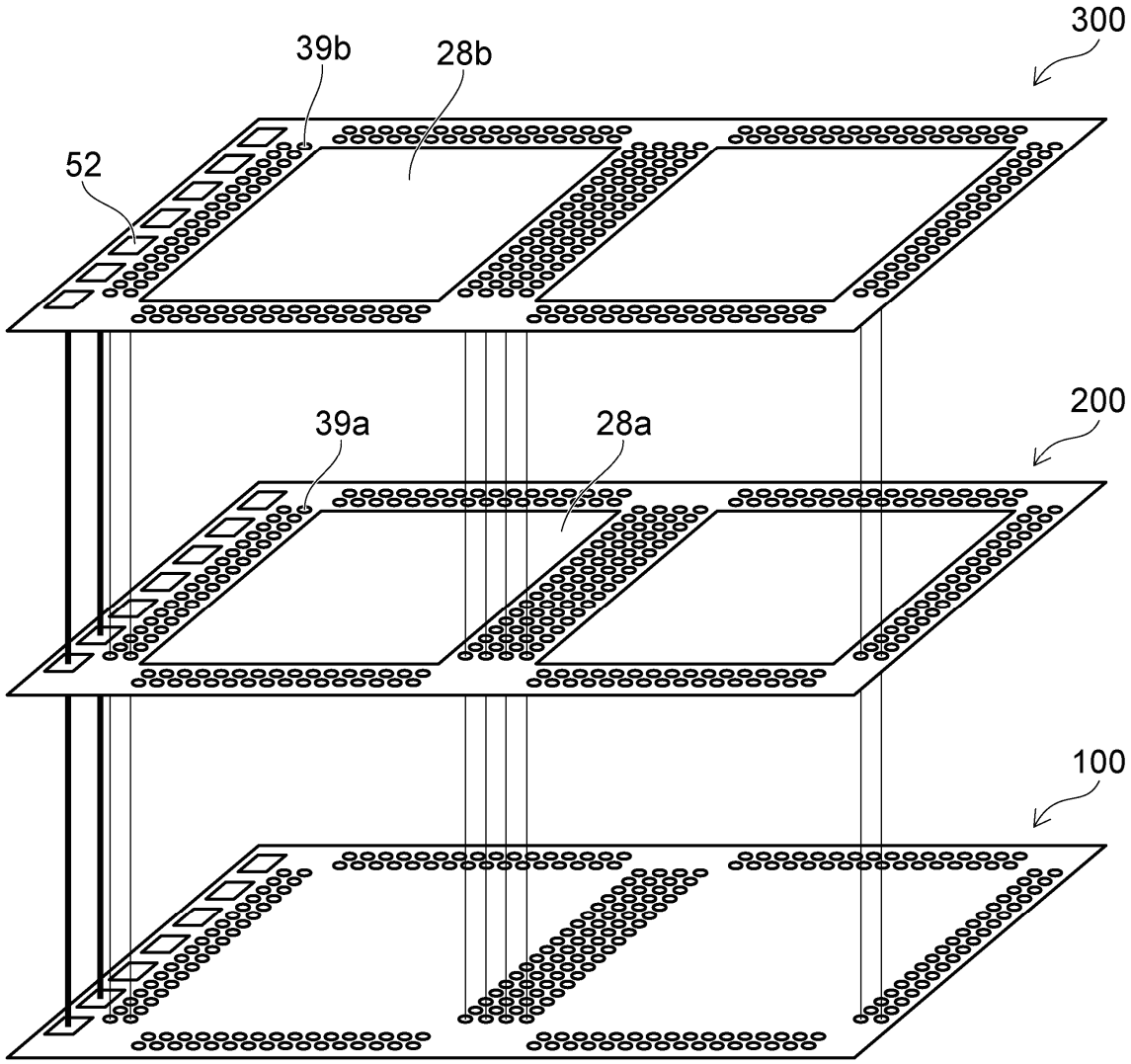


FIG. 6

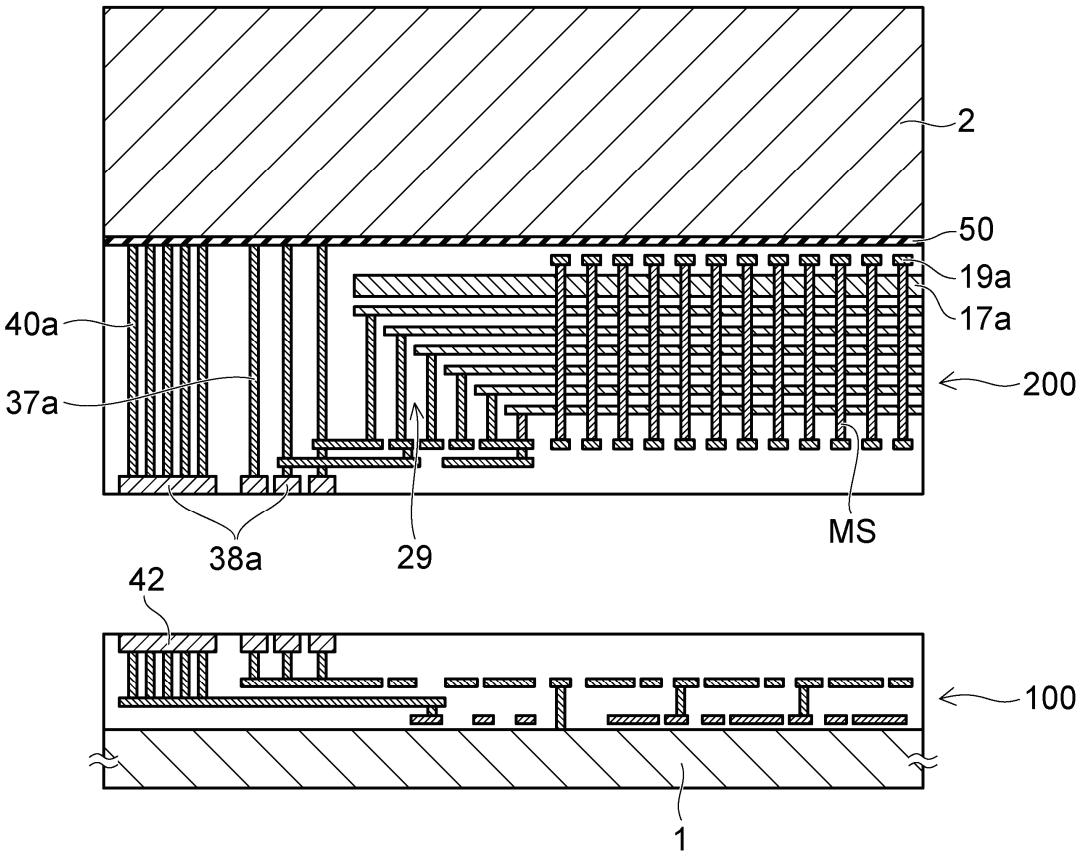



FIG. 7

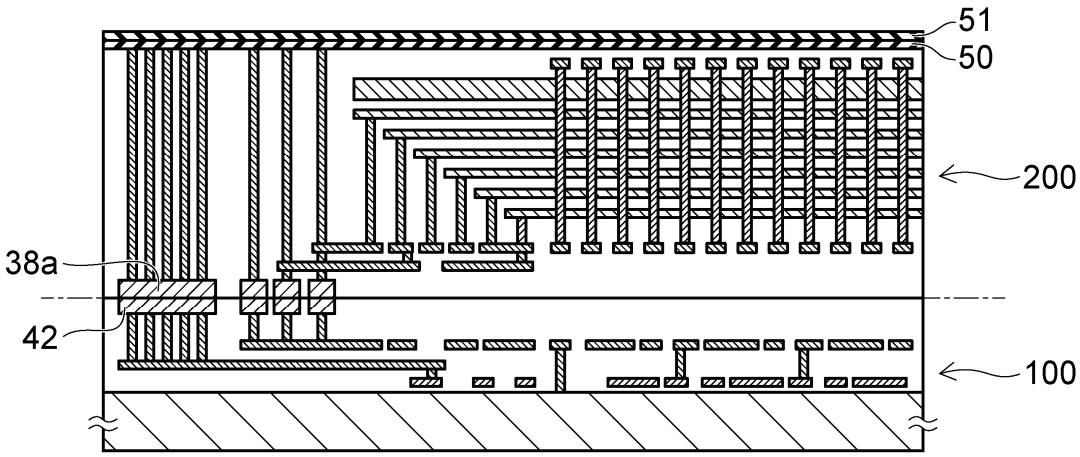


FIG. 8

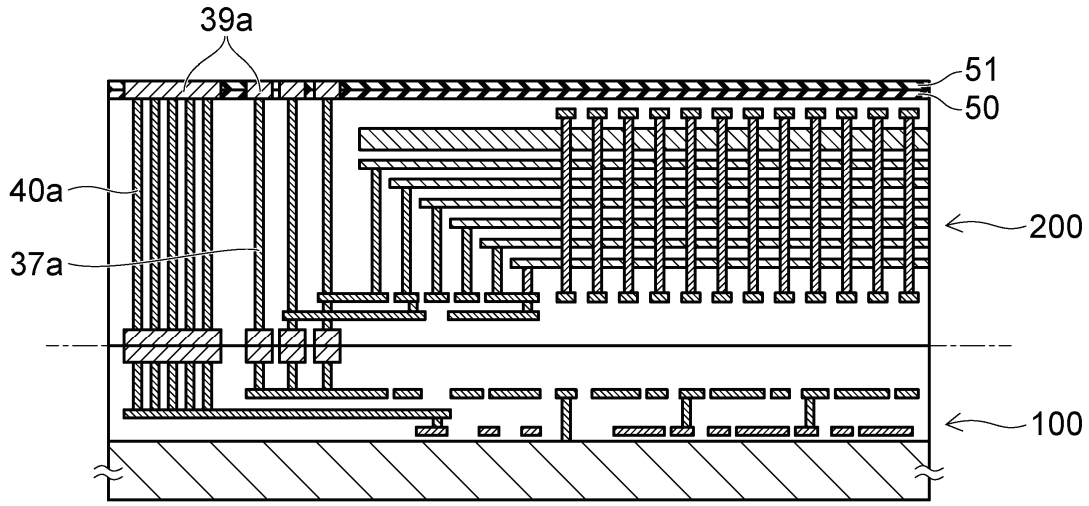



FIG. 9

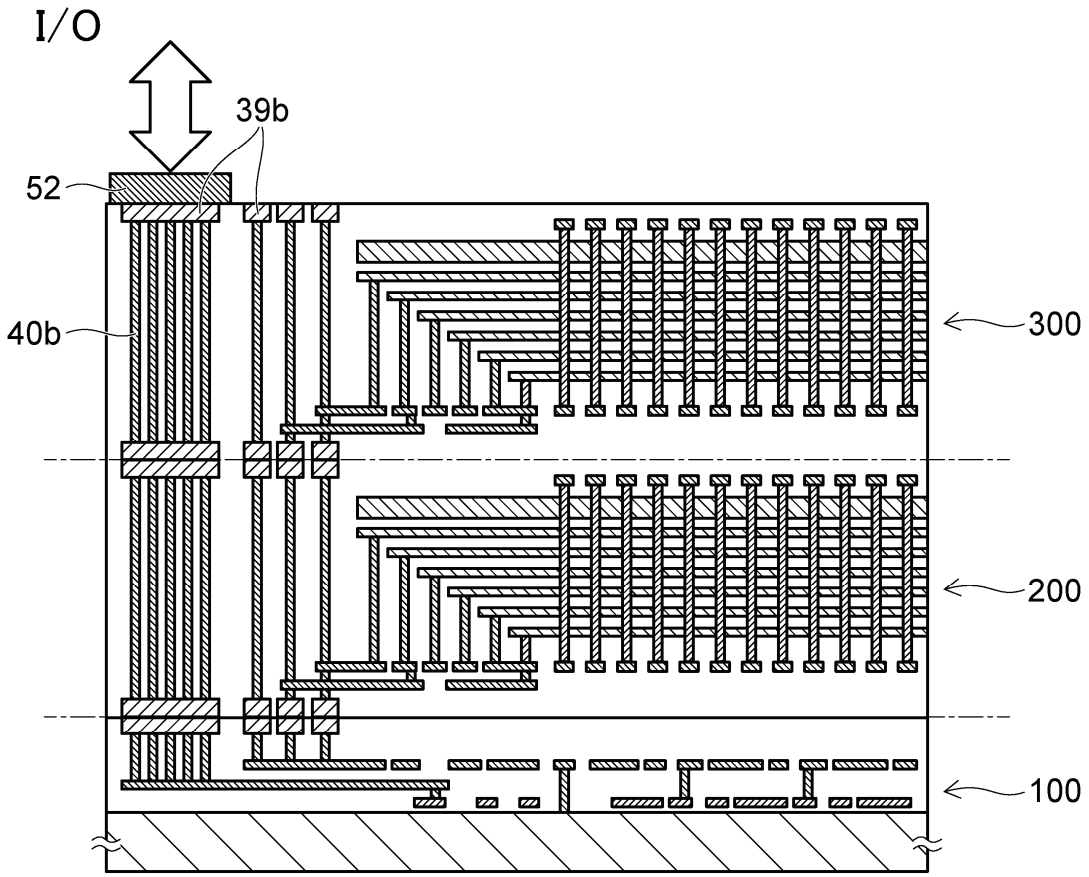


*FIG. 10*

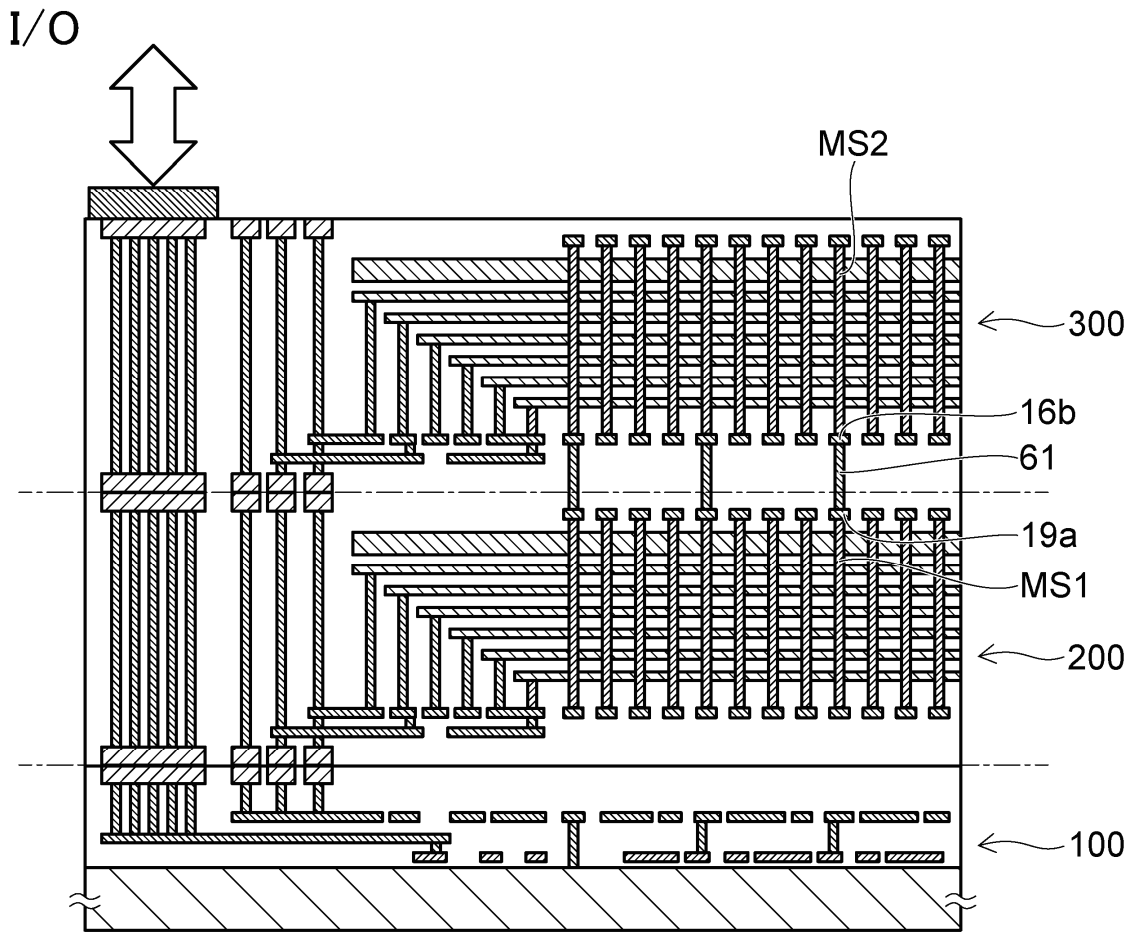


FIG. 11

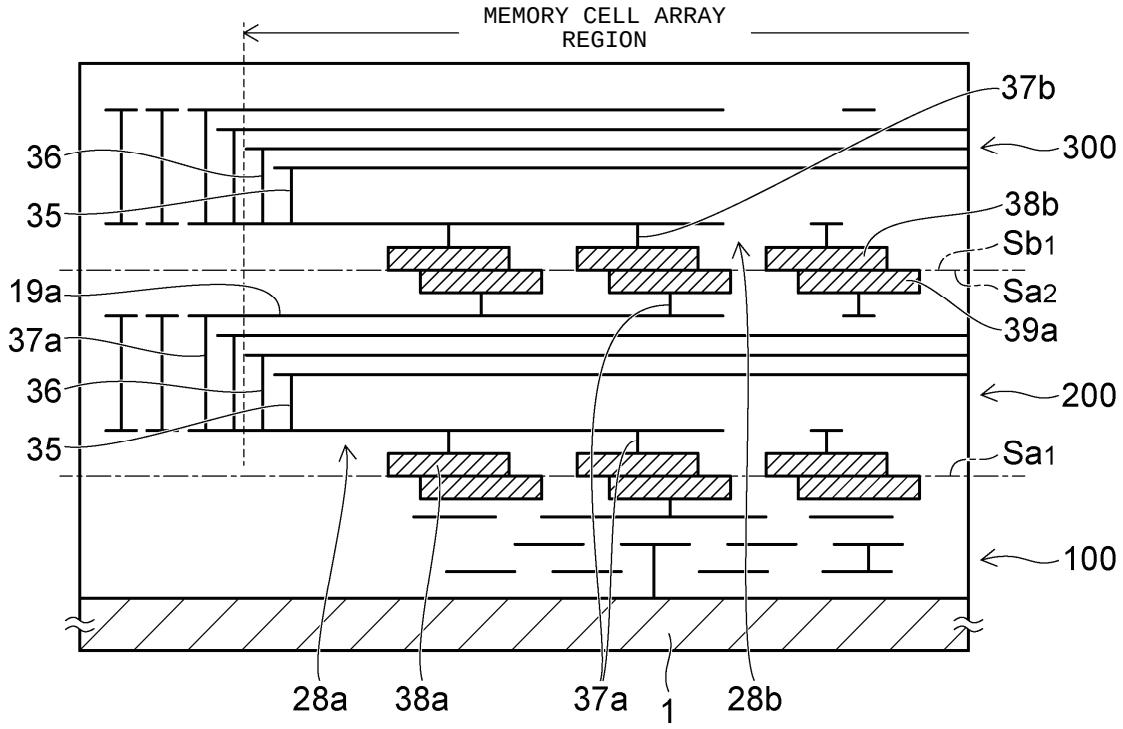

MEMORY CELL ARRAY REGION
37b
300
36
35
38b
Sb1
19a
Sa2
39a
37a
36
200
35
Sa1
100
28a
38a
37a
1
28b

*FIG. 12*

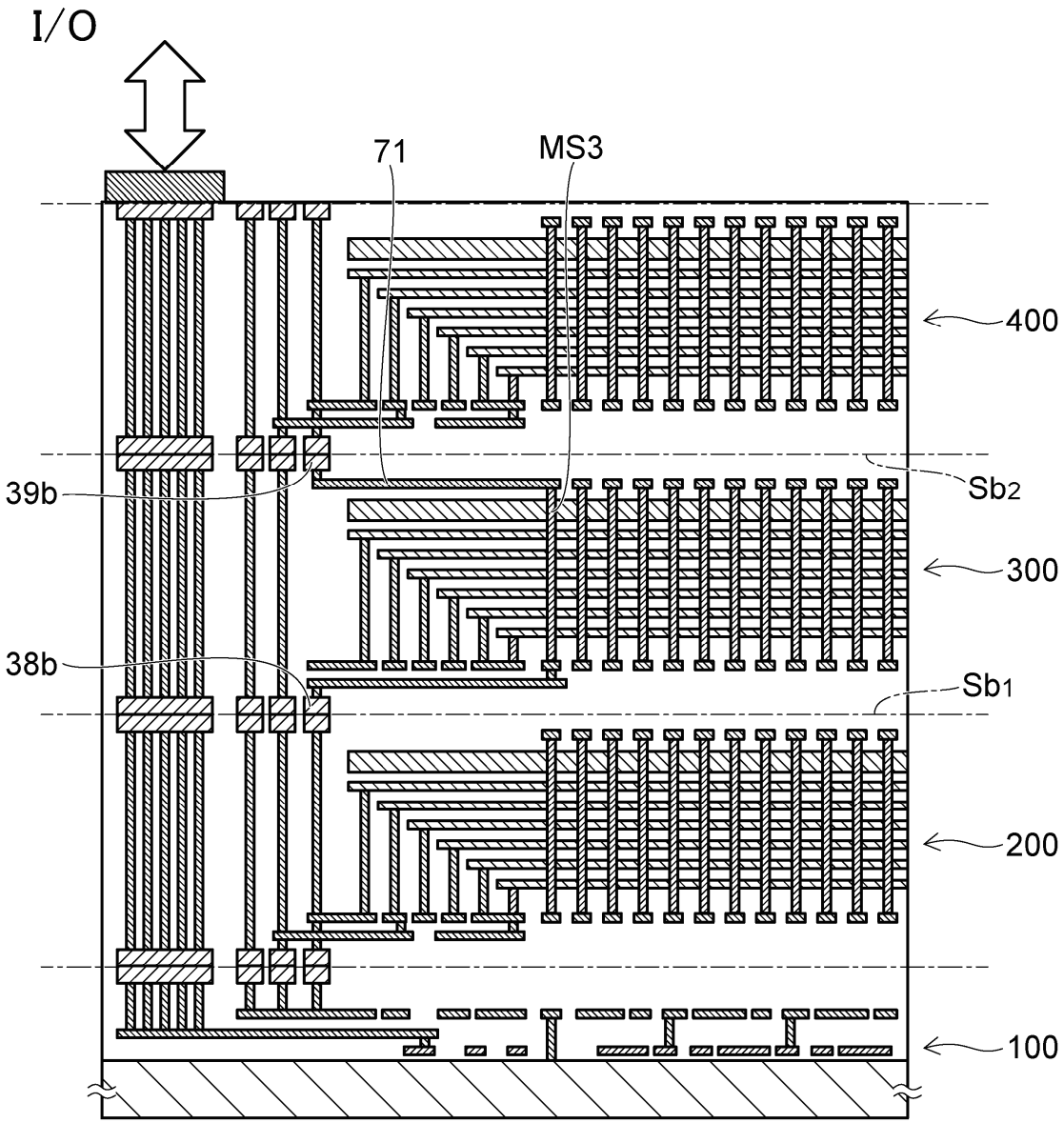


FIG. 13

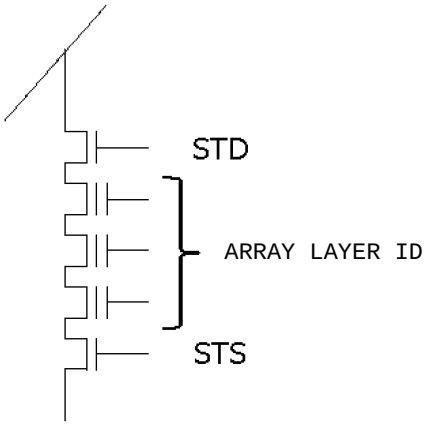
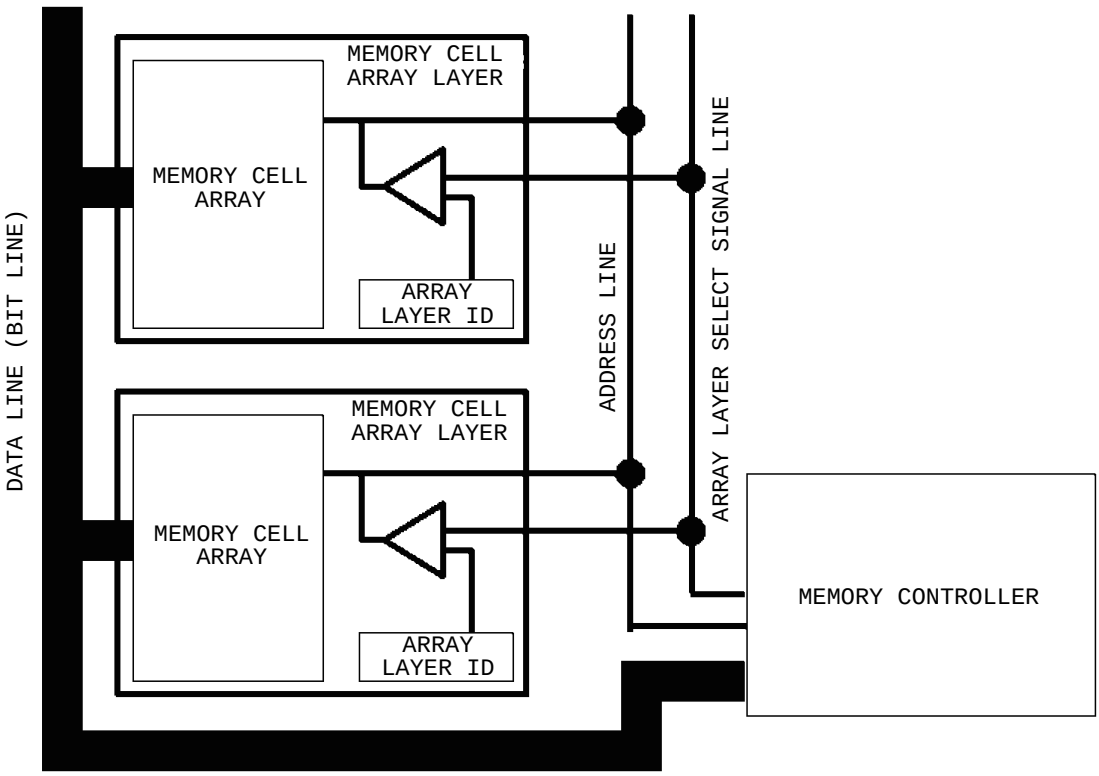

STD
ARRAY LAYER ID
STS

FIG. 14


DATA LINE (BIT LINE)
MEMORY CELL ARRAY LAYER
MEMORY CELL ARRAY
ARRAY LAYER ID
MEMORY CELL ARRAY LAYER
MEMORY CELL ARRAY
ARRAY LAYER ID
ADDRESS LINE
ARRAY LAYER SELECT SIGNAL LINE
MEMORY CONTROLLER