

CACHE ENABLING ARCHITECTURE

Abstract

A cache enabling architecture in which an optical storage reading and/or writing device (2), a caching processor (5) and a mass writing and reading device (3) are each connected to a data bus (1). The optical storage reading and/or writing device
5 exchanges information directly with the caching processor over the data bus. The caching uses the mass writing and reading device as cache memory.

FIG. 1



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