

CLAIMS:

1. A processor comprising:
 - a first processing core of a processor coupled to a an internal cache of the processor as a direct agent for thread instructions and data; and
 - a second processing core of the processor coupled to the cache as a direct agent for separate thread instructions and data;
 - a first programmable integrated circuit (IC) of the processor coupled to the first processing core to execute workloads assigned by the first processing core and coupled to the cache as a direct agent to access data of the first processing core independent of the first processing core to independently execute workloads;
 - a second programmable IC of the processor coupled to the second processing core to execute workloads assigned by the second processing core and coupled to the cache as a direct agent to access data of the second processing core independent of the second processing core to independently execute workloads, wherein the first and second programmable ICs are field programmable gate arrays (FPGAs) that accelerate execution of performance critical loops in a workload; and
 - a third processing core coupled to the first programmable IC, wherein the cache comprises a first memory device coupled only to the first processing core, the third processing core and the first programmable IC, and wherein the first programmable IC accelerates execution of workloads processed at the first processing core and the third processing core.
2. The processor of claim 1, wherein the first processing core selects a first workload to be accelerated at the first programmable IC and the second processing core selects a second workload to be accelerated at the second programmable IC.
3. The processor of claim 1, wherein the first programmable IC is programmed to execute a first type of workload and the second programmable IC is programmed to execute a second type of workload.
4. The processor of claim 1, wherein the first and second programmable ICs provide one or more independent threads to perform latency hiding.
5. The processor of claim 1, wherein the first processing core comprises a first controller to control execution of the first programmable IC, and the second processing core comprises a second controller to control execution of the second programmable IC.
6. The processor of claim 5, wherein the first controller and the second controller control execution of the first programmable IC and the second programmable IC via memory-mapped I/O (MMIO) regions.
7. The processor of claim 5, wherein the first controller and the second controller control execution of the first programmable IC and the second programmable IC via dedicated processor instructions.
8. The processor of claim 1, wherein the processor comprises a general-purpose microprocessor.

9. The processor of claim 8, wherein the cache comprises:

a first cache memory device coupled to the first processing core and the first programmable IC; and
a second cache memory device coupled to the second processing core and the second programmable IC.

10. The processor of claim 9, wherein the first programmable IC is an independent agent to the first cache memory device, and the second programmable IC is an independent agent to the second cache memory device.

11. The processor of claim 1 wherein the processor comprises a graphics processing unit (GPU).

12. The processor of claim 11, wherein the cache comprises:

a first memory device coupled to the first processing core and the first programmable IC; and a
second memory device coupled to the second processing core and the second programmable IC.

13. A central processing unit (CPU), comprising:

a plurality of processing cores including a first processing core and a second processing core;

a first field programmable gate array (FPGA) of the CPU coupled to the first processing core
to execute workloads assigned by the first processing core;

a first cache memory device of the CPU coupled to the first processing core and the first FPGA,
wherein the first processing core and the first FPGA are independently coupled to the first cache
memory device as direct agents for independent access to thread instructions and data;

a second FPGA of the CPU coupled to the second processing core to execute workloads assigned by
the second processing core;

a second cache memory device of the CPU coupled to the second processing core and the second
FPGA, wherein the second processing core and the second FPGA are independently coupled to the
second cache memory device as direct agents for independent access to thread instructions and
data; and

a third processing core coupled to the first FPGA, wherein the first cache memory device comprises a
first memory device coupled only to the first processing core, the third processing core and the
first FPGA, and wherein the first FPGA accelerates execution of workloads processed at the first
processing core and the third processing core.

14. The CPU of claim 13, wherein the first processing core selects a first workload to be accelerated
at the first FPGA and the second processing core selects a second workload to be accelerated at the
second FPGA.

15. The CPU of claim 14, wherein the first FPGA is programmed to execute a first type of workload
and the second FPGA is programmed to execute a second type of workload.

16. The CPU of claim 15, wherein the first processing core comprises a first controller to control
execution of the first FPGA, and the second processing core comprises a second controller to control
execution of the second FPGA.

17. The CPU of claim 13, further comprising a third processing core coupled to the first FPGA and the first cache memory device, wherein the first FPGA accelerates execution of workloads processed at the first processing core and the third processing core.

18. A graphics processing unit (GPU), comprising:

a plurality of graphics processing cores of the GPU, including a first graphics processing core and a second graphics processing core;

a first field programmable gate array (FPGA) of the GPU coupled to the first graphics processing core to execute workloads assigned by the first graphics processing core;

a first memory device coupled to the first graphics processing core and the first FPGA, wherein the first graphics processing core and the first FPGA are independently coupled to the first memory device as direct agents for independent access to thread instructions and data;

a second FPGA of the GPU coupled to the second graphics processing core to execute workloads assigned by the second graphics processing core; and a second memory device coupled to the second graphics processing core and the second FPGA, wherein the second graphics processing core and the second FPGA are independently coupled to the second memory device as direct agents for independent access to thread instructions and data; and

a third processing core coupled to the first FPGA, wherein the first memory device is coupled only to the first graphics processing core, the third processing core and the first FPGA, and wherein the first FPGA accelerates execution of workloads processed at the first graphics processing core and the third processing core.

19. The GPU of claim 18, wherein the first graphics processing core selects a first workload to be accelerated at the first FGA and the second graphics processing core selects a second workload to be accelerated at the second FPGA.

20. The GPU of claim 19, wherein the first FPGA is programmed to execute a first type of graphics workload and the second FPGA is programmed to execute a second type of graphics workload.

21. The GPU of claim 20, wherein the first graphics processing core comprises a first controller to control execution of the first FPGA, and the second graphics processing core comprises a second controller to control execution of the second FPGA.

22. The GPU of claim 18, wherein the third processing core comprises a third graphics processing core coupled to the first FPGA and the first memory device, wherein the first FPGA accelerates execution of workloads processed at the first graphics processing core and the third graphics processing core.