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TITLE OF THE INVENTION

METHOD AND APPARATUS FOR LOW-TEMPERATURE ANNEALING OF METALLIZATION MICRO-STRUCTURES IN THE PRODUCTION OF A MICROELECTRONIC DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

Not Applicable

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not Applicable

BACKGROUND OF THE INVENTION

In the production of semiconductor integrated circuits and other microelectronic articles from microelectronic workpieces, such as semiconductor wafers, it is often necessary to provide multiple metal layers on a substrate to serve as interconnect metallization which electrically connects the various devices on the integrated circuit to one another. Traditionally, aluminum has been used for such interconnects, however, it is now recognized that copper metallization may be preferable.

Modern semiconductor manufacturing processes, especially those used for advanced logic devices, make use of multiple layers of metal interconnects.

As the length of metal interconnects increases and the cross-sectional area and spacing between them decreases, the RC delay caused by the interconnect wiring also increases. With the drive toward decreasing interconnect size and the increasing demands placed on the interconnects, the current aluminum interconnect technology becomes deficient. Copper interconnects can help alleviate many of the problems experienced in connection with the current aluminum technology.

In view of the limitations of aluminum interconnect technology, the industry has sought to use copper as the interconnect metallization by using a damascene and/or patterned plating electroplating process where holes, more commonly called vias, trenches and other recesses are used to produce the desired copper patterns. In the damascene process, the wafer is first provided with a metallic seed layer and barrier/adhesion layer that are disposed over a dielectric layer into which trenches are formed. The seed layer is used to conduct electrical current during a subsequent metal electroplating step. Preferably, the seed layer is a very thin layer of metal that can be applied using one of several processes. For example, the seed layer of metal can be laid down using physical vapor deposition or chemical vapor deposition processes to produce a layer on the order of 1000 angstroms thick. The seed layer can also be formed of copper, gold, nickel, palladium, and most or all other metals. The seed layer is formed over a surface that is convoluted by the presence of

the trenches, or other device features, which are recessed into the dielectric substrate.

In single damascene processes using electroplating, a process employing two electroplating operations is generally employed. First, a copper layer is electroplated onto the seed layer in the form of a blanket layer. The blanket layer is plated to an extent which forms an overlying layer, with the goal of completely providing a copper layer that fills the trenches that are used to form the horizontal interconnect wiring in the dielectric substrate. The first blanket layer is then subject, for example, to a chemical mechanical polish step in which the portions of the layer extending above the trenches are removed, leaving only the trenches filled with copper. A further dielectric layer is then provided to cover the wafer surface and recessed vias are formed in the further dielectric layer. The recessed vias are disposed to overlie certain of the filled trenches. A further seed layer is applied and a further electroplated copper blanket layer are provided that extend over the surface of the further dielectric layer and fills the vias. Again, copper extending above the level of the vias is removed using, for example, chemical mechanical polishing techniques. The vias thus provide a vertical connection between the original horizontal interconnect layer and a subsequently applied horizontal interconnect layer. Electrochemical deposition of copper films has thus become an important process step in the manufacturing of high-performance microelectronic

products.

Alternatively, the trenches and vias may be etched in the dielectric at the same time in what is commonly called a "dual damascene" process. These features are then processed, as above, with barrier layer, seed layer and fill/blanket layer that fill the trenches and vias disposed at the bottoms of the trenches at the same time. The excess material is then polished, as above, to produce inlaid conductors.

The electrical properties of the copper metallization are important to the performance of the associated microelectronic device. Such devices may fail if the copper metallization exhibits excessive electromigration that ultimately results in an open circuit condition in one or more of the metallization structures. One factor that has a very large influence on the electromigration resistance of sub-micron metal lines is the grain size of the deposited metal. This is because grain boundary migration occurs with a much lower activation energy than trans-granular migration.

To achieve the desired electrical characteristics for the copper metallization, the grain structure of each deposited blanket layer is altered through an annealing process. This annealing process is traditionally thought to require the performance of a separate processing step at which the semiconductor wafer is subject to an elevated temperature of about 400 degrees Celsius.

The present inventors have recognized substantial improvements over the

foregoing processes employing the elevated temperature annealing. To this end, the present inventors have disclosed herein a process for filling vias, trenches, and the like using an electrochemical metal deposition process that does not require a subsequent elevated temperature annealing step or, in the alternative, that uses a subsequent elevated temperature annealing process that takes place at temperatures that are traditionally used in the copper metallization process and are compatible with low temperature semiconductor processing. Additionally, the present inventors have set forth various apparatus for implementing such an annealing process in a controlled manner.

BRIEF SUMMARY OF THE INVENTION

A method for filling recessed microstructures at a surface of a semiconductor wafer with metallization is set forth. In accordance with the method, a layer is deposited into the microstructures with a process, such as an electroplating process, that generates grains that are sufficiently small so as to substantially fill the recessed microstructures. The deposited metal is subsequently subjected to an annealing process at a temperature below about 100 degrees Celsius, and may even take place at ambient room temperature.

One embodiment of the method comprises providing a semiconductor wafer with a feature that is to be connected with copper metallization. At least one dielectric layer is applied over a surface of the semiconductor wafer including the feature. Recessed microstructures are then provided in the at least one dielectric layer. A surface of the wafer, including the recessed microstructures, is provided with barrier/adhesion layer and a seed layer for subsequent electrochemical copper deposition. Copper metallization is electrochemically deposited on the surface of the wafer to substantially fill the recessed microstructures. The present inventor has found that such an electrochemically deposited layer may be annealed at temperatures that are substantially lower than the temperatures typically thought necessary for such annealing. Various methods are set forth that take advantage of this finding.

In a further embodiment of the disclosed method, the electrochemically

deposited copper layer is allowed to self-anneal at ambient room temperature for a predetermined period of time before removing copper metallization from the surface of the wafer that extends beyond the recessed features.

In accordance with a still further embodiment of the disclosed method, subsequent wafer processing, including removal of selected areas of the copper metallization, takes place without an intermediate elevated temperature annealing step and may, for example, take place before self-annealing is allowed to occur.

In accordance with a still further embodiment of the method, the electrochemically deposited copper is subject to an elevated temperature annealing process. However, that annealing process takes place at a temperature below about 100 degrees Celsius or at a temperature below which an applied low-K dielectric layer suffers degradation in its mechanical and electrical properties.

Various novel apparatus for executing unique annealing processes are also set forth. One such apparatus for use in applying metallization in recessed micro-structures of a microelectronic workpiece comprises at least one deposition station for depositing a conductive material, such as electrolytically deposited copper, into at least the recessed micro-structures of the microelectronic workpiece. The apparatus also includes at least one annealing station for subjecting the microelectronic workpiece to an annealing temperature

that is at or below about 250 degrees Celsius and/or for subjecting the workpiece to a controlled temperature gradient. The temperature gradient may be such that the temperature decreases in a direction that is opposite to the direction of formation of the metal material as it is deposited at the at least one deposition station.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Fig. 1 illustrates one embodiment of a plating apparatus that may be used to apply an electrochemically deposited copper metallization layer to the surface of a semiconductor wafer in accordance with the disclosed methods.

Figs. 2A-2G illustrate the various steps used in one embodiment of the disclosed method.

Fig. 3 is a graph showing the sheet resistance of an electrochemically deposited layer that has been deposited in accordance with the disclosed method as a function of time.

Figs. 4 and 5 are graphs of various x-ray scanning parameters associated with an electrochemically deposited layer that has been deposited in accordance with the disclosed method.

Figs. 6-8 illustrate the use of a low-temperature annealing process to remove voids in a copper film.

Figs. 9 and 10 illustrate the effect of temperature rate on temperature gradient over a cross-section of the workpiece of Figs. 6-8.

Figs. 11-15 illustrate various apparatus that may be used in the disclosed low-temperature annealing process.

Figs. 16 and 17 illustrate hollow the apparatus of Figs. 11-15 may be integrated in a wet chemical processing tool set.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 1 shows various components of a processing station 10 suitable for electroplating a metal, such as copper, onto a semiconductor wafer in accordance with the disclosed method. The two principal parts of processing station 10 are a processing head, shown generally at 15, and an electroplating bowl assembly 20. It will be recognized, however, that a wide variety of processing station configurations may be used to implement the disclosed method and that the specific construction of the station 10 is merely exemplary. To this end, such a processing station may merely comprise an anode, one or more wafer contacts to render the wafer a cathode, a plating chamber having a plating bath that contacts both the wafer and the anode, and a source of plating power. Various configurations of these elements may be employed.

As shown in Fig. 1, the electroplating bowl assembly 20 includes a cup assembly 25 that is disposed within a reservoir container 30. Cup assembly 25 includes a fluid cup portion 35 holding the chemistry for the electroplating process. The cup assembly of the illustrated embodiment also has a depending skirt 40 which extends below the cup bottom 45 and may have flutes open therethrough for fluid communication and release of any gas that might collect as the chamber of the reservoir assembly below fills with liquid. The cup is preferably made from polypropylene or other suitable material.

A lower opening in the bottom wall of the cup assembly 25 is connected to

a polypropylene riser tube 50 which, for example, is adjustable in height relative thereto by a threaded connection. A first end of the riser tube 50 is secured to the rear portion of an anode shield 55 that supports anode 60. A fluid inlet line 165 is disposed within the riser tube 50. Both the riser tube 50 and the fluid inlet line are secured with the processing bowl assembly 20 by a fitting 70. The fitting 70 can accommodate height adjustment of both the riser tube and line 65. As such, the connection between the fitting 70 and the riser tube 50 facilitates vertical adjustment of the anode position. The inlet line 65 is preferably made from a conductive material, such as titanium, and is used to conduct electrical current to the anode 60, as well as supply fluid to the cup.

Process fluid is provided to the cup through fluid inlet line 65 and proceeds therefrom through fluid inlet openings 75. Plating fluid then fills the chamber 35 through openings 75 as supplied by a plating fluid pump (not shown) or other suitable supply.

The upper edge of the cup sidewall 80 forms a weir that limits the level of electroplating solution within the cup. This level is chosen so that only the bottom surface of wafer W is contacted by the electroplating solution. Excess solution pours over this top edge surface into an overflow chamber 85.

The outflow liquid from chamber 85 is preferably returned to a suitable reservoir. The liquid can then be treated with additional plating chemicals or other constituents of the plating or other process liquid and used again.

In preferred use of the apparatus for electroplating, the anode 60 is a consumable anode used in connection with the plating of copper or other metals onto semiconductor materials. The specific anode may alternatively be an inert anode, the anode used in station 10 varying depending upon the specifics of the plating liquid and process being used.

The embodiment of the station shown in Fig. 1 also employs a diffuser plate 90 which is disposed above the anode 60 for providing a more even distribution of the flow of the fluid plating bath across the surface of wafer W. Fluid passages are provided over all or a portion of the diffuser plate 90 to allow fluid communication therethrough. The height of the diffuser plate within the cup assembly may be adjustable using height adjustment mechanisms 95.

The anode shield 55 is secured to the underside of the consumable anode 60 using anode shield fasteners 100 to prevent direct impingement by the plating solution as the solution passes into the processing chamber 35. The anode shield 55 and anode shield fasteners 100 are preferably made from a dielectric material, such as polyvinylidene fluoride or polypropylene. The anode shield serves to electrically isolate and physically protect the backside of the anode.

The processing head 15 holds a wafer W within the processing chamber 35. In the disclosed embodiment of station 10, the head 15 is constructed to rotate the wafer W within chamber 35. To this end, the processing head 15 includes a rotor assembly 150 having a plurality of wafer-engaging contact fingers

105 that hold the wafer against features of the rotor. Fingers 105 are preferably adapted to conduct current between the wafer and a plating electrical power supply and may be constructed in accordance with various configurations.

The processing head 15 is supported by an head operator 115. Head operator 115 includes an upper portion 120 that is adjustable in elevation to allow height adjustment of the processing head. Head operator 115 also has a head connection shaft 125 that is operable to pivot about a horizontal pivot axis 130. Pivotal action of the processing head using operator 115 allows the processing head to be placed in an open or face-up position (not shown) for loading and unloading wafer W. Fig. 1 illustrates the processing head pivoted into a face-down position in preparation for processing. It will be recognized that such flipping of the wafer is not necessary to the performance of the disclosed methods.

Figs. 2A – 2G illustrate one method of filling a trench and via formed on the surface of a semiconductor wafer wherein the electrochemically deposited copper layer may be applied using the apparatus described in connection with Fig. 1. Fig. 2A illustrates a base 400 having an area 405 that is to be connected by copper metallization. In Fig. 2B a layer 410 of dielectric material, such as silicon dioxide or a low-K dielectric material, is deposited over the base 400 including over area 405. Through a photoresist process and reactive ion etch or the like, selective portions of layer 410 are removed to form, for example, a trench 415 and via 420 into which copper metallization is to be deposited. The end structure is

shown in the perspective view of Fig. 2C wherein the via 420 overlies connection area 405 and trench 415 overlies via 420. Connection area 405 may be, for example, a metallization feature above the substrate.

As shown in Fig. 2D, a barrier layer 423 and seed layer 425 may be disposed on the surface of dielectric layer 410. The barrier layer may be, for example, tantalum or titanium nitride. The barrier layer 423 is typically used when the structure 405 is susceptible to contamination from copper or the seed layer metal, and/or when the seed layer metal or copper may readily migrate through the dielectric layer 410 and contaminate other portions of the microelectronic circuit. As such, barrier layer 423 should be sufficiently thick along the contour of the trenches and vias to act as a diffusion barrier. Layer 423 may also function as an adhesion layer to facilitate binding between the seed layer 425 and the dielectric 410. If, however, the structure 405 is not susceptible to such contamination, there is sufficient adhesion, and the dielectric layer 410 itself acts as a barrier layer, then a separate barrier layer 423 may not be necessary. The seed layer 425 may, for example, be a copper layer or other conductive metal layer and is preferably at least 200 Angstroms thick at its thinnest point. Sidewalls 430 of the trench 415 and via 420 as well as the bottom of via 420 should be covered by the seed layer 425 and barrier layer 423 to facilitate a subsequent electrochemical copper deposition step. The seed layer 425 may be deposited through, for example, a CVD or PVD process.

The semiconductor wafer with the seed layer 425 is subject to a subsequent electrochemical copper deposition process. The electrochemical copper deposition process is executed so as to form numerous nucleation sites for the copper deposition to thereby form grain sizes that are substantially smaller than the characteristic dimensions of the via 420 and trench 415. An exemplary structure having such characteristics is illustrated in Fig. 4E wherein layer 440 is a layer of copper metallization that has been deposited using an electrochemical deposition process.

As shown in Fig. 2E, the copper metallization 440 formed in the electrochemical deposition process is deposited over the seed layer 425 and extends a distance above the surface of dielectric layer 410. Since the only features that are to contain the metallization are the via 420 and trench 415, excess copper above the dielectric layer 410 must be removed. Removal of the excess copper above the upper surface of the dielectric layer 410 may be executed using a chemical mechanical polish technique. An exemplary structure in which such removal has taken place is illustrated in Fig. 2F. After such removal, a capping barrier layer 445 may be disposed, for example, over the entire surface of the wafer, or the processes set forth in Figs. 2A - 2F may be repeated without a capping barrier layer 445 whereby the trench 415, now filled with copper metallization, corresponds to the structure 405 that further copper metallization is to contact.

A comparison between Figs. 4E and 4F reveals that an increase in the grain size of the copper layer 440 has taken place. Traditionally, the change in the grain size has been forced through an annealing process. In such an annealing process, the wafer is subject to an elevated temperature that is substantially above the ambient temperature conditions normally found in a clean room. For example, such annealing usually takes place in a furnace having a temperature generally around or slightly below 400 degrees Celsius, or about half of the melting temperature of the electrodeposited copper. Annealing steps are normally performed at a temperature of at least 25 percent of the melting point temperature of the material as measured on an absolute temperature scale. As such, a separate annealing step is performed on the wafer using a separate piece of capital equipment. Such an annealing step is usually performed for each layer of metallization that is deposited on the wafer. These additional steps increase the cost of manufacturing devices from the wafer and, further, provide yet another step in which the wafer may be mishandled, contaminated, or otherwise damaged.

Absent such an annealing step, the traditional view is that the substantial number of grains per given volume in such sub-micron structures significantly decreases the electromigration resistance of the metal lines that are produced and gives the material a higher resistivity. This is because grain boundary migration occurs with a much lower activation energy than trans-

granular migration. As such, conventional wisdom dictates that a separate annealing step is required.

The present inventor has found that such a separate annealing step in which the electrochemically deposited copper is subject to a subsequent high temperature annealing process (e.g., at about 400 degrees Celsius) is not, in fact, necessary. Rather, electrochemically deposited copper metallization having grain sizes substantially smaller than the sub-micron structures that they fill may be subject to an annealing process in which the annealing of the copper metallization takes place at, for example, room temperature or at temperatures substantially below 400 degrees Celsius where the annealing process is more easily controlled and throughput is increased.

In accordance with one embodiment of the disclosed method, the electrochemical deposition of the copper layer 440 takes place in the apparatus set forth in Fig. 1. The processing chamber 110 is configured so that the top of the diffuser 90 is approximately between 0.5 cm – 5 cm (preferably 2.0 cm) from the top of the cup 25. The distance between the top of the diffuser 90 and the top of the anode 60 is between 0.5 cm – 10 cm (preferably 1.6 cm) but always greater than the diffuser to cup distance.

The electrochemical plating solution may be Enthone-OMI Cu Bath M Make-up Solution having 67 g/l of CuSO4, 170 g/l of H2SO4, and 70 ppm of HCl. The additive solutions utilized may be Enthone-OMI Cu Bath M-D (6.4

ml/l - make-up) and Enthone-OMI Cu Bath M LO 70/30 Special (1.6 ml/l - make-up). The flow rate through the cup 25 of this solution may be approximately 1.0 – 10 GPM (preferably 5.5 GPM) and the plating temperature may be between about 10-40 degrees Celsius (preferably 25 degrees Celsius). The plating bath could alternatively contain any of a number of additives from manufacturers such as Shipley (Electroposit 1100), Lea Ronal (Copper Gleam PPR), or polyethylene glycol (PEG). An alkaline plating bath suitable for electroplating microelectronic components is set forth in co-pending provisional patent application U.S.S.N. _____, entitled " PROCESS AND PLATING SOLUTION FOR ELECTROPLATING A COPPER METALLIZATION LAYER ONTO A WORKPIECE" (Attorney Docket No. SEM4492P0250US; Corporate Docket No. P98-0039) which is hereby incorporated by reference.

The electrochemical process of the disclosed embodiment may be used to electroplate a copper metallization layer onto the wafer at a thickness sufficient to at least fill the trenches and/or vias. Generally stated, the embodiment disclosed herein may be divided into five sub-processes. A dwell (pre-plate) sub-process takes place when the wafer is first introduced to the electroplating bath. At that time, no plating current is provided. Rather, the surface of the wafer that is to be plated is exposed to the plating bath for a predetermined period of time without plating power, such as for five seconds.

After the dwell cycle, a low current initiation sub-process may ensue.

During the low current initiation sub-process, a low plating current is provided between the anode and the wafer. In accordance with the disclosed embodiment, a direct current with a current density of approximately 3.2 mA/cm^2 is utilized. The low current process may proceed, for example, for a predetermined period of time such as 30 seconds.

After the low current initiation sub-process is completed, a high current plating sub-process is initiated. It is during this sub-process that a majority of the copper is plated onto the wafer. During this step, a high plating current is provided for the electroplating operations. The plating waveform may be a constant voltage or current, a forward-only pulsed voltage or current, or a forward and reverse voltage or current. In accordance with the disclosed embodiment, and average cathode current density of approximately 20 mA/cm^2 is used with a current waveform that is direct current, forward pulsed, or reverse pulsed. Preferably, a direct current or forward only pulsed current is utilized with a frequency between 1 and 1000 Hz. More preferably, the frequency is between 5 and 20 Hz, with a duty cycle between 50 percent and 95 percent. More preferably, the duty cycle is between 65 percent and 85 percent. The time duration of the high current plating sub-process is dependent on the nominal thickness of the copper metallization layer that is to be applied to the wafer. For a copper metallization layer having a nominal thickness of 1.5 microns, the high current sub-process proceeds for approximately three minutes

and 40 seconds. During both the low current initiation and high current plating sub-processes, the wafer is preferably spun on the rotor at a rate of between about 1 – 100 rpm (preferably 20 rpm).

Once the desired amount of copper has been plated onto the wafer, the wafer is lifted from contact with the plating solution. This process takes approximately two seconds, after which the wafer is spun on the rotor to remove the plating solution. For example, the wafer may be spun at 200 – 2000 rpm (preferably 500 rpm) for a time period of five seconds to remove the majority of the electroplating solution from the surface of the wafer. Subsequent rinsing and drying steps may be executed on the wafer in, for example, other processing chambers dedicated to such functions.

The foregoing process generates nucleation sites, grain growth mechanisms, and copper grain sizes that are sufficiently small so as to fill trenches and vias with widths as low or less than 0.3 micron and aspect ratios greater than 4-to-1. Initial grain size may be varied depending upon the plating waveform used and/or the additives used in the plating solution. Despite the small copper grain size that results from these processes, the resulting copper metallization layer may be annealed at substantially lower temperatures than traditionally suggested to form substantially larger copper grains thereby providing the copper with enhanced electrical characteristics when compared to copper deposition processes that do not promote self-annealing.

Figs. 3-5 are derived from experimental data obtained by the present

inventor on two different wafers showing that copper metallization deposited in a process in which the initial grain size of the copper crystals is sufficiently small so as to fill sub-micron dimension trenches and vias undergoes a self-annealing process at room temperature. Fig. 3 is a graph of the sheet resistance, Rs, over time of a 1.5 micron copper film deposited in the manner stated above. As illustrated, the sheet resistance begins to decrease approximately eight hours after the copper metallization has been electrochemically deposited on the wafer. After about 20 hours, a substantial decrease in the sheet resistance takes place until, ultimately, the sheet resistance is stabilized at a time between 40 and 80 hours after the deposition. Such measurements were made using a 4-point probe such as a Prometrix RS30.

Figs. 4 and 5 relate to x-ray diffraction scanning of the electrochemically deposited copper layer. With respect to Fig. 4, the area under each curve is proportional to the volume of the copper film with crystals having their [111] crystal plane directions perpendicular to the plane of the exposed surface of the copper layer. As illustrated, line 510 represents the measurements taken immediately after the copper metallization layer was deposited onto the wafer. Line 520 represents the measurements taken hours after the metallization layer was deposited. A comparison between the curves represented by lines 510 and 520 indicates that the number of re-oriented crystals has increased over time.

In the Rocking Curves of Fig. 5, line 530 represents the Rocking Curve of the copper metallization layer immediately after it has been deposited on the

wafer, while line 540 represents the Rocking Curve of the copper metallization layer hours after it has been deposited. The width of the curve designated by line 530 at half its height, when compared to that of the curve designated by line 540, indicates that the copper crystals are becoming more aligned and that the grain sizes of the copper crystals have increased.

Pursuant to the foregoing findings, one embodiment of the present method requires that the copper metallization be allowed to self-anneal for a predetermined period of time prior to chemical mechanical planarization thereof. At room temperatures, this predetermined period of time may range, for example, between 20 and 80 hours. In accordance with a further embodiment of the method, chemical mechanical planarization may take place before the self-annealing is completed (e.g., before the end of the predetermined period) and, further, may enhance the self-annealing process by imparting activation energy to the metallization layer during the process.

In accordance with a still further embodiment of the method, the copper metallization layer may be annealed before or after chemical mechanical polishing at an elevated temperature which is substantially below the temperature used in the annealing processes that have been traditionally employed. To this end, the wafer having the metallization layer may be placed in an oven having a temperature that is substantially below the 400 degrees Celsius traditionally thought to be necessary to promote the annealing process of copper having such small grain sizes. At a low temperature of about 60 degrees Celsius, the

annealing process may be completed in about 15 minutes. At temperatures above 100 degrees Celsius, the annealing times become so short (<1 minute) so as to make annealing at higher temperatures unwarranted and wasteful.

The foregoing process is particularly advantageous when used prior to chemical mechanical polishing (CMP). CMP involves the use of mechanical and chemical forces to remove copper that is deposited in excess of what is desired for interconnects. As a direct result of changes in the grain size of copper films, the CMP polish rate, or removal rate, is seen to vary. The initial, small grained (i.e. many grain boundaries) films are seen to polish faster (at least with a particular CMP slurry) than they do after self-annealing and the associated grain growth. This indicates that with the particular slurry being used, the chemical action may be more severe than the mechanical action, or that the mechanical polishing is more effective on films with higher hardness values. The observed change in polish rate of 30 to 50% is to be expected as a direct result of the grain size change.

The change in grain size is expected to affect both the mechanical and the chemical aspects of CMP. Small-grained films are generally harder than large-grained ones. The hardness of a material will have a direct effect on the abrasion rate in a mechanical polishing process. Likewise, grain boundaries are chemically etched faster than single grain areas of a metal film. Therefore, a film containing a larger fraction of grain boundaries per unit surface area will chemically etch faster, on average, than one with larger grains, and therefor fewer

grain boundaries.

Because of the changes in removal rate of the CMP process with a change in grain size of a copper film, the present inventors have found that it is advantageous to stabilize the copper film in a known state prior to the CMP process. If the state of the film at the time of CMP is ignored, the polish rates will vary as a function of elapsed time since deposition due to the self-annealing characteristics of the copper films observed by the present inventors. Therefore, to properly control the polish rate of the CMP process, the grain size of the deposited film when the CMP process is attempted should be in a known state. This known state may be achieved by performing the low-temperature annealing process prior to performing CMP of the workpiece, thereby effectively bypassing the self-annealing process. The low-temperature process fixes the metallization layer in the unknown state prior to performing the CMP process. As such, workpiece-to-workpiece consistency in the performance of the CMP process may be achieved.

If the CMP process is not performed prior to a low-temperature annealing of the copper film, then the CMP process should be undertaken at a predetermined time after the deposition of the film. In this manner, the CMP process is undertaken at a time at which the film characteristics are known to thereby ensure the desired workpiece-to-workpiece consistency.

Each of the disclosed embodiments of the method is particularly suitable for providing a copper metallization layer in combination with a low-K dielectric

material. Many low-K dielectric materials become unstable if subject to temperatures greater than about 250-300 degrees Celsius. As such, annealing at the traditional temperatures close to about 400 degrees Celsius may destroy these dielectrics. Since the method of the present invention suggests the annealing of the copper metallization layer at temperatures substantially below 400 degrees Celsius (even ambient room temperatures typically found in clean room environments), the method is particularly suitable for use in manufacturing semiconductor devices using both copper metallization and low-K dielectric materials. With respect to the first and second embodiments of the method noted above, the wafer is not subject to any elevated temperature process to anneal the copper layer. With respect to the third embodiment discussed above, the copper metallization may be annealed at an elevated temperature that is high enough to substantially accelerate the self-annealing process while being low enough so as not to corrupt the low-K dielectric material. Low-K dielectric materials suitable for use with such copper metallization layers include, but are not limited to, fluorinated silicon dioxide, polyimides, fluorinated polyimides, siloxanes, parylenes, Teflon AF, nanofoams, aerogels, xerogels. Such low-K dielectrics include commercially available organic polymer dielectrics such as: Avatrel (B.F. Goodrich); BCB and PFCB (Dow Chemical); Flare 1.0 and Flare 1.5 (Allied Signal); PAE2 (Schumacher); and PQ100 and PQ600 (Hitachi). In such instances, the annealing process may also be combined with the baking process required for the low-K dielectric.

The process illustrated in Figs. 2A – 2G indicate that the via 420 and trench 415 are formed together. However, it will be recognized that the structures may be generally formed and filled separately in accordance with the single-damascene process described above. In such instances, the via 420 is first plated in accordance with the steps set forth in Figs. 2A – 2F while the trench 415 is subsequently plated in accordance with the steps set forth in Figs. 2A – 2F after plating of the via 420 has been completed. In effect, the via 420 corresponds to the structure 405 during plating of the trench 415. The methods disclosed herein are suitable for both the single-damascene and dual-damascene processes described herein.

It is also possible to plate micro recessed structures other than those set forth above and employ the foregoing low temperature annealing processes. For example, recessed structures forming a pattern in a photoresist layer may be plated pursuant to other processes used to form copper micro-metallization layers and structures. In such processes, the seed/barrier layer is preferably only provided at the bottoms of the microstructures and does not cover the photoresist sidewalls. After the plating of the recessed microstructures, the copper is subject to annealing at room temperature or at an elevated temperature below about 100, substantially below the 400 degrees typically employed.

Figs. 6 and 7 illustrate the use of low-temperature annealing of a copper film to remove voids that may occur when the copper film is deposited into, for example, a recessed microstructure of a workpiece 490. In Fig. 6, one or more

material layers 500 have been patterned with one or more recessed microstructures, such as trench 505. The one or more material layers 500 may be comprised, for example, of a low-K dielectric material, a barrier layer, an adhesion layer, combinations of such layers, etc. One or more layers of copper film 510 are disposed over the upper surface of the layer 500 and in the trench 505. The copper film 510 may be comprised, for example, of a copper seed layer and a layer of copper that has been electro-deposited over the copper seed layer.

When attempting to fill a recessed microstructure, such as trench 505, the upper portion of the microstructure tends to fill before the lower portions of the microstructure have been filled. This results in a "pinch-off" condition that leaves a void region 515 within the microstructure. Such void regions 515 are undesirable and may effectively render the metallization disposed in the microstructure useless.

A low-temperature annealing of the copper film 510 may be used to close the void regions 515 that have formed within any microstructures due to the occurrence of a "pinch-off" condition. The present inventors have found that annealing temperatures of about 250 degrees Celsius and below are sufficient to eliminate such void regions 515. Annealing at temperatures of about 250 degrees Celsius and below has numerous advantages over the traditional high-temperature annealing at 400 degrees Celsius. First, such low

temperature annealing processes permit the use of low-K dielectrics that would otherwise be damaged at the higher temperatures that have been traditionally used. Second, low temperature annealing reduces the concerns with respect to differential expansion of the copper film 510 and underlying materials. Third, low temperature annealing produces films having a low resistivity even when the annealing time is relatively short. Fourth, the stabilized copper film assists in ensuring uniform application of subsequent CMP processes. Finally, low temperature annealing is easily controlled and is suitable for single workpiece or batch workpiece annealing processes. Fig. 7 illustrates what the workpiece of Fig. 6 looks like after being subjected to a low temperature annealing process.

Fig. 8 illustrates a preferred manner of heating the workpiece 490 during the low-temperature annealing process. As shown, heat is applied to one side of the workpiece 490, as illustrated by arrows 520, and is removed from the workpiece 490 from the opposite side, as illustrated by arrows 525. Preferably, heat is applied to or generated at the side of the workpiece 490 proximate the lower portions of the microstructure 505, and is removed from the workpiece at the upper surface of the copper film 510. This creates a temperature gradient through the cross-section of the workpiece 490. This temperature gradient is illustrated by temperature designations T1 through T5, where: $T1 > T2 > T3 > T4 > T5$. The temperature gradient through the copper

film 510 causes a stress gradient that provides a driving force that promotes re-crystallization of the copper film 510. This stress gradient is due to the fact that the thermal expansion of the copper film is constrained by (1) of underlying material layers and (2) the overlying film at lower temperature.

One factor that may be used to control the magnitude of temperature gradient across the workpiece is the temperature ramp rate that is used to apply the heat. Higher magnitude ramp rates will result in larger temperature gradients, particularly at the end of the ramp. This property is illustrated in Figs. 9 and 10 in which the ramp rate of Fig. 9 is greater than the ramp rate of Fig. 10.

Figs. 11- 15 illustrate various manners of heating a surface of the workpiece 490 to create the desired temperature gradient. In Fig. 11, the workpiece 490 is disposed on a hot plate 530 to heat a first side of the workpiece. Heat is removed from the opposite side of the workpiece 490 by directing a flow of a cooler gas, illustrated by arrows 535 across the workpiece. The temperature difference between the hot plate 530 and the cooler gas 535, as well as the flow rate of the gas, can be used to control the temperature gradient. Depending on the desired temperature gradient, a separate source of cooler gas may be unnecessary thereby allowing the use of ambient gas.

Fig. 12 illustrates a further manner of generating the desired temperature gradient. In this embodiment, the hot plate 530 is used to apply

heat to the first side of the workpiece 490. However, heat is extracted from the second side of the workpiece 490 by a heat sink 540 that, for example, may be cooled by a controlled flow of coolant, as illustrated by arrows 545. The temperature gradient may be controlled, for example, by regulating the temperature and flow of the coolant.

Radiant heating of the workpiece 490 using, for example, ultra-violet light is illustrated in Fig. 13. As shown, a source of ultra-violet light 550 is disposed above the workpiece 490 and radiates ultra-violent light energy, as shown at arrows 560 to generate heat at a first side of the workpiece. Heat may be removed from the second side of the workpiece 490 by any one of a variety of the apparatus. In the illustrated embodiment, heat is removed from the second side of the workpiece 490 by the heat sink 540 that is cooled by a controlled flow of coolant. A similar configuration is illustrated in Fig. 14 where the first side of the workpiece 490 is heated by a heating element 565.

A high-precision apparatus for generating the desired temperature gradient is illustrated in Fig. 15. In this embodiment, a laser 570 is connected for two-dimensional movement to a laser position drive mechanism 575. Control of the position of the laser 570 by the drive mechanism 575 is effected by a programmable control system 580.

The laser 570 is disposed to direct laser light toward a first side of the workpiece 490 to generate heat at the first side. The laser 570 may be

dynamically positioned during the annealing process to selectively heat predetermined portions of the first side for predetermined periods of time. The laser position, laser light intensity, and time duration used for annealing the predetermined portions of the first side may be, for example, set by a recipe that is entered by the user. One or more temperature sensors may be disposed at the first side of the workpiece to effect temperature feedback control of the annealing process, as illustrated at line 585.

Heat is removed at the second side of the workpiece 490 by the heat sink 540. Accurate control of the temperature of the heat sink 540 and, thus, the temperature gradient, may be effected by accurately controlling the temperature and flow rate of the coolant. In the illustrated embodiment, the flow of coolant is regulated by a flow regulator 590 that is under the control of the control system 580. Higher coolant flow rates through the heat sink 540 typically result in larger temperature gradients while lower coolant flow rates typically result in smaller temperature gradients. As such, programming within the control system 580 may actuate the flow regulator 590 to limit coolant flow when the temperature gradient, or a measured parameter related thereto, exceeds a predetermined recipe value and to increase coolant flow when the temperature gradient, or a measured parameter related thereto, falls below a predetermined recipe value. Flow regulation may also be obtained by replacing flow regulator 590 with a pump mechanism.

One or more measurable parameters may be used as a basis for controlling the coolant flow. For example, a temperature sensor 595 may be used to measure the temperature of the coolant as it exits the heat sink 540. The output of the temperatures sensor 595 may be applied as an input to the control system 580 to effect coolant flow and/or coolant temperature. Alternatively, or in addition, a temperature sensor 600 may be used to measure the temperature of the coolant as it enters the heat sink 540. In instances in which both temperature sensors 595 and 600 are utilized, the control system 580 may use the temperature difference between the entering and exiting coolant to calculate the amount of heat extracted at the second side of the workpiece 490. This calculated heat value, in turn, may be used to control the laser light intensity and coolant flow rate according to a user programmed recipe, a multi-variable system model, recipe/model combinations, etc.

One or more of the foregoing heating systems may be integrated with a wet-chemical processing tool that is capable of electrochemical deposition of copper. Once such processing tool is the LT-210™ electroplating apparatus available from Semitool, Inc., of Kalispell, Montana. Figs. 16 and 17 illustrate such integration.

The system of Fig. 16 includes a plurality of processing stations 610. Preferably, these processing stations include one or more rinsing/drying stations and one or more electroplating stations, although further wet-chemical

processing stations may also be employed. The system also preferably includes an annealing station, such as at 615, for executing a low-temperature annealing process on each workpiece. The annealing process may be executed in a single-wafer or batch processing fashion. The workpieces are transferred between the processing stations 610 and the annealing station 615 using one or more robotic arms 620 that are disposed for linear movement along a central track 625.

Fig. 17 illustrates a further manner in which an annealing station 630 may be integrated in a wet-chemical processing tool set. Unlike the embodiment of Fig. 16, this embodiment employs a separate heating unit 635 that is serviced by a dedicated robotic mechanism 640. The dedicated robotic mechanism 640 accepts workpieces that are transferred to it by the robotic mechanisms 620. Transfer may take place through an intermediate staging door/area 645. As such, it becomes possible to hygienically separate the annealing station 630 from other portions of the tool set. Additionally, the illustrated annealing station may be implemented as a separate module that is attached to upgrade an existing tool set.

Numerous modifications may be made to the foregoing system without departing from the basic teachings thereof. Although the present invention has been described in substantial detail with reference to one or more specific embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the scope and spirit of the invention.



CLAIMS

1. A method for filling recessed micro-structures at a surface of a semiconductor workpiece with copper metallization comprising the steps of:

depositing a copper layer into the micro-structures with a process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures;

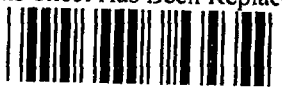
subjecting the deposited copper to an annealing process at a temperature below about 100 degrees Celsius.

2. A method as claimed in claim 1 wherein the copper is deposited using an electroplating process.

3. A method as claimed in claim 1 wherein an electroplating waveform is used, at least in part, to ensure sufficiently small copper grain size.

4. A method as claimed in claim 1 wherein an electroplating solution additive is used, at least in part, to ensure sufficiently small copper grain size.

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5. A method as claimed in claim 1 wherein the annealing process is carried out at ambient room temperature.

6. A method as claimed in claim 1 wherein the annealing process comprises subjecting the workpiece to a controlled temperature gradient in which the temperature decreases along a cross-section of the workpiece in a direction that is opposite to the direction of formation of the copper during its deposition.

7. A method for filling recessed micro-structures at a surface of a semiconductor workpiece with metallization comprising the steps of:

depositing a metal layer into the micro-structures with a process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures;

subjecting the deposited metal to an annealing process at a temperature below about 100 degrees Celsius.

8. A method as claimed in claim 7 wherein the metal is deposited using an electroplating process.

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9. A method as claimed in claim 7 wherein an electroplating waveform is used, at least in part, to ensure sufficiently small metal grain size.

10. A method as claimed in claim 7 wherein an electroplating solution additive is used, at least in part, to ensure sufficiently small metal grain size.

11. A method as claimed in claim 7 wherein the annealing process is carried out at ambient room temperature.

12. A method as claimed in claim 7 wherein the annealing process comprises subjecting the workpiece to a controlled temperature gradient in which the temperature decreases along a cross-section of the workpiece in a direction that is opposite to the direction of formation of the copper during its deposition.

13. A method for filling recessed micro-structures at a surface of a semiconductor workpiece with copper metallization comprising the steps of:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed micro-structures in the at least one dielectric layer;

preparing a surface of the workpiece including the recessed micro-structures with a seed layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer to the surface of the workpiece to substantially fill the recessed micro-structures;

allowing the electrochemically deposited copper layer to self-anneal for a predetermined period of time at ambient room temperature;

removing copper metallization from the surface of the workpiece except from the recessed microstructures, said removing step occurring after the predetermined period of time has elapsed.

14. A method as claimed in claim 13 wherein the predetermined period is greater than about 20 hours.

15. A method as claimed in claim 13 wherein the step of preparing a surface of the workpiece comprises:

applying at least one barrier layer over the dielectric layer; and

applying a seed layer over the barrier layer.

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16. A method as claimed in claim 15 wherein the step of applying the seed layer is defined by applying the seed layer using a chemical vapor deposition process.

17. A method as claimed in claim 15 wherein the step of applying the seed layer is defined by applying the seed layer using a physical vapor deposition process.

18. A method as claimed in claim 13 wherein the step of preparing a surface of the workpiece comprises:

applying at least one adhesion layer over the dielectric layer; and

applying a seed layer over the adhesion layer.

19. A method as claimed in claim 13 wherein the step of removing the copper metallization is defined by removing the copper metallization using a chemical mechanical polish technique.

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20. A method for filling recessed micro-structures at a surface of a semiconductor workpiece with copper metallization comprising the steps of:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed micro-structures in the at least one dielectric layer;

preparing a surface of the workpiece including the recessed micro-structures with a seed layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer to the surface of the workpiece to substantially fill the recessed micro-structures;

removing copper metallization from the surface of the workpiece except from the recessed micro-structures;

allowing the electrochemically deposited copper layer to self-anneal at ambient room temperature without subjecting the workpiece to a separate and distinct elevated temperature annealing process.

21. A method as claimed in claim 20 wherein the step of preparing a surface of the workpiece comprises:

applying at least one adhesion layer over the dielectric layer; and

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applying a seed layer over the adhesion layer.

22. A method as claimed in claim 20 wherein the step of preparing a surface of the workpiece comprises:

applying at least one barrier layer over the dielectric layer; and

applying a seed layer over the barrier layer.

23. A method as claimed in claim 22 wherein the step of applying the seed layer is defined by applying the seed layer using a chemical vapor deposition process.

24. A method as claimed in claim 22 wherein the step of applying the seed layer is defined by applying the seed layer using a physical vapor deposition process.

25. A method as claimed in claim 20 wherein the step of removing the copper metallization is defined by removing the copper metallization using a chemical mechanical polish technique.

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26. A method for filling recessed micro-structures at a surface of a semiconductor workpiece with copper metallization comprising the steps of:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed micro-structures in the at least one dielectric layer;

preparing a surface of the workpiece, including the recessed micro-structures, with a seed layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer to the surface of the workpiece to substantially fill the recessed micro-structures;

subjecting the electrochemically deposited copper layer to an annealing process at a temperature below about 100 degrees Celsius.

27. A method as claimed in claim 26 wherein the step of preparing a surface of the workpiece comprises:

applying at least one adhesion layer over the dielectric layer; and

applying a seed layer over the adhesion layer.

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28. A method as claimed in claim 26 wherein the step of preparing a surface of the workpiece comprises:

applying at least one barrier layer over the dielectric layer; and

applying a seed layer over the barrier layer.

29. A method as claimed in claim 28 wherein the step of applying the seed layer is defined by applying the seed layer using a chemical vapor deposition process.

30. A method as claimed in claim 28 wherein the step of applying the seed layer is defined by applying the seed layer using a physical vapor deposition process.

31. A method as claimed in claim 26 wherein the step of removing the copper metallization is defined by removing the copper metallization using a chemical mechanical polish technique.

32. A method as claimed in claim 26 wherein the annealing process comprises subjecting the workpiece to a controlled temperature gradient in which the temperature decreases along a cross-section of the

workpiece in a direction that is opposite to the direction of formation of the copper during its deposition.

33. A method for filling recessed micro-structures at a surface of a semiconductor workpiece with copper metallization comprising the steps of:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one low-K dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed micro-structures in the at least one low-K dielectric layer;

preparing a surface of the workpiece, including the recessed micro-structures, with a seed layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer to the surface of the workpiece to substantially fill the recessed micro-structures;

subjecting the electrochemically deposited copper layer to an annealing process at a temperature below which the low-K dielectric layer substantially degrades.

34. A method as claimed in claim 33 wherein the annealing process comprises subjecting the workpiece to a controlled temperature gradient

in which the temperature decreases along a cross-section of the workpiece in a direction that is opposite to the direction of formation of the copper during its deposition .

35. A method as claimed in claim 33 wherein the annealing step takes place at a temperature corresponding to a baking temperature of the low-K dielectric.

36. A method for reducing voids in a metal material that has been electrolytically deposited into recessed micro-structures of a microelectronic workpiece comprising the step of subjecting the workpiece to an annealing process at a temperature that is at or below about 250 degrees Celsius.

37. A method as set forth in claim 36 wherein the metal material comprises copper.

38. A method as set forth in claim 36 wherein the annealing process comprises subjecting the workpiece to a controlled temperature gradient in which the temperature decreases along a cross-section of the

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workpiece in a direction that is opposite to the direction of formation of the metal material during its deposition .

39. A method as set forth in claim 37 wherein the annealing process comprises subjecting the workpiece to a controlled temperature gradient in which the temperature decreases along a cross-section of the workpiece in a direction that is opposite to the direction of the formation of the deposited metal material.

40. A method for reducing voids in a metal material that has been electrolytically deposited into recessed micro-structures of a microelectronic workpiece comprising the step of subjecting the workpiece to an annealing process in which the workpiece is subject to a controlled temperature gradient in which the temperature decreases along a cross-section of the workpiece in a direction that is opposite to the direction of the formation of the deposited metal material.

41. An apparatus for use in applying metallization in recessed micro-structures of a microelectronic workpiece comprising:

at least one deposition station for depositing a conductive material into at least the recessed micro-structures of the microelectronic workpiece;

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at least one annealing station for subjecting the microelectronic workpiece to an annealing temperature that is at or below about 250 degrees Celsius.

42. An apparatus as set forth in claim 41 wherein the at least one deposition station electrolytically deposits the conductive material and wherein the conductive material comprises copper.

43. An apparatus as set forth in claim 41 and further comprising a robotic workpiece handling system for transferring microelectronic workpieces to and from the at least one deposition station and to or from the least one annealing station.

44. An apparatus as set forth in claim 42 wherein the workpiece handling system comprises:

a first robot arm disposed to transfer the microelectronic workpieces to and from the at least one deposition station;

a second robot arm disposed to transfer the microelectronic workpieces to and from the at least one annealing station.

45. An apparatus as set forth in claim 41 wherein the at least one annealing station operates to subject the workpiece to a controlled temperature

gradient in which the temperature decreases along a cross-section of the workpiece in a direction that is opposite to the direction in which the metal material is formed at the at least one deposition station.

46. An apparatus as set forth in claim 42 wherein the at least one annealing station operates to subject the workpiece to a controlled temperature gradient in which the temperature decreases along a cross-section of the workpiece in a direction that is opposite to the direction in which the metal material is formed at the at least one deposition station.

47. An apparatus as set forth in claim 41 wherein the at least one annealing station comprises:

a heated generator proximate a first side of the workpiece to heat the first side of the workpiece; and

a fluid flow system directing a flow of cooling fluid at a second side of the workpiece, opposite the first side, to thereby generate a temperature gradient between the first and second sides of the workpiece.

48. An apparatus as set forth in claim 47 wherein the fluid flow system directs a cooling gas across the second surface of the workpiece.

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49. An apparatus as set forth in claim 47 wherein the fluid flow system comprises:

a cooling member proximate a second side of the microelectronic workpiece for cooling the second side of the workpiece ; and

at least one channel associated with the cooling member for directing a flow of cooling gas therethrough to cool the cooling member.

50. An apparatus as set forth in claim 47 wherein the heat generator comprises a hot plate contacting the first side of the microelectronic workpiece.

51. An apparatus as set forth in claim 47 wherein the heat generator comprises an ultraviolet radiation source disposed to direct ultraviolet radiation toward the first side of the microelectronic workpiece.

52. An apparatus as set forth in claim 47 wherein the heat generator comprises radiative heat source disposed at the first side of the microelectronic workpiece.

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53. An apparatus as set forth in claim 47 wherein the heat generator comprises a laser source disposed to selectively direct laser radiation at selective portions of the first side of the microelectronic workpiece.

54. An apparatus as set forth in claim 41 and further comprising a programmable control system connected to control the magnitude of the temperature gradient.

55. An apparatus for use fabricating metallization in recessed micro-structures of a microelectronic workpiece comprising:

at least one deposition station for depositing a conductive material into at least the recessed micro-structures of the microelectronic workpiece;

at least one annealing station for subjecting the microelectronic workpiece to an annealing process in which the workpiece is subject to a controlled temperature gradient.

56. An apparatus as claimed in claim 55 in which the temperature gradient is such that the temperature decreases along a cross-section of the workpiece in a direction that is opposite to the direction of the formation of the deposited metal material.

57. An apparatus as set forth in claim 55 wherein the at least one deposition station electrolytically deposits the conductive material and wherein the conductive material comprises copper.

58. An apparatus as set forth in claim 55 and further comprising a robotic workpiece handling system for transferring microelectronic workpieces to and from the at least one deposition station and to or from the least one annealing station.

59. An apparatus as set forth in claim 58 wherein the workpiece handling system comprises:

a first robot arm disposed to transfer the microelectronic workpieces to and from the at least one deposition station;

a second robot arm disposed to transfer the microelectronic workpieces to and from the at least one annealing station.

60. An apparatus as set forth in claim 55 wherein the at least one annealing station comprises:

a heated generator proximate a first side of the workpiece to heat the first side of the workpiece; and

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a fluid flow system directing a flow of cooling fluid at a second side of the workpiece, opposite the first side, to thereby generate a temperature gradient between the first and second sides of the workpiece.

61. An apparatus as set forth in claim 55 wherein the fluid flow system directs a cooling gas across the second surface of the workpiece.

62. An apparatus as set forth in claim 55 wherein the fluid flow system comprises:

a cooling member proximate a second side of the microelectronic workpiece for cooling the second side of the workpiece ; and

at least one channel associated with the cooling member for directing a flow of cooling gas therethrough to cool the cooling member.

63. An apparatus as set forth in claim 55 wherein the heat generator comprises a hot plate contacting the first side of the microelectronic workpiece.

64. An apparatus as set forth in claim 55 wherein the heat generator comprises an ultraviolet radiation source disposed to direct ultraviolet radiation toward the first side of the microelectronic workpiece.

65. An apparatus as set forth in claim 55 wherein the heat generator comprises radiative heat source disposed at the first side of the microelectronic workpiece.

66. An apparatus as set forth in claim 55 wherein the heat generator comprises a laser source disposed to selectively direct laser radiation at selective portions of the first side of the microelectronic workpiece.

67. An apparatus as set forth in claim 55 and further comprising a programmable control system connected to control the magnitude of the temperature gradient.

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