Combination of Terminator Apparatus Enhancements

ABSTRACT

An SCSI bus line 14a apparatus including in combination at least two of any of an active deassertion (ADR) circuit, a signal line impedance matching (SLIM) circuit 310 and a signal line increased circuit kicker (SLICK) circuit (110). In the ADR circuit, if a current sinking circuit senses an increased voltage on the common node of the signal lines of a bus due to active deassertion of a signal line, the current sinking circuit sinks enough current from the signal lines to prevent an over-current condition on asserted signal lines or soon-to-be asserted signal lines. In the SLIM circuit 310, transient voltages are removed from a signal line by limiting to within a range the voltages that can appear on the signal line. In the SLICK circuit 110, a current switching device is controlled to provide current to raise the voltage level of a notch occurring in a signal on a signal line when the line is deasserted, but is responsive to a monitoring circuit for disconnecting the current when a programmed length of time has been exceeded after assertion.

Figure 3.

This Sheet Has Been Replaced

