9903990-1

reference copy

THIS SHEET HAS BEEN REPLACED

Multi-Chip Module With Extension

Background

This invention relates generally to multi-chip modules for coupling more than one chip together in a single package.

For a number of reasons, it is desirable to package more than one integrated circuit die or chip in a single package. In some cases, the two dice may necessitate different processing technologies. In such case, the two dice must be made independently and then combined thereafter. For example, one die may be made using a bipolar process and another may be made using a complementary metal oxide semiconductor (CMOS) process. Similarly, one die may use a logic process and the other die may use a memory process. For example, some dice may use stacked gate designs which may be incompatible with logic processes.

Thus, in a variety of situations, it may be desirable to put components in close proximity without making them on the same integrated circuit fabrication process. In addition, in some cases, the level of integration available may be such that to achieve the full capabilities, separate dice must be used. If separate dice are used, it may still be desirable to connect the dice together to the outside world through a single set of input and output connections. These input and output connections may be, for example, pins or solder balls. In some cases it may be desirable to interconnect the two dice to each other and then to interconnect them together to the outside world.

Thus, there is a need for packages which enable dice to be connected together before connection to the outside world.

Summary

In accordance with one aspect, a multi-chip module includes a laminate layer having a top and a bottom sides and a central passage. A first chip is secured to the bottom side of the layer. The first chip is wire bonded to the top side of the layer through the passage. A second chip is secured to the top side of the layer by bumps. The layer includes an extension accessible beyond one of the chips. The extension includes contacts which may be coupled to at least one of the first and second chips.

9903990-1

This Sheet Has Been Replaced

17 AUG 1999

THIS SHEET HAS BEEN REPLACED

Other aspects are described in the accompanying specification and claims.

Brief Description of the Drawings

Fig. 1 is a greatly enlarged cross-sectional view of one embodiment of the present invention;

Fig. 2 is a greatly enlarged cross-sectional view of a subassembly, in accordance with the embodiment shown in Fig. 1, after a first chip has been connected to a laminate layer and the assembly wire bonded;

Fig. 3 is a greatly enlarged cross-sectional view of the embodiment shown in Fig. 2 after a second chip has been attached;

Fig. 4 is a greatly enlarged cross-sectional view of the package of Fig. 3 after it has been subject to encapsulation;

Fig. 5 is a greatly enlarged bottom plan view of one embodiment of the present invention; and

Fig. 6 is a greatly enlarged bottom plan view of another embodiment of the present invention.

Detailed Description

Referring to Fig. 1, a multi-chip module 10 includes a first chip 16, a second chip 22 and a laminate layer 12 sandwiched between the first and second chips 16 and 22. The laminate layer 12 provides one or more layers of conductive traces separated by insulators and coupled by vias to enable interconnection between the first chip 16, the second chip 22 and external devices (not shown).

The laminate layer 12 includes an upper side 30, a lower side 32 and central passage 14. The central passage may extend along the length of the module 10 in a rectangular arrangement, in one embodiment of the invention.

As shown in Fig. 1, the laminate layer 12 may extend outwardly beyond both of the first and second chips 16 and 22 to form an extension 40. The extension 40 provides a contact surface to make contact with external devices.

The first chip 16 may be coupled to the laminate layer 12 by extending wire bond wires 20 through the central passage 14 to the pads 34 on the upper surface 30 of the laminate layer 12,

THIS SHEET HAS BEEN REPLACED

as shown in Fig. 2. The first chip 16 may be physically coupled to the second chip 22 by an adhesive layer 18. The adhesive layer 18 may conventionally be an adhesive tape strip which adhesively secures the upper surface of the first chip 16 to the lower surface 32 of the laminate layer 12.

The second chip 22 may be coupled to the laminate layer 12 directly using bumps 24 which may be formed of solder balls. As illustrated, the bumps 24 may be of substantially smaller diameter than the bumps 28 provided for connecting the entire module 10 to external devices.

In this way, a relatively low profile multi-chip module may be fabricated. For example, by way of illustration only, in one embodiment of the present invention, the first and second chips 16 and 22 may be on the order of .25 millimeters thick, the laminate layer 12 may be on the order of .25 millimeters thick and the spacing between the first and second chips may be on the order of 0.1 millimeters in the case of the second chip 22 and .075 millimeters in the case of the first chip 16. This gives an overall height of less than one millimeter. If the solder bumps 28 are on the order of .5 millimeters in diameter, the overall height of the assembly may be on the order of about one millimeter, for example .85 millimeter. Thus, a relatively compact, low profile assembly may be fashioned using the winged extension 40.

Referring now to Fig. 2, the sequence of assembling the multi-chip module 10 is illustrated. Initially the first chip 16 is secured by adhesive tape 18 to the lower surface 32 of the laminate layer 12. Wire bond wires 20 extend through the passage 14 to couple the pads 34 on the upper surface 30 of the laminate layer 12 to the first chip 16.

Turning next to Fig. 3, the second chip 22 may be surface mounted on the laminate layer 12 using solder balls 24. After a reflow step, the solder balls 24 soften sufficiently to secure the second chip 22 to be contacts 44 on the upper surface of the laminate layer 12.

Thereafter, the entire assembly is placed in an encapsulation mold, in one embodiment of the present invention, forming the encapsulant 26 in the regions between the first and second chips 16 and 22, as shown in Fig. 4. This leaves the extension 40 extending outwardly from the rest of the package. Alternatively, the gaps between the chips 16 and 22 may be filled up with underfill material.

THIS SHEET HAS BEEN REPLACED

For example, in one embodiment of the present invention, solder balls or bumps 28 may be electrically coupled by contacts 52 or 62 to a trace 48 or 58 by way of a via 50 or 60. The traces 48 and 58 in turn may be coupled to contacts 54 or 44 on the upper surface 30 of the laminate layer 12 by way of a via, 56 or 46.

Finally, the solder balls 28 or other interconnection devices are secured to the extensions 40. In this way, external devices may be contacted by the solder balls 28, making electrical connections to one or more of the first and second chips 16 and 22 through the laminate layer 12.

Referring to Fig. 5, in one embodiment of the present invention, the extension 40 may extend outwardly from each opposed edges 41 of the module 10. Solder balls 28 may be aligned along each side in the length direction of the extension 40. In some embodiments, each extension 40 may extend outwardly beyond than the approximate width of one solder ball 28 so that a plurality of solder balls may be coupled, two or more solder balls deep, along the edges 41 of the module 10.

Referring to Fig. 6, in accordance with still another embodiment of the present invention, the extension 40 may extend around all four edges 41 of the module 10. In this way, solder balls 28 may be coupled along four edge portions 41a-d to increase the number of connections that may be made. Again, the extension 40 may extend further outwardly to allow solder balls to be attached, two or more deep, along the edges 41 of the module 10.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

This Sheet Has Been Replaced



This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

1. A multi-chip module comprising:

a laminate layer having top and bottom sides and a central passage;

a first chip secured to the bottom side of said layer, said first chip wire bonded to the top side of said layer through said passage;

a second chip secured to the top side of the layer and coupled by bumps to said layer; and

said layer including an extension beyond at least one of said chips, said extension including contacts.

2. The module of claim 1 wherein said contacts are contacted by solder balls.

3. The module of claim 1 including a pair of opposed extensions each extending outwardly beyond the rest of the module and each having contacts.

4. The module of claim 1 wherein said extension extends all the way around said module.

5. The module of claim 1 wherein said first chip is bonded to said layer using adhesive securement.

6. The module of claim 5 wherein said adhesive securement is adhesive tape.

7. The module of claim 1 wherein the overall height of said module is approximately one millimeter or less.

8. The module of claim 1 wherein said first and second chips are aligned one over the other and centered over said passage.

9. The module of claim 8 wherein said passage is centered in said layer.

* C L M S *

10. The module of claim 1 wherein said package has bilateral symmetry.

11. The module of claim 1 wherein said region between said first and second chips is filled with encapsulant.

12. The module of claim 1 wherein said extension extends outwardly beyond said first and second chips.

13. A method of forming a multi-chip module comprising:

adhesively securing a first chip to a first surface of a laminate layer;

inverting the assembly of said laminate layer and said first chip;

wire bonding said first chip to a second surface of said laminate layer;

securing a second chip to the second surface of said laminate layer using bumps;

positioning said first and second chips on said laminate layer so that at least a portion of said laminate layer extends outwardly beyond said first and second chips; and

providing an electrical contact on said extension.

14. The method of claim 13 including aligning said first and second chips over one another.

15. The method of claim 14 including providing a pair of extensions extending outwardly beyond said first and second chips.

16. The method of claim 14 including aligning said chips so as to form an extension of said laminate layer that extends outwardly beyond said chips and completely around said module.

17. The method of claim 15 including providing solder balls on said contacts on said extensions.



18. The method of claim 13 including filling a region between said chips with an encapsulant.

19. The method of claim 18 including forming a passage through said laminate layer and forming wire bonds from said first chip through said passage to the second surface of said laminate layer.

20. The method of claim 18 including coupling said contact and said first and second chips through traces extending through said laminate layer.

21. A multi-chip module comprising:

a central support layer having a top side and a bottom side, a bonding pad on each of said sides and conductive interconnections extending through said layer;

a first chip secured to the bottom side of said layer;

a second chip secured to the top side of said layer, said second chip secured by bumps to said layer; and

said layer extending outwardly beyond said first and second chips, said layer including a bonding pad on an extension extending outwardly beyond said first and second chips for connecting said chips to external devices.

22. The module of claim 21 wherein said layer is a laminate layer.

23. The module of claim 21 wherein said first chip is adhesively secured to said layer.

24. The module of claim 23 wherein said first chip is secured by adhesive tape to said layer.

25. The module of claim 21 wherein said layer includes a central aperture, said first chip wire bonded to the top side of said layer through said aperture.



26. The module of claim 21 including solder balls connected to said contacts on said bottom and top sides.

27. The module of claim 21 having an overall height of less than approximately 1 millimeter.

28. The module of claim 21 wherein said extension extends outwardly beyond said first and second chips in two directions.

29. The module of claim 21 wherein said layer extends beyond said chips completely around said chips.

30. The module of claim 21 wherein said first and second chips are aligned with one another and positioned centrally on said layer.

31. The module of claim 30 wherein a passage is formed centrally through said layer for wire bonding said first chip to said layer.

32. A method comprising:

coupling a first chip to a first side of a support structure;

coupling a second chip to a second side of said support structure;

causing said support structure to extend outwardly beyond the first chip; and

providing a bonding pad on the portion of said structure extending outwardly beyond said first chip.

33. The method of claim 32 wherein coupling a first chip includes adhesively coupling a first chip to said support structure.

34. The method of claim 33 wherein coupling a first chip includes wire bonding said first chip to bonding pads on said second side of said support structure.

CLMS *

35. The method of claim 32 wherein coupling a second chip includes bump bonding said second chip to said second side of said support structure.

36. The method of claim 32 wherein causing said support structure to extend outwardly includes causing said support structure to extend outwardly from two opposed edges of the first chip.

37. The method of claim 36 wherein causing said support structure to extend outwardly includes causing said support structure to extend outwardly beyond four edges of said first chip.

38. The method of claim 32 wherein causing said support structure to extend outwardly includes causing said support structure to extend outwardly beyond said first and second chips.

39. The method of claim 32 including coupling said first and second chips to said bonding pad on said portion via traces extending through said structure.

40. The method of claim 39 including coupling a solder ball to said bonding pad.

