IMPROVED SILICIDE FORMATION ON POLYSILICON

Abstract

An integrated circuit includes a doped polysilicon/silicide ("polycide") gate electrode. The doped polysilicon layer comprises sub-layers (41, 42, 43, 44). The sub-layers are formed by varying the silicon deposition conditions, typically including the deposition rate, while decreasing the dopant concentration. The metal silicide layer (45) is then formed on top of the doped polysilicon layer. An improvement in uniformity and planarity of the structure is obtained as a result of stress accommodation. In addition, the sub-layers reduce the channeling effect that occurs during high energy source/drain dopant implantation. These effects allow for a reduced stack height of the gate electrode, resulting in improvements in very small (sub-micron) device structures.

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