Description

This invention relates to error correction encoding apparatus, for example to such apparatus that may be employed in recording and/or reproducing systems for optical discs or the like.

In a disc apparatus employing an optical disc as a recording medium, such as a player for a compact disc (CD) having concentric tracks on which digital audio data, for example, are recorded as a string of pits, the tracks on the disc are irradiated by a laser beam, the disc is rotationally driven at a constant linear velocity (CLV) by a spindle motor, and changes in the intensity of the reflected light caused by the presence or absence of pits are detected for reproducing the digital audio data.

During data reproduction by the CD player, the error rate may reach a value in the order of 10^{-5}. In order to combat this, a cross-interleave Reed-Solomon code (CIRC), which is obtained by combining a Reed-Solomon code, an error correcting code having a high random error correcting ability, and means for converting a burst error into a random error using an interleaving technique, is used for error correction, so that no hindrances are produced under ordinary operating environments.

A previously proposed audio data recording system which uses CIRC, such as disclosed in EP-A-0 342 833, employs an encoding apparatus 110 arranged and constructed as shown in Figure 9 of the accompanying drawings. Digital audio data are inputted to the encoding apparatus 110 in parallel, with 6 samples, that is 16 x 2 x 6 which equals 192 bits or 24 bytes, for each of left and right channels, as one unit. These input data are rearranged after the data of even-numbered samples are delayed by a scrambling circuit by two CIRC units. The input data, rearranged by a scrambling circuit 111, are subjected to encoding with a first error correction code C2 by a first error code generator 112, and supplied to an interleaving circuit 113 after the parity Q of a Reed-Solomon code where m=8, n=28, k=24 and d=5 is appended thereto. The interleaving circuit 113 applies different amounts of delay to the data such that the maximum amount of delay of 108 frames is applied for interleaving. The parity P of a Reed-Solomon code where m=8, n=32, k=28 and d=5 is appended to the data interleaved by the circuit 113, by way of encoding with a second error correction code C1 by way of a second error correction code generator 114. The input data, to which the parities Q and P have been appended in the above manner, are processed by an odd number delay circuit 115 where only odd-numbered symbols are further delayed by one symbol and the signs of the parities Q and P are inverted to provide a 32 byte long CIRC encoded output which is to be recorded.

A previously proposed reproducing system for digital audio data, which uses the above-described CIRC, employs a decoding apparatus 120 as shown in Figure 10 of the accompanying drawings. In the decoding apparatus 120, playback (reproduced) data encoded by the encoding apparatus 110 are supplied to an even-number delay circuit 121 where even-numbered symbols are delayed by one frame, and the signs of the parities Q and P are inverted. Error correction is performed in a first error correction circuit 122 by the second error correction code C1 on the basis of the parity P. The playback data, thus error corrected by the first error correcting circuit 122, are deinterleaved by a deinterleaving circuit 123 which applies a delay, which is an inversion of that applied by the interleaving circuit 113 of the encoding apparatus 110, before being supplied to a second error correcting circuit 124. The second error correcting circuit 124 performs error correction by a first error correcting code C2 on the basis of the parity Q. The playback data, thus error-corrected by the first error correcting code C1 and the second error correcting code C2, are descrambled by a descrambling circuit 125 by data rearrangement corresponding to that performed by the scrambling circuit 111 in the encoding apparatus 110.

The above-described encoding and decoding apparatus 110 and 120 have been constructed as integrated circuits and extensively used as an encoder and decoder for CIRC processing.

There has been prescribed for the compact disc (CD) a data format in which 24 channel bit synchronising signals, produced as eight to fourteen modulation (EFM) data converted from 8-bit-per-symbol signals, are converted into 14 channel bit data, 14 channel bit or 1-symbol sub-code, 14 32 channel bit or 32 symbol data per se, such as play data and parity data, and each 3 channel bit margin bits provided between adjacent symbols, totalling 588 channel bits, are arranged as one frame and 98 frames are arranged as a sub-code block.

It is to be noted that, in a so-called CD-interactive (CD-I) system for the compact disc (CD) for simultaneously recording image data, letter data etc. as well as audio data, six modes have been prescribed besides the so-called CD-DA mode as used, for example, for audio data, as shown in Figure 11 of the accompanying drawings.

Thus, for the CD-DA mode having a sound quality level corresponding to the current 16-bit pulse code modulation (PCM), straight PCM with a sampling frequency of 44.1 kHz and a number of quantising bits equal to 16 is used. For an A level stereo mode and an A level monaural mode having a sound quality corresponding to a long-playing record, adaptive differential pulse code modulation (ADPCM) with a sampling frequency of 37.8 kHz and a number of quantising bits equal to 8 is used. For a B level stereo mode and a B level monaural mode having a sound quality corresponding to FM broadcasting, adaptive PCM or

ADPCM having a sampling frequency of 37.8 kHz and a number of quantising bits equal to 4 is used. Finally, for a C level stereo mode and a C level monaural mode having a sound quality corresponding to AM broadcasting, ADPCM with a sampling frequency of 18.9 kHz and a number of quantising bits equal to 4 is used.

That is, referring to Figure 11, where a cross-hatched rectangular mark denotes a sector where data are not recorded, the bit reduction rate for the A level stereo mode is one-half that of the CD-DA mode, so that data are recorded at every other sector, the playback time of the disc being approximately two hours. For the A level monaural mode, the bit reduction rate is 1/4 and data are recorded at every four sectors, the playback time of the disc being about four hours. For the B level stereo mode, the bit reduction rate is 1/4 and data are recorded at every four sectors, the playback time for the disc being about four hours. For the B level stereo mode, the bit reduction rate is 1/8 and data are recorded at every eight sectors, the playback time for the disc being about eight hours. For the C level stereo mode, the bit reduction rate is 1/8 and data are recorded at every eight sectors, the playback time for the disc being about eight hours. For the C level monaural mode, the bit reduction rate is 1/16 and data are recorded at every 16 sectors, the playback time for the disc being about 16 hours.

In the digital audio data reproducing system employing the above-described CIRC, if burst errors beyond the correction capabilities should occur in playback data, the errors are distributed evenly throughout an interleaving length and thereby rendered less manifest. With a CD player handling continuous PCM audio data, error data may be interpolated by nearby data, so that foreign sounds are less likely to be produced. However, if the data are data lacking in correlation between adjacent data, or compressed audio data according to the above-mentioned CD-I system, it is not possible to correct errors in the playback data by using nearby data. Therefore, if burst errors in excess of the correction capabilities are produced in the playback data and the errors are evenly distributed throughout the interleaving length, the errors occur discretely for the interleaving length, that is for a time longer than 14.7 ms for the CD-DA mode, so that more data than the errors per se become unusable.

According to a first aspect of the invention as defined in claim 1 there is provided an error correction encoding apparatus for processing an input data word series with encoding for error correction, the apparatus comprising:

first delay means for applying different amounts of delay to respective data words constituting a data block for converting the input data word series in a first array state into an input data word series in a second array state;

first error correction encoding means for generating a first check words series from the data word series in said second array state;

second delay means for applying different amounts of delay to the data word series in said second array state and to the first check word series for converting said data word series and said check word series into a data word series and a check word series in a third array state; and

second error correction encoding means for generating a second check word series from said data word series and said check word series in the third array state;

the amounts of delay applied by said first and second delay means being set so that the array state of said data word series in said third array state is the same as the array state of said data word series in said first array state.

According to a second aspect of the invention as defined in claim 6 there is provided an error correction decoding apparatus for executing an error correction decoding operation on an input data word series on which error correction encoding has been executed such that different amounts of delay are applied to data words constituting a data block of a data word series in a first array state for converting said data word series into a data word series in a second array state, first check word series are generated from the data word series in said second array state, different amounts of delay are applied to said data word series and said first check word series in said second array state for converting said data word series and said check word series into a data word series and a check word series in a third array state, and second check word series are generated from the data word series and the check word series in the third array state, the amounts of delay being such that the data word series in said third array state is equal to the array state of said data word series in said first array state, said apparatus comprising:

first error correction decoding means for processing the data word series constituting a data block of the input data word series in said third array state and the first check word series by error correction by an error correction code using said second check word series;

first delay means for applying different amounts of delay to said data word series and the check word series corrected for errors by said first error correction decoding means for converting said data word series and the first check word series into the data word series and the first check word series in said second array state;

second error correcting decoding means for error-correcting said data word series in said second array state by an error correction code using said first check word series; and

second delay means for applying different amounts of delay to said data word series corrected

for errors by said second error correcting decoding means for converting said data word series into a data word series in said first array state, the amounts of delay applied by said first and second delay means being set so that the array state of said data word series in said first array state is the same as the array state of said data word series in said third array state.

Preferred embodiments of the invention described in detail below provide an encoding apparatus and a decoding apparatus in which the correction capabilities provided by the customary CIRC are maintained and in which, should burst errors exceeding the correction capabilities be produced in playback data, the errors are not distributed throughout the interleaving length.

The invention will now be further described, by way of illustrative and non-limiting example, with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of an encoding apparatus embodying the invention;

Figure 2 is a block diagram of a decoding apparatus embodying the invention;

Figure 3 is a block diagram of a modified encoding apparatus embodying the invention;

Figure 4 is a block diagram of a modified decoding apparatus embodying the invention;

Figure 5 is a block diagram of a disc recording and/or reproducing apparatus which uses an encoding apparatus and a decoding apparatus embodying the invention;

Figure 6 shows a data format employed in the disc recording and/or reproducing apparatus shown in Figure 5;

Figure 7 shows the state of a controlled memory of a recording system of the disc recording and/or reproducing apparatus shown in Figure 5;

Figure 8 shows the state of a controlled memory of a reproducing system of the disc recording and/or reproducing apparatus shown in Figure 5;

Figure 9 is a block diagram of a previously proposed encoding apparatus used in a CD player;

Figure 10 is a block diagram of a previously proposed decoding apparatus used in a CD player; and

Figure 11 shows CD-I data formats.

An encoding apparatus and a decoding apparatus embodying the invention will now be explained in detail with reference to the drawings.

The encoding apparatus and the decoding apparatus embodying the invention are applied to an encoder of a recording system and to a decoder of a reproducing system, respectively, of an optical disc recording and/or reproducing system for recording and/or reproducing digital audio data, such as that shown for example in Figure 5 and described in more detail below.

The encoding apparatus (encoder) is shown at 30 in Figure 1 and includes a first delay circuit 32 applying different amounts of delay to data of respective bits constituting each data block, a first check word generating circuit 33 for generating a first check word by a first error correction code for the data of the respective bits from the first delay circuit 32, a second delay circuit 34 for applying different amounts of delay to the data of the respective bits from the first delay circuit 32, and a second check word generating circuit 35 for generating a second check word by a second error correction code.

The encoding apparatus 30 shown in Figure 1 is designed for processing digital audio data conforming to the CD standard by an encoding operation equivalent to the above-mentioned CIRC. To the encoding apparatus 30 there are inputted in parallel 6 samples, that is 16 bits x 2 x 6 = 192 bits or 24 bytes as one unit for each of the left and right channels. These input data are supplied to the first delay circuit 32 via an even-number delay circuit 31 for delaying even-numbered symbols by one frame.

The first delay circuit 32 applies different amounts of delay to the input data by way of an interleaving operation in which the maximum delay amounts to 108 frames at D=4.

The first check word generating circuit 33 is designed for processing the input data, thus interleaved by the first delay circuit 32, by an encoding operation with the first error correction code C2, for appending the parity Q of the Reed-Solomon code where m=8, n=28, k=24 and d=5 to the input data.

The second delay circuit 34 applies different amounts of delay to the interleaved data from the first delay circuit 32 so that the sum-total of the amounts of the delay applied to the data will be equal. That is, the delay circuit 34 resolves the interleaving applied by the first delay circuit 32.

The second check word generating circuit 35 processes the deinterleaved data from the second delay circuit 34 by encoding with the second error correction code C1 for appending the parity P of the Reed-Solomon code where m=8, n=32, k=28 and d=5 to the deinterleaved data. The data with the appended parities Q and P are processed by an even number delay circuit 36 which produces a one-frame delay for only odd-numbered symbols so that the same amounts of delay are applied to the data in their entirety. The parities Q and P are inverted in sign to provide a 32 byte CIRC encoded output which is to be recorded.

The encoded output from the above-described encoding apparatus 30 has correcting capabilities equivalent to those of the customary CIRC, because the parity Q generated by the first check word generating circuit 33 from the interleaved input data from the first delay circuit 32 and the parity P generated by the second check word generating circuit 35 from the second delay circuit 34 have been appended to the encoded output. In addition, since the same amount

of delay in sum-total is afforded to the data of the encoded output of the encoding apparatus by the first and second circuits 32, 34, while the encoded output is not interleaved, there is no risk of error distribution even if burst errors in excess of the correction capabilities should occur in the recording and/or reproducing system.

The decoding apparatus embodying the invention for decoding an encoded output produced by the encoding apparatus 30 is constructed as shown for example in Figure 2.

In the decoding apparatus, as shown at 40 in Figure 2, data reproduced from data encoded by the encoding apparatus 30 are processed by an even number delay circuit 41 so that even-numbered symbols are delayed by one frame. The parities Q and P are then inverted in sign. Error correction is then performed by a first error correcting circuit 42 with the second error correction code C1 on the basis of the parity P. The playback data, thus error-corrected by the first error correcting circuit 42, are interleaved by a first delay circuit 43, which applies the same amount of delay to the data as that afforded by the first delay circuit 32 in the encoding apparatus 30, before being supplied to a second error correcting circuit 44. The second error correction circuit 44 performs error correction with the first error correction code C2 on the basis of the parity Q. The playback data, thus corrected for errors by the first error correcting code C2 and the second error correction code C1, are processed by a second delay circuit 45 applying the same amount of delay to the playback data as that applied by the second delay circuit 34 in the encoding apparatus 30, whereby the interleaving applied by the first delay circuit 43 is released. The deinterleaved data are processed by an odd number delay circuit 46 which delays only odd-numbered data by one frame, so that the data are outputted with the same amount of delay for the respective data.

It is to be noted that an encoding apparatus 50 having the same function as that of the encoding apparatus 30 shown in Figure 1 may also be constructed by combining a part of the function of an encoder and a decoder presented as an integrated circuit for CIRC processing. Thus, the encoding apparatus 50 may be constructed as shown in Figure 3 by connecting a decoding apparatus 120 as shown in Figure 10 to the input side of an encoding apparatus 110 as shown in Figure 9. In this case, the decoding apparatus 120 is used for skipping the first and second error correcting circuits 122, 124 in Figure 10: that is, the circuits 122, 124 are effectively omitted in this case. The operating performed by the scrambling circuit 111 enclosed within the encoding apparatus 110 is cancelled by the descrambling circuit 125 connected to its input.

As shown by bracketed reference numerals in Figure 3, the deinterleaving circuit 123 of the decoding apparatus 120 shown in Figure 10 is used as a first delay circuit 52 of the encoding apparatus 50 embodying the invention. Also, the interleaving circuit 113 of the encoding apparatus 110 shown in Figure 9 is used as a second delay circuit 54 of the encoding apparatus 50, and the first and second correcting code generators 112, 115 of the encoding apparatus 110 shown in Figure 9 are used as first and second check word generating circuits 53, 55 in the encoding apparatus 50.

It is also to be noted that a decoding apparatus 60 having the same function as that of the decoding apparatus 40 shown in Figure 2 may also be constructed by combining a part of the function of an encoder and a decoder presented as an integrated circuit for CIRC processing. Thus, the encoding apparatus 60 may be constructed as shown in Figure 4 by connecting the decoding apparatus 120 shown in Figure 10 to an input side of the encoding apparatus 110 shown in Figure 9. In this case, the operation performed by the descrambling circuit 125 enclosed in the decoding apparatus 120 shown in Figure 10 is counteracted by the scrambling circuit 111 connected to its output.

As shown by bracketed reference numerals in Figure 4, the first and second error correcting circuits 122, 124 of the decoding apparatus 120 are used as first and second error correcting circuits 62, 64 in the decoding apparatus 60 embodying the invention. Also, the deinterleaving circuit 123 of the decoding circuit 120 is used as a first delay circuit 63 of the decoding apparatus 60, while the interleaving circuit 113 of the encoding apparatus 110 is used as a second delay circuit 65 of the decoding apparatus 60.

The above-mentioned disc recording and/or reproducing apparatus, which uses an encoding apparatus and a decoding apparatus embodying the invention, will now be described.

Referring to Figure 5, the disc recording and/or reproducing apparatus is provided with a magneto-optical disc 2, rotationally driven by a spindle motor 1, acting as a recording medium, and effects data recording by thermomagnetic recording. An optical head 3 irradiates an object track on the disc 2 with laser light and also detects laser light reflected from the object track to detect focusing errors by a so-called astigmatic method, while detecting tracking error by a so-called pushpull method. For reproducing data from the magneto-optical disc 2, the optical head 3 detects the difference in the polarisation angle (Kerr rotation angle) of the light reflected from the target track to generate a reproduced (playback) signal.

The output of the optical head 3 is supplied to a radio frequency (RF) circuit 5. The RF circuit 5 extracts the focusing error signal and the tracking error signal from the output of the optical head 3 and transmits the extracted signals to a servo control circuit 6, while converting the playback signal into correspond-

ing binary signals which it applies to a decoder 21 of the reproducing system, which will be explained subsequently.

The servo control circuit 6 is constituted by a focusing servo circuit, a tracking servo circuit, a spindle motor servo control circuit and a thread servo control circuit, none of which is shown. The focusing servo control circuit executes focusing control of an optical system of the optical head 3 so that the focusing error signal is reduced to zero. The tracking servo control circuit executes tracking control of the optical system of the optical head 3 so that the tracking error signal is reduced to zero. The spindle motor servo control circuit controls the spindle motor 1 for rotationally driving the disc 2 at a predetermined rotational velocity, such as at a constant linear velocity. The thread servo control circuit causes the optical head 3 and a magnetic head 4 to be moved to a target track position on the disc 2 as designed by a system controller (central processing unit or "CPU") 7. The servo control circuit 6, which executes these various control operations, transmits information indicating operating states of components controlled by the servo control circuit 6 to the system controller 7.

A key input operating section 8 and a display section 9 are connected to the system controller 7. The system controller 7 controls the recording system and the reproducing system to adopt an operating mode designated by operating input information from the key input operating section 8. The system controller 7 supervises, on the basis of sector-by-sector address information reproduced from the recording track of the magneto-optical disc 2 by header time or sub-Q data, the recording position as well as the reproducing position on the recording track traced by the optical head 3 and the magnetic head 4.

The recording system of the disc recording and/or reproducing apparatus is provided with an analogue to digital (A/D) converter 12 supplied with an analog audio signal AIN from an input terminal 10 by way of a low-pass filter 11.

The A/D converter 12 quantises the audio signal AIN to generate digital audio data at a predetermined transfer rate corresponding to the CD-I system. The digital audio data from the A/D converter 12 are supplied to an adaptive differential pulse code modulation (ADPCM) encoder 13.

The ADPCM encoder 13 processes the predetermined transfer rate digital audio data quantised from the audio signal AIN by the A/D converter 12 by subjecting it to a data compressing operation in conformity with the various modes in the CD-I system, and has its operating mode designated by the system controller 7. With the present disc recording and/or reproducing apparatus, the digital audio data of the CD-DA mode shown for example in Figure 6 are compressed by 1/4 by the ADPCM encoder 13 into B level stereo mode ADPCM audio data having a transfer rate of 18.75 (75/4) sectors/second. The B level stereo mode ADPCM audio data, continuously outputted from the ADPCM encoder 13 at the transfer rate of 18.75 sectors/second, are supplied to a memory, for example a random access armory (RAM) 14.

The memory 14 is controlled as regards data writing and readout by the system controller 7. The B level stereo mode ADPCM audio data, supplied from the ADPCM encoder 13, are written continuously into the memory 14 at the transfer rate of 18.75 sectors/second. Also, the B level stereo mode ADPCM audio data, continuously written into the memory 14 at the transfer rate of 18.75 sectors/second, are read out in a burst manner as recording data from the memory 14 at the transfer rate of 75 sectors/second.

Referring to Figure 7, the memory 14 is controlled by the system controller 7 so that a write pointer W of the memory 14 is continuously incremented at the transfer rate of 18.75 sectors/second to write the ADPCM audio data in the memory 14 at the transfer rate of 18.75 sectors/second and, if the data volume stored in the memory 14 exceeds a predetermined volume K, a read pointer R of the memory 14 is incremented in a burst manner at the transfer rate of 75 sectors/second to read out the predetermined volume K of the ADPCM data from the memory 14 as recording data in a burst manner at the transfer rate of 75 sectors/second.

The ADPCM audio data read out in burst manner from the memory 14 at the transfer rate of 75 sectors/second, that is the recording data, are supplied to an encoder 15.

The recording data supplied in a burst fashion from the memory 14 is processed by the encoder 15 with an error correcting coding operating, such as by parity addition or interleaving or eight to fourteen modulation (EFM). The recording data, thus encoded by the encoder 15, is supplied to a magnetic head driving circuit 16.

The magnetic head 4 is connected to the magnetic head driving circuit 16 for applying a modulation magnetic field conforming to the recording data to the magneto-optical disc 2.

The system controller 7 executes a recording position controlling operation for the memory 14 and, based on the controlling operation, executes disc recording position control so that the recording data read out in a burst fashion from the memory 14 will be recorded continuously on the recording track of the magneto-optical disc 2, as shown in Figure 6. For recording position control, the recording position of the recording data read out in a burst fashion from the memory 14 is supervised by the system controller 7 and control signals designating the recording position on the recording track of the magneto-optical disc 2 are supplied to the servo control circuit 6.

With the present recording system of the disc recording and/or reproducing apparatus, by controlling

the memory 14 by the system controller 7 in the above-described manner, the ADPCM audio data continuously outputted from the ADPCM encoder 13 at the transfer rate of 18.75 sectors/second are continuously written into the memory 14 at the transfer rate of 18.75 sectors/second and, when the data volume stored in the memory 14 exceeds the predetermined volume K, the predetermined volume K of ADPCM audio data is read out in a burst fashion from the memory 14 as recording data at the transfer rate of 75 sectors/second, so that the input data may be continuously written into the memory 14, while a vacant space for more than a predetermined volume is maintained at all times in the memory 14. On the other hand, the recording data read out in a burst fashion from the memory 14 may be continuously recorded on the recording tracks of the magneto-optical disc 2 by controlling the recording position on the recording tracks of the magneto-optical disc 2 by the system controller 7. Moreover, since a vacant space in excess of the predetermined data volume is perpetually maintained in the memory 14, input data may be continuously written in the vacant space of more than the predetermined data volume, even if the system controller 7 detects the occurrence of a track jump or the like due to a disturbance or the like to interrupt the recording operation on the magneto-optical disc 2, and the resetting operation may be executed in the interim, so that the input data may be continuously written on the recording track of the magneto-optical disc 2.

Header time data corresponding to the physical address of the sector is recorded on the disc 2 by being appended sector by sector to the ADPCM audio data. Table-of-contents data indicating the recording region and the recording mode are recorded in a table-of-contents region.

The reproducing system of the disc recording and/or reproducing apparatus will now be described.

The reproducing system is designed for reproducing data continuously recorded by the above-described recording system on the recording track of the magneto-optical disc 2, and is provided with the decoder 21 to which is supplied a playback output which has been generated by the optical head 3 tracing the recording track on the magneto-optical disc 2 with laser light, and which has been converted into binary format by the RF circuit 5.

The decoder 21 is a counterpart of the encoder 15 in the above-described recording system, and processes the playback output, converted into the binary format by the RF circuit 5, with the above-mentioned decoding operation or with the EFM decoding operation, while reproducing the above-mentioned B level stereo mode ADPCM audio data at a transfer rate of 75 sectors/second which is faster than the normal transfer rate for the above-mentioned B level stereo mode. The reproduced data, generated by the decoder 21, is supplied to a memory, which may be a random access memory (RAM) 22.

The memory 22 has its data writing and readout controlled by the system controller 7 so that the playback data supplied from the decoder 21 at the transfer rate of 75 sectors/second is written in a burst fashion at the transfer rate of 75 sectors/second. Also, the playback data written in a burst fashion at the transfer rate of 75 sectors/second in the memory 22 are continuously read out at the usual B level stereo mode transfer rate of 18.75 sectors/second.

The system controller 7 executes, besides the above-mentioned memory control operation for the memory 22, a reproducing position control from the recording track of the magneto-optical disc 2, in such a manner that the playback data written in a burst fashion by the above-mentioned memory control in the memory 22 is continuously reproduced from the recording track of the disc 2. The reproducing position control is executed by supervising a reproducing position on the disc 2 of the above-mentioned playback data written in a burst fashion in the memory 22 by the system controller 7 and by supplying a control signal designating the reproducing position on the recording track of the disc 2 to the servo control circuit 6, as shown in Figure 6.

The B-level stereo mode ADPCM audio data, obtained as playback data read out continuously from the memory 22 at a transfer rate of 18.75 sectors/second, are supplied to an ADPCM decoder 23.

The ADPCM decoder 23 is a counterpart of the ADPCM encoder 13 of the recording system, and has its operating mode designated by the system controller 7. With the present disc recording and/or reproducing apparatus, the B level stereo mode ADPCM audio data are expanded by a factor of four for reproducing the digital audio data. The reproduced digital audio data is transmitted by the ADPCM decoder 23 to a digital-to-analogue (D/A) converter 24.

The digital audio data from the ADPCM decoder 23 are converted by the D/A converter 24 into an analogue audio signal AOUT. The analogue audio signal AOUT, generated by the D/A converter 24, is outputted via a low-pass filter 25 at an output terminal 26.

The reproducing system of the disc recording and/or reproducing apparatus embodying the invention is provided with a digital output function in that the digital audio data at the output of the ADPCM decoder 23 is outputted at a data output terminal 28 via a digital output encoder 27 as a digital audio signal DOUT.

With the above-described reproducing system of the disc recording and/or reproducing apparatus, the system controller 7 controls the memory 22 in such a manner that the B-level stereo mode ADPCM audio data reproduced from the recording track of the magneto-optical disc 2 is written in a burst manner in the memory 22 at a transfer rate of 75 sectors/second,

and read out continuously from the memory 22 as playback data at the transfer rate of 18.75 sectors/second, so that the playback data may be continuously read out from the memory 22 while the data-depleted region in excess of a predetermined volume L (Figure 8) is perpetually maintained within the memory 22. Also, the playback data intermittently read out from the magneto-optical disc 2 may be continuously reproduced from the recording track on the magneto-optical disc 2 by controlling the reproducing position on the recording track of the disc by the system controller 7. In addition, the data read-out region in excess of the predetermined volume L is perpetually maintained in the memory 22, as described previously, so that, even when the system controller 7 detects an occurrence of a track jump etc. due to, for example, disturbances, and the operation of reproducing the magneto-optical disc 2 is discontinued, the playback data may be read out from the data read-out region having a space in excess of the predetermined data volume to continue outputting analogue audio signals and resetting may be performed in the interim.

As described above, the optical disc recording and/or reproducing apparatus records and reproduces B-level stereo mode ADPCM audio data. However, recording and reproduction may similarly be made of ADPCM audio data of other modes of the other CD-I systems. As far as the PCM audio data of the CD-DA mode is concerned, time compression may be effected in the memory 14 in the recording system, while recording data may be recorded during the time when the magneto-optical disc 2 is rotationally driven at a velocity conforming to the compression ratio of time compression. Also, time compression may be effected in the memory 22 in the reproducing system 22.

A data compression system other than the ADPCM system may be employed without any inconvenience.

With the above-described encoding apparatus embodying the invention, first check words are generated by the first error correction code in the first check word generating means from data which have been given difference amounts of delay by first delay means, while second check words are generated by the second error check code in the second check word generating means from data from the second delay means with the same amount of delay, so that the apparatus has correcting capabilities equivalent to those of the customary CIRC. Since the first delay means or circuit applies different amounts of delay to respective bit data constituting a data block, while the second delay circuit applies different amounts of delay to the respective bit data from the first delay means, the sum-total of the delay amounts applied to the respective bit data by the first and second delay means are the same. Thus, the encoded data are not interleaved, so that the risk of error distribution on occurrence of burst errors exceeding the correction capabilities in the transmission system may be eliminated.

With the decoding apparatus embodying the invention, the respective bit data constituting a data block encoded by the encoding apparatus are processed by the first error correcting means by error correction by the second error correction code using the second check word, while the respective bit data from the first delay means applying the same amount of delay as that applied by the first delay means of the encoding apparatus to the respective bit data thus corrected for error by the first error correcting means are processed by error correction by the first error correcting code by the second error correction means so that the apparatus has correction capabilities equivalent to those of the customary CIRC. The respective bit data, corrected for errors by the first and second error correcting means, are given the same amount of delay by the second delay means as that given by the second delay means of the encoding apparatus, before being outputted, so that, even if burst errors exceeding the correction capabilities should occur in the transmission system, the errors are not distributed, so that data defects may be minimised.

Claims

1. An error correction encoding apparatus (30; 50) for processing an input data word series with encoding for error correction, the apparatus comprising:

first delay means (32; 52) for applying different amounts of delay to respective data words constituting a data block for converting the input data word series in a first array state into an input data word series in a second array state;

first error correction encoding means (33; 53) for generating a first check words series from the data word series in said second array state;

second delay means (34; 54) for applying different amounts of delay to the data word series in said second array state and to the first check word series for converting said data word series and said check word series into a data word series and a check word series in a third array state; and

second error correction encoding means (35; 55) for generating a second check word series from said data word series and said check word series in the third array state;

characterised in that the amounts of delay applied by said first and second delay means (32, 34; 52, 54) are set so that the array state of said data word series in said third array state is the same as the array state of said data word series in said first array state.

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and read out continuously from the memory 22 as playback data at the transfer rate of 18.75 sectors/second, so that the playback data may be continuously read out from the memory 22 while the data-depleted region in excess of a predetermined volume L (Figure 8) is perpetually maintained within the memory 22. Also, the playback data intermittently read out from the magneto-optical disc 2 may be continuously reproduced from the recording track on the magneto-optical disc 2 by controlling the reproducing position on the recording track of the disc by the system controller 7. In addition, the data read-out region in excess of the predetermined volume L is perpetually maintained in the memory 22, as described previously, so that, even when the system controller 7 detects an occurrence of a track jump etc. due to, for example, disturbances, and the operation of reproducing the magneto-optical disc 2 is discontinued, the playback data may be read out from the data read-out region having a space in excess of the predetermined data volume to continue outputting analogue audio signals and resetting may be performed in the interim.

As described above, the optical disc recording and/or reproducing apparatus records and reproduces B-level stereo mode ADPCM audio data. However, recording and reproduction may similarly be made of ADPCM audio data of other modes of the other CD-I systems. As far as the PCM audio data of the CD-DA mode is concerned, time compression may be effected in the memory 14 in the recording system, while recording data may be recorded during the time when the magneto-optical disc 2 is rotationally driven at a velocity conforming to the compression ratio of time compression. Also, time compression may be effected in the memory 22 in the reproducing system 22.

A data compression system other than the ADPCM system may be employed without any inconvenience.

With the above-described encoding apparatus embodying the invention, first check words are generated by the first error correction code in the first check word generating means from data which have been given difference amounts of delay by first delay means, while second check words are generated by the second error check code in the second check word generating means from data from the second delay means with the same amount of delay, so that the apparatus has correcting capabilities equivalent to those of the customary CIRC. Since the first delay means or circuit applies different amounts of delay to respective bit data constituting a data block, while the second delay circuit applies different amounts of delay to the respective bit data from the first delay means, the sum-total of the delay amounts applied to the respective bit data by the first and second delay means are the same. Thus, the encoded data are not interleaved, so that the risk of error distribution on occurrence of burst errors exceeding the correction capabilities in the transmission system may be eliminated.

With the decoding apparatus embodying the invention, the respective bit data constituting a data block encoded by the encoding apparatus are processed by the first error correcting means by error correction by the second error correction code using the second check word, while the respective bit data from the first delay means applying the same amount of delay as that applied by the first delay means of the encoding apparatus to the respective bit data thus corrected for error by the first error correcting means are processed by error correction by the first error correcting code by the second error correction means so that the apparatus has correction capabilities equivalent to those of the customary CIRC. The respective bit data, corrected for errors by the first and second error correcting means, are given the same amount of delay by the second delay means as that given by the second delay means of the encoding apparatus, before being outputted, so that, even if burst errors exceeding the correction capabilities should occur in the transmission system, the errors are not distributed, so that data defects may be minimised.

Claims

1. An error correction encoding apparatus (30; 50) for processing an input data word series with encoding for error correction, the apparatus comprising:

   first delay means (32; 52) for applying different amounts of delay to respective data words constituting a data block for converting the input data word series in a first array state into an input data word series in a second array state;

   first error correction encoding means (33; 53) for generating a first check words series from the data word series in said second array state;

   second delay means (34; 54) for applying different amounts of delay to the data word series in said second array state and to the first check word series for converting said data word series and said check word series into a data word series and a check word series in a third array state; and

   second error correction encoding means (35; 55) for generating a second check word series from said data word series and said check word series in the third array state;

   characterised in that the amounts of delay applied by said first and second delay means (32, 34; 52, 54) are set so that the array state of said data word series in said third array state is the same as the array state of said data word series in said first array state.

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2. Apparatus according to claim 1, comprising third delay means (31; 51) for applying the same amount of delay to one of even-numbered data words and odd-numbered data words of said data word series in said first array state, and fourth delay means (36; 56) for applying the same amount of delay as that applied by said third delay means (31; 51) to the other of said even-numbered data words and said odd-numbered data words of said data word series and the check word series in said third array state.

3. Apparatus according to claim 2, comprising sign-inverting means for inverting the signs of said first and second check word series in said third array state.

4. Apparatus according to claim 1, claim 2 or claim 3, wherein said first and second check word series are parity codes of Reed-Solomon codes.

5. Apparatus according to any one of claims 1 to 4, which is capable of processing a said input data word series in a data compressed state.

6. An error correction decoding apparatus for executing an error correction decoding operation on an input data word series on which error correction encoding has been executed such that different amounts of delay (32; 52) are applied to data words constituting a data block of a data word series in a first array state for converting said data word series into a data word series in a second array state, first check word series are generated (33; 53) from the data word series in said second array state, different amounts of delay (34; 54) are applied to said data word series and said first check word series in said second array state for converting said data word series and said check word series into a data word series and a check word series in a third array state, and second check word series are generated (35; 55) from the data word series and the check word series in the third array state, the amounts of delay being such that the data word series in said third array state is equal to the array state of said data word series in said first array state, said apparatus comprising:

first error correction decoding means (42; 62) for processing the data word series constituting a data block of the input data word series in said third array state and the first check word series by error correction by an error correction code (C1) using said second check word series;

first delay means (43; 63) for applying different amounts of delay to said data word series and the check word series corrected for errors by said first error correction decoding means (42; 62) for converting said data word series and the first check word series into the data word series and the first check word series in said second array state;

second error correcting decoding means (44; 64) for error-correcting said data word series in said second array state by an error correction code (C2) using said first check word series; and

second delay means (45; 65) for applying different amounts of delay to said data word series corrected for errors by said second error correcting decoding means (44; 64) for converting said data word series into a data word series in said first array state, the amounts of delay applied by said first and second delay means being set so that the array state of said data word series in said first array state is the same as the array state of said data word series in said third array state.

7. Apparatus according to claim 6, comprising third delay means (41; 61) for applying the same amount of delay to one of even-numbered data words and check words and odd-numbered data words and check words of said data word series in said third array state, and fourth delay means (45; 65) for applying the same amount of delay as that applied by said third delay means (41; 61) to the other of said even-numbered data words and said odd-numbered data words of said data word series in said third array state.

8. Apparatus according to claim 7, comprising sign-inverting means for inverting the signs of said first and second check word series in said third array state.

9. Apparatus according to claim 6, claim 7 or claim 8, wherein said first and second check word series are parity codes of Reed-Solomon codes.

10. Apparatus according to any one of claims 6 to 9, which is capable of executing error correction decoding on a said input data word series in a data compressed state.

11. Apparatus according to any one of claims 6 to 10, which is capable of executing error correction decoding on a said input data word series reproduced from a recording medium.

Patentansprüche

1. Codierungs-Gerät (30; 50) zur Fehlerkorrektur zum Verarbeiten einer Eingangsdatenwörterreihe mit einer Codierfunktion für eine eine Fehlerkorektur, welches Gerät umfaßt:

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ein erstes Verzögerungsmittel (32; 52) zum Anwenden verschiedener Verzögerungsbeträge auf betreffende Datenwörter, die einen Datenblock bilden, zum Umsetzen der Eingangsdatenwörterreihe in einem ersten Feldzustand in eine Eingangsdatenwörterreihe in einem zweiten Feldzustand,

ein erstes Korekturcodierungsmittel (33; 53) zum Erzeugen einer ersten Prüfwörterreihe aus der Datenwörterreihe in dem zweiten Feldzustand,

ein zweites Verzögerungsmittel (34; 54) zum Anwenden verschiedener Verzögerungsbeträge auf die Datenwörterreihe in dem zweiten Feldzustand und die erste Prüfwörterreihe zum Umsetzen der Datenwörterreihe und der Prüfwörterreihe in eine Datenwörterreihe und eine Prüfwörterreihe in einem dritten Feldzustand und

ein zweites Korrekturcodierungsmittel (35; 55) zum Erzeugen einer zweiten Prüfwörterreihe aus der Datenwörterreihe und der Prüfwörterreihe in dem dritten Feldzustand,

dadurch **gekennzeichnet**, daß die Verzögerungsbeträge, die durch die ersten und zweiten Verzögerungsmittel (32, 34; 52, 54) angewendet werden, so eingestellt sind, daß der Feldzustand der Datenwörterreihe in dem dritten Feldzustand der gleiche wie derjenige der Datenwörterreihe in dem ersten Feldzustand ist.

2. Gerät nach Anspruch 1, das ein drittes Verzögerungsmittel (31, 51) zum Anwenden des gleichen Verzögerungsbetrags auf eines von geradzahligen und ungeradzahligen Datenwörtern der Datenwörterreihe in dem ersten Feldzustand und ein viertes Verzögerungsmittel (36; 56) zum Anwenden des gleichen Verzögerungsbetrags wie desjenigen, der durch das dritte Verzögerungsmittel (31; 51) angewendet wird, auf das andere der geradzahligen Datenwörter und der ungeradzahligen Datenwörter der Datenwörterreihe und der Prüfwörterreihe in dem dritten Feldzustand umfaßt.

3. Gerät nach Anspruch 2, das ein Vorzeichenumkehrmittel zum Umkehren der Vorzeichen der ersten und zweiten Prüfwörterreihen in dem dritten Feldzustand umfaßt.

4. Gerät nach Anspruch 1, 2 oder 3, wobei die ersten und zweiten Prüfwörterreihen Paritätscodes bestehend aus Reed-Solomon-Codes sind.

5. Gerät nach einem der Ansprüche 1 bis 4, das in der Lage ist, eine Eingangsdatenwörterreihe in einem Datenkompressionszustand zu verarbeiten.

6. Decodierungs-Gerät zur Fehlerkorrektur zum Ausführen einer Fehlerkorrektur-Decodierungsoperation an einer Datenwörterreihe, an welcher eine Fehlerkorrektur-Codierung derart ausgeführt wurde, daß verschiedene Verzögerungsbeträge (32; 52) auf Datenwörter angewendet wurden, die einen Datenblock einer Datenwörterreihe in einem ersten Feldzustand bilden, zum Umsetzen der Datenwörtreihe in eine Datenwörterreihe in einem zweiten Feldzustand, wobei erste Prüfwörterreihen (33; 53) aus der Datenwörterreihe in dem zweiten Feldzustand erzeugt werden, verschiedene Verzögerungsbeträge (34; 54) auf die Datenwörterreihe und die erste Prüfwörterreihe in dem zweiten Feldzustand zum Umsetzen der Datenwörterreihe und der Prüfwörterreihe in eine Datenwörterreihe und eine Prüfwörterreihe in einem dritten Feldzustand angewendet werden und zweite Prüfwörterreihen aus der Datenwörterreihe und der Prüfwörterreihe in dem dritten Feldzustand erzeugt werden (35; 55), wobei Verzögerungsbeträge derart eingestellt sind, daß die Datenwörterreihe in dem dritten Feldzustand gleich dem Feldzustand der Datenwörterreihe in dem ersten Feldzustand ist, welches Gerät umfaßt:

ein erstes Fehlerkorrektur-Decodierungsmittel (42; 62) zum Verarbeiten der Datenwörterreihe, die einen Datenblock der Eingangsdatenwörterreihe in dem dritten Feldzustand bildet, und der ersten Prüfwörterreihe durch Fehlerkorrektur mittels eines Fehlerkorrekturcodes (C1) unter Benutzung der zweiten Prüfwörterreihe,

ein erstes Verzögerungsmittel (43; 63) zum Anwenden verschiedener Verzögerungsbeträge auf die Datenwörterreihe und die Prüfwörterreihe, die durch das erste Fehlerkorrektur-Decodierungsmittel (42; 62)auf Fehler hin korrigiert sind, zum Umsetzen der Datenwörterreihe und der ersten Prüfwörterreihe in die Datenwörterreihe und die erste Prüfwörterreihe in dem zweiten Feldzustand,

ein zweites Fehlerkorrektur-Decodierungsmittel (44; 64) zur Fehlerkorrektur der Datenwörterreihe in dem zweiten Feldzustand mittels eines Fehlerkorrekturcodes (C2) unter Benutzung der ersten Prüfwörterreihe und

ein zweites Verzögerungsmittel (45; 65) zum Anwenden verschiedener Verzögerungsbeträge auf die Datenwörterreihe, welche auf Fehler hin durch das zweite Fehlerkorektur-Decodierungsmittel (44; 64) korrigiert ist, zum Umsetzen der Datenwörterreihe in eine Datenwörterreihe in dem ersten Feldzustand, wobei die Verzögerungsbeträge, die durch die ersten und zweiten Verzögerungsmittel angewendet werden, derart eingestellt sind, daß der Feldzustand der Datenwörterreihe in dem ersten Feldzustand der glei-

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che wie der Feldzustand der Datenwörterreihe in dem dritten Feldzustand ist.

7. Gerät nach Anspruch 6, das ein drittes Verzögerungsmittel (41; 61) zum Anwenden des gleichen Verzögerungsbetrags auf geradzahlige Datenwörter und Prüfwörter und ungeradzahlige Datenwörter und Prüfwörter der Datenwörterreihe in dem dritten Feldzustand und ein viertes Verzögerungsmittel (45; 65) zum Anwenden des gleichen Verzögerungsbetrags wie demjenigen, der durch das dritte Verzögerungsmittel (41; 61) auf die anderen der geradzahligen Datenwörter und die ungeradzahligen Datenwörter der Datenwörterreihe in dem dritten Feldzustand angewendet wird.

8. Gerät nach Anspruch 7, das ein Vorzeichenumkehrmittel zum Umkehren der Vorzeichen der ersten und zweiten Prüfwörterreihen in dem dritten Feldzustand umfaßt.

9. Gerät nach Anspruch 6, 7 oder 8, wobei die ersten und zweiten Prüfwörterreihen Paritätscodes bestehend aus Reed-Solomon-Codes sind.

10. Gerät nach einem der Ansprüche 6 bis 9, das in der Lage ist, eine Fehlerkorrektur-Decodierung an einer Eingangsdatenwörterreihe in einem Datenkompressionszustand auszuführen.

11. Gerät nach einem der Ansprüche 6 bis 10, das in der Lage ist, eine Fehlerkorrektur-Decodierung an einer Eingangsdatenwörterreihe auszuführen, die von einem Aufzeichnungsmedium wiedergegeben ist.

Revendications

1. Dispositif de codage pour la correction d'erreurs (30 ; 50) pour traiter une série de mots de données d'entrée par un codage pour la correction des erreurs, le dispositif comprenant :

un premier moyen à retard (32 ; 52) pour appliquer différents retards à des mots de données respectifs constituant un bloc de données pour la conversion de la série de mots de données d'entrée à un premier état d'ensemble en une série de mots de données d'entrée à un deuxième état d'ensemble ;

un premier moyen de codage pour la correction d'erreurs (33 ; 53) pour générer une première série de mots de contrôle à partir de la série de mots de données audit deuxième état d'ensemble ;

un deuxième moyen à retard (34 ; 54) pour appliquer différents retards à la série de mots de données audit deuxième état d'ensemble et à la première série de mots de contrôle pour la conversion de ladite série de mots de données et de ladite série de mots de contrôle en une série de mots de données et une série de mots de contrôle à un troisième état d'ensemble ; et,

un second moyen de codage pour la correction d'erreurs (35 ; 55) pour générer une seconde série de mots de contrôle à partir de ladite série de mots de données et de ladite série de mots de contrôle audit troisième état d'ensemble ;

caractérisé en ce que les retards appliqués par lesdits premier et deuxième moyens à retard (32, 34 ; 52, 54) sont établis de telle sorte que l'état d'ensemble de ladite série de mots de données audit troisième état d'ensemble est le même que l'état d'ensemble de ladite série de mots de données audit premier état d'ensemble.

2. Dispositif selon la revendication 1, comprenant un troisième moyen à retard (31 ; 51) pour appliquer le même retard aux uns des mots de données de numéros pairs et des mots de données de numéros impairs de ladite série de mots de données audit premier état d'ensemble, et un quatrième moyen à retard (36 ; 56) pour appliquer le même retard que celui appliqué par ledit troisième moyen à retard (31 ; 51) aux autres desdits mots de données de numéros pairs et desdits mots de données de numéros impairs de ladite série de mots de données et à la série de mots de contrôle audit troisième état d'ensemble.

3. Dispositif selon la revendication 2, comprenant un moyen d'inversion de signes pour inverser les signes desdites première et seconde séries de mots de contrôle audit troisième état d'ensemble.

4. Dispositif selon la revendication 1, la revendication 2 ou la revendication 3, dans lequel lesdites première et seconde séries de mots de contrôle sont des codes de parité de codes de Reed-Solomon.

5. Dispositif selon l'une quelconque des revendications 1 à 4, qui a la capacité de traiter une dite série de mots de données d'entrée à un état comprimé des données.

6. Dispositif de décodage pour la correction d'erreurs pour exécuter une opération de décodage pour la correction d'erreurs sur une série de mots de données d'entrée sur laquelle a été exécuté un codage pour la correction des erreurs tel que différents retards (32 ; 52) sont appliqués aux mots de données constituant un bloc de données d'une série de mots de données à un pre-

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mier état d'ensemble pour la conversion de ladite série de mots de données en une série de mots de données à un deuxième état d'ensemble, des premières séries de mots de contrôle sont générées (33 ; 53) à partir de la série de mots de données audit deuxième état d'ensemble, différents retards (34 ; 54) sont appliqués à ladite série de mots de données et auxdites premières séries de mots de contrôle audit deuxième état d'ensemble pour la conversion de ladite série de mots de données et desdites séries de mots de contrôle en une série de mots de données et une série de mots de contrôle à un troisième état d'ensemble, et des secondes séries de mots de contrôle sont générées (35 ; 55) à partir de la série de mots de données et de la série de mots de contrôle au troisième état d'ensemble, les retards étant tels que la série de mots de données audit troisième état d'ensemble est égale à l'état d'ensemble de ladite série de mots de données audit premier état d'ensemble, ledit dispositif comprenant ;

un premier moyen de décodage pour la correction d'erreurs (42 ; 62) pour traiter la série de mots de données constituant un bloc de données de la série de mots de données d'entrée audit troisième état d'ensemble et les premières séries de mots de contrôle par correction des erreurs par un code de correction d'erreurs (C1) en utilisant lesdites secondes séries de mots de contrôle ;

un premier moyen à retard (43 ; 63) pour appliquer différents retards à ladite série de mots de données et aux séries de mots de contrôle dont les erreurs ont été corrigées par ledit premier moyen de décodage pour la correction d'erreurs (42 ; 62) pour la conversion de ladite série de mots de données et des premières séries de mots de contrôle en la série de mots de données et les premières séries de mots de contrôle audit deuxième état d'ensemble ;

un second moyen de décodage pour la correction d'erreurs (44 ; 64) pour corriger les erreurs de ladite série de mots de données audit deuxième état d'ensemble par un code de correction d'erreurs (C2) en utilisant lesdites premières séries de mots de contrôle ; et,

un deuxième moyen à retard (45 ; 65) pour appliquer différents retards à ladite série de mots de données dont les erreurs ont été corrigées par ledit second moyen de décodage pour la correction d'erreurs (44 ; 64) pour la conversion de ladite série de mots de données en une série de mots de données audit premier état d'ensemble, les retards appliqués par lesdits premier et deuxième moyens à retard étant établis de telle sorte que l'état d'ensemble de ladite série de mots de données audit premier état d'ensemble est le même que l'état d'ensemble de ladite série de mots de données audit troisième état d'ensemble.

7. Dispositif selon la revendication 6, comprenant un troisième moyen à retard (41 ; 61) pour appliquer le même retard aux uns des mots de données de numéros pairs et des mots de données de numéros impairs et à des mots de contrôle de ladite série de mots de données audit troisième état d'ensemble, et un quatrième moyen à retard (45 ; 65) pour appliquer le même retard que celui appliqué par ledit troisième moyen à retard (41 ; 61) aux autres desdits mots de données de numéro pairs et desdits mots de données de numéros impairs de ladite série de mots de données audit troisième état d'ensemble.

8. Dispositif selon la revendication 7, comprenant un moyen d'inversion de signes pour inverser les signes desdites premières et secondes séries de mots de contrôle audit troisième état d'ensemble.

9. Dispositif selon la revendication 6, la revendication 7 ou la revendication 8, dans lequel lesdites premières et secondes séries de mots de contrôle sont des codes de parité de codes de Reed-Solomon.

10. Dispositif selon l'une quelconque des revendications 6 à 9, qui a la capacité d'exécuter un décodage pour la correction d'erreurs sur une dite série de mots de données d'entrée à un état comprimé des données.

11. Dispositif selon l'une quelconque des revendications 6 à 10, qui a la capacité d'exécuter un décodage pour la correction d'erreurs sur une dite série de mots de données d'entrée reproduite à partir d'un support d'enregistrement.