DESCRIPTION

SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device and a method for manufacturing the semiconductor device.

[0002]

In this specification, a semiconductor device generally means a device which can function by utilizing semiconductor characteristics, and an electrooptic device, a semiconductor circuit, and electronic equipment are all semiconductor devices.

BACKGROUND ART

[0003]

A technique by which a transistor is formed using a semiconductor thin film formed over a substrate having an insulating surface has attracted attention. The transistor is applied to a wide range of electronic devices such as an integrated circuit (IC) or an image display device (display device). A silicon-based semiconductor material is widely known as a material for a semiconductor thin film applicable to a transistor. As another material, an oxide semiconductor has been attracting attention.

[0004]

For example, a transistor whose active layer includes an amorphous oxide including indium (In), gallium (Ga), and zinc (Zn) is disclosed (see Patent Document 1).

[0005]

Transistors including oxide semiconductors have on-state characteristics (e.g., on-state current) superior to those of transistors including amorphous silicon. In order to apply the transistors including oxide semiconductors to high-performance devices, such transistors are required to have further improved characteristics, and thus techniques of crystallization of oxide semiconductors have been developed (Patent Document 2). In Patent Document 2, a technique in which an oxide semiconductor is crystallized by heat treatment is disclosed.

[Reference]

[Patent Document]

[0006]

[Patent Document 1] Japanese Published Patent Application No. 2006-165528

[Patent Document 2] Japanese Published Patent Application No. 2008-311342

DISCLOSURE OF INVENTION

[0007]

An oxide semiconductor film used in a transistor is formed by a sputtering method in many cases. However, when the oxide semiconductor film is formed by sputtering, in some cases, an ionized rare gas element or a particle ejected from a surface of a target flicks off a particle of a film, such as a gate insulating film, on which the oxide semiconductor film is to be formed (the film is also referred to as "formed film"). Particles flicked off from the formed film enter the oxide semiconductor film and functions as an impurity element therein. In particular, the oxide semiconductor film in the vicinity of a surface of the formed film (the surface is also referred to as "formed film surface") may have high concentration of the impurity element. Further, when the impurity element is left in the oxide semiconductor film in the vicinity of the formed film surface, the impurity element causes adversely effect on characteristics of the transistor.

[0008]

Furthermore, the impurity element included in the oxide semiconductor film in the vicinity of the formed film surface inhibits crystallization of the oxide semiconductor film. As a result, an amorphous region is left in the oxide semiconductor film in the vicinity of the formed film surface.

[0009]

Thus, the following countermeasure can be considered: the oxide semiconductor film is made thick, and a crystal region formed in a surface layer is used. However, in order to reduce parasitic capacitance and to operate the transistor with lower power, the oxide semiconductor film is desirably formed thin. In that case, a channel formation region is formed in the oxide semiconductor film in the vicinity of the formed film surface, and crystallization of the oxide semiconductor film is desirably

progressed in the vicinity of the formed film surface accordingly.

[0010]

In view of the above problem, an object is to reduce the concentration of impurities included in an oxide semiconductor film in the vicinity of the formed film surface. Further, an object is to improve crystallinity of the oxide semiconductor film. Further, an object is to provide a semiconductor device having stable electric characteristics with use of the oxide semiconductor film.

[0011]

One embodiment of the disclosed invention is a semiconductor device including an insulating film which includes oxidized material containing silicon, an oxide semiconductor film provided to be in contact with the insulating film, a source electrode and a drain electrode electrically connected to the oxide semiconductor film, and a gate electrode adjacent to the oxide semicondur film. The oxide semiconductor film includes a first region in which a concentration of silicon distributed from an interface with the gate insulating film toward an inside of the oxide semiconductor film is lower than or equal to 1.0 at. %, and at least the first region includes a crystal portion. The gate electrode may be located below the oxide semiconductor film with the insulating film interposed therebetween.

[0012]

One embodiment of the disclosed invention is a semiconductor device including a gate electrode, a gate insulating film which includes oxidized material containing silicon and covers the gate electrode, an oxide semiconductor film provided to be in contact with the gate insulating film and overlap with at least the gate electrode, a channel protective film provided to be in contact with the oxide semiconductor film, and a source electrode and a drain electrode which are provided over the channel protective film and electrically connected to the oxide semiconductor film. The oxide semiconductor film includes a first region in which a concentration of silicon distributed from an interface with the gate insulating film toward an inside of the oxide semiconductor film is lower than or equal to 1.0 at. %, and at least the first region includes a crystal portion.

[0013]

In each of the above structures, the first region is preferably provided to be in

contact with the gate insulating film or the insulating film and have a thickness less than or equal to 5 nm, and the concentration of silicon included in a region other than the first region is preferably lower than the concentration of silicon included in the first region.

[0014]

In each of the above structures, the region in the oxide semiconductor film other than the first region preferably includes a crystal portion.

[0015]

Further, one embodiment of the disclosed invention is a semiconductor device including a gate electrode, a gate insulating film which includes oxidized material containing silicon and covers the gate electrode, an oxide semiconductor film provided to be in contact with the gate insulating film and overlap with at least the gate electrode, a source electrode and a drain electrode electrically connected to the oxide semiconductor film, and a protective insulating film which includes oxidized material containing silicon and covers the oxide semiconductor film and the source electrode and the drain electrode. The oxide semiconductor film includes a first region in which a concentration of silicon distributed from an interface with the gate insulating film toward an inside of the oxide semiconductor film is lower than or equal to 1.0 at.%. The oxide semiconductor film includes a second region in which a concentration of silicon distributed from an interface with the protective insulating film toward the inside of the oxide semiconductor film is lower than or equal to 1.0 at.%. At least the first region and the second region include a crystal portion.

[0016]

In each of the above structures, the first region is preferably provided to be in contact with the gate insulating film and have a thickness less than or equal to 5 nm, the second region is preferably provided to be in contact with the protective insulating film and have a thickness less than or equal to 5 nm, and the concentration of silicon included in a region other than the first region and the second region is preferably lower than the concentrations of silicon included in the first region and the second region.

[0017]

Further, in each of the above structures, a crystal portion is preferably included

in the region in the oxide semiconductor film other than the first region and the second region.

[0018]

Further, in each of the above structures, a c-axis of the crystal portion is preferably aligned in a direction perpendicular to the interface between the oxide semiconductor film and the gate insulating film or the insulating film.

[0019]

Further, in each of the above structures, the concentration of silicon included in the first region is preferably lower than or equal to 0.1 at.%.

[0020]

Further, in each of the above structures, the gate insulating film or the insulating film includes carbon, and the concentration of carbon in the first region is preferably lower than or equal to 1.0×10^{20} atoms/cm^3.

[0021]

According to one embodiment of the disclosed invention, the concentration of impurities included in the oxide semiconductor film in the vicinity of the formed film surface can be reduced. In addition, crystallinity of the oxide semiconductor film can be improved. Thus, with use of such an oxide semiconductor film, a semiconductor device having stable electric characteristics can be provided.

BRIEF DESCRIPTION OF DRAWINGS

[0022]

FIGS. 1A and 1B are a plan view and a cross-sectional view illustrating one embodiment of a semiconductor device.

FIGS. 2A and 2B are a plan view and a cross-sectional view illustrating one embodiment of a semiconductor device.

FIGS. 3A and 3B are a plan view and a cross-sectional view illustrating one embodiment of a semiconductor device.

FIGS. 4A to 4E are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 5A to 5E are cross-sectional views illustrating an example of a

manufacturing process of a semiconductor device.

FIG. 6 is a model diagram used for calculation.

FIGS. 7A to 7C show calculation results.

FIGS. 8A to 8C show calculation results.

FIGS. 9A to 9C illustrate one embodiment of a semiconductor device.

FIG. 10 illustrates one embodiment of a semiconductor device.

FIG. 11 illustrates one embodiment of a semiconductor device.

FIG. 12 illustrates one embodiment of a semiconductor device.

FIGS. 13A to 13F each illustrate an electronic device.

FIG. 14 is a graph showing measurement results according to one example of the present invention.

FIG. 15 illustrates a structure of a sample according to one example of the present invention.

FIG. 16 is a graph showing measurement results according to one example of the present invention.

FIG. 17 illustrates a structure of a sample according to one example of the present invention.

FIGS. 18A and 18B are graphs showing measurement results according to one example of the present invention.

FIGS. 19A and 19B each illustrate a structure of a sample according to one example of the present invention.

FIGS. 20A and 20B are graphs showing measurement results according to one example of the present invention.

FIGS. 21A and 21B are model diagrams used for calculation.

FIGS. 22A and 22B are model diagrams used for calculation.

FIG. 23 shows calculation results.

FIGS. 24A and 24B are model diagrams used for calculation.

FIG. 25 shows calculation results.

BEST MODE FOR CARRYING OUT THE INVENTION

[0023]

Hereinafter, embodiments of the invention disclosed in this specification will

be described in detail with reference to the accompanying drawings. Note that the present invention is not limited to the following description and it will be readily appreciated by those skilled in the art that modes and details can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the invention should not be construed as being limited to the description in the following embodiments.

[0024]

Note that the position, the size, the range, or the like of each structure illustrated in the drawings and the like are not accurately represented in some cases for easy understanding. Therefore, the disclosed invention is not necessarily limited to the position, size, range, or the like as disclosed in the drawings and the like.

[0025]

In this specification and the like, ordinal numbers such as "first", "second", and "third" are used in order to avoid confusion among components, and the terms do not mean limitation of the number of components.

[0026]

Note that in this specification and the like, the term such as "over" or "below" does not necessarily mean that a component is placed "directly on" or "directly under" another component. For example, the expression "a gate electrode over a gate insulating layer" can mean the case where there is an additional component between the gate insulating layer and the gate electrode.

[0027]

In addition, in this specification and the like, the term such as "electrode" or "wiring" does not limit a function of a component. For example, an "electrode" is sometimes used as part of a "wiring", and vice versa. Furthermore, the term "electrode" or "wiring" can include the case where a plurality of "electrodes" or "wirings" is formed in an integrated manner.

[0028]

Functions of a "source" and a "drain" are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flowing is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be replaced with each other in this specification and the like.

[0029]

Note that in this specification and the like, the term "electrically connected" includes the case where components are connected through an object having any electric function. There is no particular limitation on an object having any electric function as long as electric signals can be transmitted and received between components that are connected through the object. Examples of an "object having any electric function" are a switching element such as a transistor, a resistor, an inductor, a capacitor, and an element with a variety of functions as well as an electrode and a wiring.

[0030]

(Embodiment 1)

In this embodiment, one embodiment of a semiconductor device and a manufacturing method thereof will be described with reference to FIGS. 1A and 1B, FIGS. 2A and 2B, FIGS. 3A and 3B, FIGS. 4A to 4E, and FIGS. 5A to 5E.

[0031]

<Example of Structure of Semiconductor Device>

In FIGS. 1A and 1B, a plan view and a cross-sectional view of a channel-etched type transistor, which has a bottom-gate structure, are shown as an example of a semiconductor device. FIG. 1A is a plan view and FIG. 1B is a cross-sectional view taken along line A-B in FIG. 1A. In FIG. 1A, some of components (e.g., a protective insulating film 109 or the like) of a transistor 110 are omitted to avoid complexity.

[0032]

The transistor 110 illustrated in FIGS. 1A and 1B includes, over a substrate 100 haivng an insulating surface, a gate electrode 101, a gate insulating film 102 covering the gate electrode 101, an oxide semiconductor film 103 provided to be in contact with the gate insulating film 102 and overlap with at least the gate electrode 101, a source electrode 105a and a drain electrode 105b electrically connected to the oxide semiconductor film 103, and the protective insulating film 109 covering the oxide semiconductor film 103 and the source electrode 105a and the drain electrode 105b.

[0033]

The thickness of the oxide semiconductor film 103 is greater than 5 nm and less than or equal to 200 nm, preferably greater than or equal to 10 nm and less than or

equal to 30 nm. Further, the oxide semiconductor film 103 preferably has a structure with crystallinity (e.g., a single crystal structure, a microcrystalline structure, or the like).

[0034]

In this embodiment, the oxide semiconductor film 103 is preferably a c-axis aligned crystalline oxide semiconductor (CAAC-OS) film.

[0035]

The CAAC-OS film is not completely single crystal or completely amorphous. The CAAC-OS film is an oxide semiconductor film with a crystal-amorphous mixed phase structure where crystal portions are included in an amorphous phase. Note that in most cases, the crystal portion fits inside a cube whose one side is less than 100 nm. From an observation image obtained with a transmission electron microscope (TEM), a boundary between an amorphous region and a crystal region in the CAAC-OS film is not clear. Further, with the TEM, a grain boundary in the CAAC-OS film cannot be found. Thus, in the CAAC-OS film, a reduction in electron mobility, due to the grain boundary, is suppressed.

[0036]

In each of the crystal portions included in the CAAC-OS film, a c-axis is aligned in a direction perpendicular to a surface where the CAAC-OS film is formed or a surface of the CAAC-OS film, triangular or hexagonal atomic arrangement which is seen from the direction perpendicular to the a-b plane is formed, and metal atoms are arranged in a layered manner or metal atoms and oxygen atoms are arranged in a layered manner when seen from the direction perpendicular to the c-axis.. Note that, among crystal portions, the directions of an a-axis and a b-axis of one crystal portion may be different from those of another crystal portion. In this specification and the like, a simple term "perpendicular" includes a range from 85° to 95°.

[0037]

In the CAAC-OS film, distribution of crystal portions is not necessarily uniform. For example, in the formation process of the CAAC-OS film, in the case where crystal growth occurs from a surface side of the oxide semiconductor film, the proportion of crystal portions in the vicinity of the surface of the oxide semiconductor film is higher than that in the vicinity of the surface where the oxide semiconductor film

is formed in some cases.

[0038]

Since the c-axes of the crystal portions included in the CAAC-OS film are aligned in the direction perpendicular to a surface where the CAAC-OS film is formed or a surface of the CAAC-OS film, the directions of the c-axes may be different from each other depending on the shape of the CAAC-OS film (the cross-sectional shape of the surface where the CAAC-OS film is formed or the cross-sectional shape of the surface of the CAAC-OS film). Note that when the CAAC-OS film is formed, the direction of c-axis of the crystal portion is the direction perpendicular to the surface where the CAAC-OS film is formed or the surface of the CAAC-OS film. The crystal portion is formed by film formation or by performing treatment for crystallization such as heat treatment after film formation.

[0039]

With use of the CAAC-OS film in a transistor, change in electric characteristics of the transistor due to irradiation with visible light or ultraviolet light can be reduced. Change and variation in threshold voltages can be suppressed. Thus, the transistor has high reliability.

[0040]

In an oxide semiconductor having crystallinity (crystalline oxide semiconductor), defects in the bulk can be further reduced. Further, when planarity of the surface of the crystalline oxide semiconductor film is enhanced, a transistor including such an oxide semiconductor can obtain higher field-effect mobility than a transistor including an amorphous oxide semiconductor. In order to enhance the surface planarity of the oxide semiconductor film, the oxide semiconductor is preferably formed over a flat surface. Specifically, the oxide semiconductor is preferably formed over a surface with an average surface roughness (R_a) less than or equal to 0.15 nm, preferably less than or equal to 0.1 nm.

[0041]

Note that the average surface roughness (R_a) is obtained by expanding, into three dimensions, arithmetic mean surface roughness that is defined by JIS B 0601:2001 (ISO4287:1997) so as to be able to apply it to a curved surface. R_a can be expressed as

an "average value of the absolute values of deviations from a reference surface to a specific surface" and is defined by the following formula.

[0042]

[FORMULA 1]

$$Ra = \frac{1}{S_0}\int_{y_1}^{y_2}\int_{x_1}^{x_2}\left|f(x,y) - Z_0\right|dxdy$$

[0043]

Here, the specific surface is a surface that is a target of roughness measurement, and is a quadrilateral region specified by four points represented by the coordinates (x_1, y_1, $f(x_1, y_1)$), (x_1, y_2, $f(x_1, y_2)$), (x_2, y_1, $f(x_2, y_1)$), and (x_2, y_2, $f(x_2, y_2)$). Moreover, S_0 represents the area of a rectangle which is obtained by projecting the specific surface on the xy plane, and Z_0 represents the height of the reference surface (the average height of the specific surface). R_a can be measured using an atomic force microscope (AFM).

[0044]

As illustrated in FIG. 1B, an end portion of the oxide semiconductor film 103 is preferably tapered at an angle of 20° to 50°. When the oxide semiconductor film 103 has a perpendicular end portion, oxygen is more likely to be released from the oxide semiconductor film 103, and accordingly, oxygen vacancies are likely to be generated. When the oxide semiconductor film 103 has a tapered end portion, generation of oxygen vacancies is suppressed, and thus generation of leakage current of the transistor 110 can be reduced.

[0045]

An oxide semiconductor used for the oxide semiconductor film 103 preferably contains at least indium (In) or zinc (Zn). In particular, In and Zn are preferably contained. In addition, as a stabilizer for reducing variation in electric characteristics of a transistor using the oxide semiconductor, one or more selected from gallium (Ga), tin (Sn), hafnium (Hf), zirconium (Zr), titanium (Ti), scandium (Sc), yttrium (Y), and an lanthanoid element (such as cerium (Ce), neodymium (Nd), or gadolinium (Gd), for example) is preferably contained.

[0046]

As the oxide semiconductor, for example, any of the following can be used:

indium oxide; tin oxide; zinc oxide; a two-component metal oxide such as an In-Zn-based oxide, a Sn-Zn-based oxide, an Al-Zn-based oxide, a Zn-Mg-based oxide, a Sn-Mg-based oxide, an In-Mg-based oxide, or an In-Ga-based oxide; a three-component metal oxide such as an In-Ga-Zn-based oxide (also referred to as IGZO), an In-Al-Zn-based oxide, an In-Sn-Zn-based oxide, a Sn-Ga-Zn-based oxide, an Al-Ga-Zn-based oxide, a Sn-Al-Zn-based oxide, an In-Hf-Zn-based oxide, an In-Zr-Zn-based oxide, an In-Ti-Zn-based oxide, an In-Sc-Zn-based oxide, an In-Y-Zn-based oxide, an In-La-Zn-based oxide, an In-Ce-Zn-based oxide, an In-Pr-Zn-based oxide, an In-Nd-Zn-based oxide, an In-Sm-Zn-based oxide, an In-Eu-Zn-based oxide, an In-Gd-Zn-based oxide, an In-Tb-Zn-based oxide, an In-Dy-Zn-based oxide, an In-Ho-Zn-based oxide, an In-Er-Zn-based oxide, an In-Tm-Zn-based oxide, an In-Yb-Zn-based oxide, or an In-Lu-Zn-based oxide; and a four-component metal oxide such as an In-Sn-Ga-Zn-based oxide, an In-Hf-Ga-Zn-based oxide, an In-Al-Ga-Zn-based oxide, an In-Sn-Al-Zn-based oxide, an In-Sn-Hf-Zn-based oxide, or an In-Hf-Al-Zn-based oxide.

[0047]

Here, an "In-Ga-Zn-based oxide" means an oxide containing In, Ga, and Zn as its main components and there is no particular limitation on the ratio of In: Ga: Zn. The In-Ga-Zn-based oxide may contain a metal element other than In, Ga, and Zn.

[0048]

Alternatively, a material represented by $InMO_3(ZnO)_m$ ($m > 0$ is satisfied, and m is not an integer) may be used as an oxide semiconductor. Note that M represents one or more metal elements selected from Ga, Fe, Mn, and Co, or the above-described element as a stabilizer. Alternatively, as the oxide semiconductor, a material represented by a chemical formula, $In_2SnO_5(ZnO)_n$ ($n > 0$, n is a natural number) may be used.

[0049]

For example, an In-Ga-Zn-based oxide with an atomic ratio of In: Ga: Zn = 1:1:1, In: Ga: Zn = 3:1:2, or In: Ga: Zn = 2:1:3, or any of oxides whose composition is in the neighborhood of the above compositions can be used.

[0050]

For the gate insulating film 102, an oxide insulating film having a sufficient withstand voltage and sufficient insulating properties is preferably used. In the case where the gate insulating film 102 has a single-layer structure, an insulating film including oxidized material containing silicon, such as silicon oxide, may be used for example.

[0051]

Alternatively, the gate insulating film 102 may have a stacked structure. In the case where the gate insulating film 102 has a stacked structure, silicon oxide may be stacked over gallium oxide, aluminum oxide, silicon nitride, silicon oxynitride, aluminum oxynitride, yttrium oxide, lanthanum oxide, silicon nitride oxide, or the like. Alternatively, silicon oxide may be stacked over a high-k material such as hafnium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate to which nitrogen is added ($HfSiO_xN_y$ ($x > 0$, $y > 0$)), or hafnium aluminate ($HfAl_xO_y$ ($x > 0$, $y > 0$)). The use of such a high-k material enables a reduction in gate leakage current.

[0052]

In the case of using an oxide insulating film as the gate insulating film 102, part of contained oxygen can be released from the oxide insulating film when the oxide insulating film is heated; thus, oxygen can be supplied to the oxide semiconductor film 103, and oxygen vacancies in the oxide semiconductor film 103 can be filled. In particular, the gate insulating film 102 preferably contains a large amount of oxygen which exceeds at least the stoichiometry in (a bulk of) the film. For example, a film of silicon oxide represented by the formula $SiO_{2+\alpha}$ ($\alpha > 0$) is preferably used as the gate insulating film 102. When such a silicon oxide film is used as the gate insulating film 102, oxygen can be supplied to the oxide semiconductor film 103, so that the transistor 110 using the oxide semiconductor film 103 can have favorable transistor characteristics.

[0053]

However, in the case of using a silicon oxide film as the gate insulating film 102, silicon in the gate insulating film 102 might be taken as an impurity into the oxide semiconductor film 103. Silicon or the like enters the oxide semiconductor film 103 and serves as an impurity, which affects characteristics of the transistor. Further, when

an impurity element enters the oxide semiconductor film 103 in the vicinity of the surface on which the oxide semiconductor film 103 is formed (formed film surface), crystallization of an oxide semiconductor film is inhibited by the impurity element. Thus, an amorphous region is left in the oxide semiconductor film in the vicinity of the formed film surface. In addition, in the case where the oxide semiconductor film 103 is a CAAC-OS film, it is difficult to form a crystal portion in the vicinity of the formed film surface.

[0054]

In particular, impurities such as silicon are likely to enter the oxide semiconductor film 103 in the vicinity of the formed film surface where the oxide semiconductor film 103 and the gate insulating film 102 are in contact with each other. A channel formation region of the transistor 110 is formed in the oxide semiconductor film 103 in the vicinity of the formed film surface; thus, when impurities such as silicon enter the vicinity of the formed film surface, characteristics of the transistor 110 might be changed.

[0055]

Change in structure of the oxide semiconductor film 103 when SiO_2, oxidized material containing silicon, is added as an impurity was examined by classical molecular dynamics calculation. The results thereof are described with reference to FIGS. 21A and 21B, FIGS. 22A and 22B, FIG. 23, FIGS. 24A and 24B, and FIG. 25. Note that simulation software "SCIGRESS ME" manufactured by Fujitsu Limited was used for classical molecular dynamics calculation. An empirical potential which characterizes the interaction between atoms is defined in the classical molecular dynamics method, so that force that acts on each atom is evaluated. Newton's equation of motion is numerically solved, whereby motion (time-dependent change) of each atom can be deterministically tracked.

[0056]

Hereinafter, calculation models and calculation conditions are described. Note that in this calculation, the Born-Mayer-Huggins potential was used.

[0057]

A single crystal structure of $InGaZnO_4$ including 1680 atoms (see FIG. 21A) and a structure of $InGaZnO_4$ including 1680 atoms in which 20 atoms of each of In, Ga,

and Zn are substituted by silicon (Si) atoms (see FIG. 21B) were formed as calculation models. In the model of Si substitution shown in FIG. 21B, silicon atoms are included at 3.57 at.% (2.34 wt.%). Further, the density of the model of the single crystal shown in FIG. 21A is 6.36 g/cm^3, and the density of the model of Si substitution shown in FIG. 21B is 6.08 g/cm^3.

[0058]

At 1727 °C which is lower than the melting point of the $InGaZnO_4$ single crystal (about 2000 °C according to estimation by the classical molecular dynamics calculation), structure relaxation was performed on the calculation models shown in FIGS. 21A and 21B by the classical molecular dynamics calculation at a fixed pressure (1 atm) for 150 psec (time step width 0.2 fsec × 750000 steps). The radial distribution functions g(r) of the two structures were calculated. Note that the radial distribution function g(r) is a function representing the probability density of atoms existing at a distance of r from one atom. As the correlation between atoms disappears, g(r) becomes closer to 1.

[0059]

FIGS. 22A and 22B show final structures obtained by performing the classical molecular dynamics calculation for 150 psec on the above two calculation models. In addition, FIG. 23 shows the radial distribution function g (r) in each structure.

[0060]

The model of single crystal shown in FIG. 22A is stable and keeps the crystal structure even in the final structure, whereas the model of Si substitution shown in FIG. 22B is unstable, and it can be observed that the crystal structure is distorted with time and changes into an amorphous structure. When the radial distribution functions g(r) of the structural models are compared with each other in FIG. 23, it is found that the single crystal model has peaks even at a long distance and has a long-range order. On the other hand, it is found that in the model of Si substitution, the peak disappears at a distance about 0.6 nm, and the model of Si substitution does not have the long-range order.

[0061]

The above calculation results indicate that when silicon (Si) is included in

$InGaZnO_4$, $InGaZnO_4$ is likely to become amorphous. Further, according to the above results, even when $InGaZnO_4$ including silicon (Si) is heated at high temperature, such $InGaZnO_4$ is not crystallized.

[0062]

Next, change in structure of the oxide semiconductor film 103 when carbon atoms (C) are added was examined by classical molecular dynamics calculation. The results thereof are described with reference to FIG. 21A, FIGS. 24A and 24B, and FIG. 25. Note that simulation software "SCIGRESS ME" manufactured by Fujitsu Limited was used for classical molecular dynamics calculation.

[0063]

Calculation models and calculation results are as follows. Note that in this calculation, the Born-Mayer-Huggins potential was used. Further, for the interaction between carbon atoms (C), a Lennard-Jones potential was used.

[0064]

A single crystal structure of $InGaZnO_4$ including 1680 atoms (see FIG. 21A) and a structure of $InGaZnO_4$ including 1680 atoms in which 20 atoms of each of In, Ga, and Zn are substituted by carbon atoms (C) and 80 atoms of oxygen (O) are substituted by carbon atoms (C) (see FIG. 24A) were formed as calculation models. In the model of C substitution shown in FIG. 24A, carbon atoms (C) are included at 8.33 at.%. Further, the density of the model of the single crystal shown in FIG. 21A is 6.36 g/cm^3, and the density of the model of C substitution shown in FIG. 24A is 5.89 g/cm^3.

[0065]

At 1727 °C which is lower than the melting point of the $InGaZnO_4$ single crystal (about 2000 °C according to estimation by the classical molecular dynamics calculation), structure relaxation was performed on the calculation models shown in FIG. 21A and FIG. 24A by the classical molecular dynamics calculation at a fixed pressure (1 atm) for 140 psec (time step width 0.2 fsec × 750000 steps). The radial distribution functions g(r) of the two structures were calculated. Note that the radial distribution function g(r) is a function representing the probability density of atoms existing at a distance of r from one atom. As the correlation between atoms disappears, g(r) becomes closer to 1.

[0066]

FIG. 22A and FIG. 24B show final structures obtained by performing the classical molecular dynamics calculation for 150 psec on the above two calculation models. The radial distribution function g(r) in each structure is shown in FIG. 25.

[0067]

The model of single crystal shown in FIG. 22A is stable and keeps the crystal structure even in the final structure, whereas the model of C substitution shown in FIG. 24B is unstable, and it can be observed that the crystal structure is distorted with time and changes into an amorphous structure. As seen in FIG. 25, by comparing the radial distribution functions g(r) of the structural models with each other, it is found that the model of single crystal has peaks even at a long distance and the long-range order. On the other hand, it is found that in the model of C substitution, the peak disappears at a distance about 0.6 nm, and the model of C substitution does not have the long-range order.

[0068]

The above calculation results indicate that when carbon (C) is included in $InGaZnO_4$, $InGaZnO_4$ is likely to become amorphous. In addition, according to the above results, even when $InGaZnO_4$ including carbon (C) is heated at high temperature, such $InGaZnO_4$ is not crystallized.

[0069]

As described above, entry of impurities into the oxide semiconductor film causes a reduction in crystallinity of the oxide semiconductor film. Thus, in the semiconductor device shown in this embodiment, entry of impurities such as silicon into the oxide semiconductor film in the vicinity of the formed film surface is suppressed. As a result, in the oxide semiconductor film 103, a region in which a concentration of silicon distributed from an interface with the gate insulating film 102 toward an inside of the oxide semiconductor film 103 is lower than or equal to 1.0 at.% is formed. Such a region is referred to as a region 103a. The concentration of silicon included in the region 103a is further preferably lower than or equal to 0.1 at.%. Further, the region 103a is provided to be in contact with the gate insulating film 102 and have a thickness less than or equal to 5 nm.

[0070]

Note that a region in the oxide semiconductor film 103 other than the region 103a is referred to as a region 103b. The concentration of silicon included in the region 103b is lower than the concentration of silicon included in the region 103a.

[0071]

Further, in the case where impurities such as carbon is included in the gate insulating film 102, such impurities might also enter the oxide semiconductor film 103 and serve as impurities, as in the case of silicon. In that case, the concentration of carbon included in the region 103a is lower than or equal to 1.0×10^{20} atoms/cm^3, preferably lower than or equal to 1.0×10^{19} atoms/cm^3.

[0072]

As described above, the concentration of impurities such as silicon entering the region 103a in the oxide semiconductor film 103 is reduced, whereby change in characteristics of the transistor 110 can be suppressed. In addition, crystallization of the oxide semiconductor film 103 can be progressed in the vicinity of the formed film surface. Further, in the case where the oxide semiconductor film 103 is a CAAC-OS film, a crystal portion can be formed even in the vicinity of the formed film surface. When transistors using such oxide semiconductor films are manufactured, a semiconductor device with stable electric characteristics can be obtained.

[0073]

Note that the details of the other components of the transistor are described in description of a method for manufacturing the transistor 110 below, with reference to FIGS. 4A to 4E.

[0074]

Over the transistor 110, a planarity insulating film may be further formed. Further, openings may be formed in the gate insulating film 102, the protective insulating film 109, and the like in order that the source electrode 105a and the drain electrode 105b may be electrically connected to a wiring. Furthermore, a second gate electrode may further be provided above the oxide semiconductor film 103 to overlap with the gate electrode 101.

[0075]

FIGS. 2A and 2B illustrate a transistor 120 having a different structure from that of the transistor 110 illustrated in FIGS. 1A and 1B. FIG. 2A is a plan view, and FIG. 2B is a cross-sectional view taken along C-D line in FIG. 2A. Note that part of components of the transistor 120 (e.g., the protective insulating film 109 and the like) is not illustrated in FIG. 2A for brevity.

[0076]

The transistor 120 illustrated in FIGS. 2A and 2B includes, over a substrate 100 having an insulating surface, a gate electrode 101, a gate insulating film 102 covering the gate electrode 101, an oxide semiconductor film 103 provided to be in contact with the gate insulating film 102 and overlap with at least the gate electrode 101, a source electrode 105a and a drain electrode 105b electrically connected to the oxide semiconductor film 103, and a protective insulating film 109 covering the oxide semiconductor film 103 and the source electrode 105a and the drain electrode 105b. A difference between the transistor 120 and the transistor 110 is that like the gate insulating film 102, an insulating film including oxidized material containing silicon is used as the protective insulating film 109 and that a region 103c is provided in the vicinity of an interface between the oxide semiconductor film 103 and the protective insulating film 109.

[0077]

The oxide semiconductor film 103 in the transistor 120 includes a region 103a, a region 103b, and the region 103c. The region 103a in the oxide semiconductor film 103 is a region where a concentration of silicon distributed from the interface with the gate insulating film 102 toward the inside of the oxide semiconductor film 103 is lower than or equal to 1.0 at.%. The region 103a is preferably provided to be in contact with the gate insulating film 102 and have a thickness less than or equal to 5 nm. The region 103c in the oxide semiconductor film 103 is a region where a concentration of silicon distributed from the interface with the protective insulating film 109 toward the inside of the oxide semiconductor film 103 is lower than or equal to 1.0 at.%. The region 103c is preferably provided to be in contact with the protective insulating film 109 and have a thickness less than or equal to 5 nm. In the oxide semiconductor film 103, a region between the region 103a and the region 103c is a region 103b.

[0078]

Note that the concentration of silicon included in the region 103b is lower than that of silicon included in the region 103a. The concentration of silicon included in the region 103a is further preferably lower than or equal to 0.1 at.%.

[0079]

Here, the concentration of silicon included in the region 103a is lower than or equal to 1.0 at.%, preferably lower than or equal to 0.1 at.%, and the concentration of silicon included in the region 103c is also lower than or equal to 1.0 at.%, preferably lower than or equal to 0.1 at.%. At this time, the concentration of silicon included in the region 103b is lower than the concentrations of silicon included in the region 103a and the region 103c.

[0080]

As described above, also in the region 103c corresponding to a back channel of the oxide semiconductor film 103, the concentration of impurities such as silicon is reduced, so that change in electric characteristics of the transistor 120 can be suppressed.

[0081]

The other components are same as those of the semiconductor device illustrated in FIGS. 1A and 1B; thus, the description on FIGS. 1A and 1B can be referred to for the details.

[0082]

Although the transistors illustrated in FIGS. 1A and 1B and FIGS. 2A and 2B are so-called channel-etched type transistors, semiconductor devices shown in this embodiment are not limited thereto. FIGS. 3A and 3B illustrate a channel-stop type transistor 130, which is different from the transistors illustrated in FIGS. 1A and 1B and FIGS. 2A and 2B. FIG. 3A is a plan view, and FIG. 3B is a cross-sectional view taken along line E-F in FIG. 3A. Note that part of components of the transistor 130 (e.g., the protective insulating film 109 and the like) is not illustrated in FIG. 3A to avoid complexity. Further, in FIG. 3A, a channel protective film 108 is three-dimensionally illustrated for easy understanding.

[0083]

The transistor 130 illustrated in FIGS. 3A and 3B includes, over a substrate 100 having an insulating surface, a gate electrode 101, a gate insulating film 102 covering the gate electrode 101, an oxide semiconductor film 103 provided to be in contact with the gate insulating film 102 and overlap with at least the gate electrode 101, the channel protective film 108 provided over and in contact with the oxide semiconductor film 103, a source electrode 105a and a drain electrode 105b which are provided over the channel protective film 108 and electrically connected to the oxide semiconductor film 103, and a protective insulating film 109 covering the oxide semiconductor film 103 and the source electrode 105a and the drain electrode 105b. In addition, as in the case of the transistor 110, the oxide semiconductor film 103 includes a region 103a and a region 103b. In other words, a difference from the transistor 110 is that the transistor 130 includes the channel protective film 108.

[0084]

As the channel protective film 108, an inorganic insulating film containing oxygen is preferably used. For example, an insulating film such as a silicon oxide film, a silicon oxynitirde film, an aluminum oxide film, an aluminum oxynitride film, a gallium oxide film, or a hafnium oxide film can be used. The preferable thickness of the channel protective film 108 is greater than or equal to 5 nm and less than or equal to 300 nm.

[0085]

The channel protective film 108 is provided over and in contact with the oxide semiconductor film 103 as described, whereby damage on the oxide semiconductor film 103 on the back channel side, which is caused by etching the source electrode 105a and the drain electrode 105b (e.g., damage caused by plasma or an etchant in etching treatment), can be prevented. Thus, the transistor 130 can obtain stable electric characteristics.

[0086]

Further, as illustrated in FIG. 3B, an end portion of the channel protective film 108 has a taper angle greater than or equal to 10° and less than or equal to 60°. The channel protective film 108 is formed to have such a shape, whereby the electric field concentration in the vicinity of a lower end portion of the channel protective film 108 can be relaxed.

[0087]

The other components are the same as those in the semiconductor device illustrated in FIGS. 1A and 1B; thus, the description on FIGS. 1A and 1B can be referred to for the details.

[0088]

<Example of Manufacturing Process of Transistor>

Examples of a manufacturing process of the transistor in FIGS. 1A and 1B, FIGS. 2A and 2B, and FIGS. 3A and 3B will be described below with reference to FIGS. 4A to 4E and FIGS. 5A to 5E.

[0089]

<Manufacturing Process of Transistor 110>

An example of a manufacturing process of the transistor 110 in FIGS. 1A and 1B will be described with reference to FIGS. 4A to 4E.

[0090]

First, the substrate 100 having an insulating surface is prepared. There is no particular limitation on a substrate that can be used as the substrate 100 having an insulating surface as long as it has at least heat resistance to withstand heat treatment performed later. For example, a glass substrate of barium borosilicate glass, aluminoborosilicate glass, or the like, a ceramic substrate, a quartz substrate, or a sapphire substrate can be used. As long as the substrate 100 has an insulating surface, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate of silicon, silicon carbide, or the like; a compound semiconductor substrate of silicon germanium or the like; an SOI substrate; or the like can be used.

[0091]

A flexible substrate may alternatively be used as the substrate 100. When a flexible substrate is used, a transistor including the oxide semiconductor film 103 may be directly formed over the flexible substrate. Alternatively, a transistor including the oxide semiconductor film 103 may be formed over a manufacturing substrate, and then, the transistor may be separated and transferred to a flexible substrate. Note that in order to separate the transistor from the manufacturing substrate and transfer it to the flexible substrate, a separation layer may be provided between the manufacturing substrate and the transistor including the oxide semiconductor film 103.

[0092]

An insulating film functioning as a base film may be provided between the substrate 100 and the gate electrode 101. The base film has a function of preventing diffusion of impurities such as hydrogen or moisture from the substrate 100, and can be formed to have a single layer or stacked structure using one or more films selected from a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, and a silicon oxynitride film.

[0093]

Next, a conductive film used for formation of a gate electrode (as well as a wiring formed in the same layer as the gate electrode) is formed over the substrate 100. The conductive film used for the gate electrode can be formed using, for example, a metal material such as molybdenum, titanium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material including any of these materials as a main component. Alternatively, the conductive film used for the gate electrode may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), indium tin oxide (In_2O_3-SnO_2, which is abbreviated to ITO in some cases), indium zinc oxide (In_2O_3-ZnO), or any of these metal oxide materials in which silicon or silicon oxide is included can be used. The gate electrode can be formed to have a single layer or a stacked structure using any of the above materials. There is no particular limitation on the method for forming the conductive film, and a variety of film formation methods such as an evaporation method, a CVD method, a sputtering method, or a spin coating method can be employed.

[0094]

Next, a resist mask is formed over the conductive film through a photolithography step and selective etching is performed, so that the gate electrode 101 is formed. Then, the resist mask is removed. The resist mask used for forming the gate electrode 101 may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask; thus, manufacturing cost can be reduced. For etching the gate electrode 101, wet etching, dry etching, or both of them may be employed.

[0095]

Next, the gate insulating film 102 is formed to cover the gate electrode 101 (see

FIG. 4A). The gate insulating film 102 can have a thickness greater than or equal to 1 nm and less than or equal to 500 nm, for example. There is no particular limitation on the method for forming the gate insulating film 102; for example, a sputtering method, an MBE method, a CVD method, a pulse laser deposition method, an ALD method, or the like can be used as appropriate for formation of the gate insulating film 102.

[0096]

For the gate insulating layer 102, an oxide insulating film having a sufficient withstand voltage and a sufficient insulating property is preferably used. In the case where the gate insulating film 102 has a single-layer structure, an insulating film including oxidized material containing silicon, such as a silicon oxide film, may be used.

[0097]

Alternatively, the gate insulating film 102 may have a stacked structure. In the case where the gate insulating film 102 has a stacked structure, silicon oxide may be stacked over gallium oxide, aluminum oxide, silicon nitride, silicon oxynitride, aluminum oxynitride, yttrium oxide, lanthanum oxide, silicon nitride oxide, or the like. Alternatively, silicon oxide may be stacked over a high-k material such as hafnium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate to which nitrogen is added ($HfSiO_xN_y$ ($x > 0$, $y > 0$)), or hafnium aluminate ($HfAl_xO_y$ ($x > 0$, $y > 0$)). The use of such a high-k material enables a reduction in gate leakage current.

[0098]

When an oxide insulating film is used as the gate insulating film 102, part of oxygen contained in the oxide insulating film can be released by performing heat treatment described later; thus, oxygen can be supplied to the oxide semiconductor film 103, and oxygen vacancies in the oxide semiconductor film 103 can be filled. In particular, the gate insulating film 102 preferably contains a large amount of oxygen which exceeds at least the stoichiometry in (a bulk of) the gate insulating film 102. For example, a film of silicon oxide represented by the formula $SiO_{2+\alpha}$ ($\alpha > 0$) is preferably used as the gate insulating film 102. When such a silicon oxide film is used as the gate insulating film 102, oxygen can be supplied to the oxide semiconductor film 103, so that the transistor 110 using the oxide semiconductor film 103 can have

favorable transistor characteristics.

[0099]

Further, before the oxide semiconductor film 103 is formed, planarization treatment may be performed on the gate insulating film 102. Although not particularly limited, the planarization treatment can be dry etching, plasma treatment, polishing (e.g., chemical mechanical polishing (CMP)), or the like.

[0100]

As plasma treatment, reverse sputtering in which an argon gas is introduced and plasma is generated can be performed. The reverse sputtering is a method in which voltage is applied to a substrate side with use of an RF power source in an argon atmosphere and plasma is generated in the vicinity of the substrate so that a surface is modified. Note that instead of an argon atmosphere, a nitrogen atmosphere, a helium atmosphere, an oxygen atmosphere, or the like may be used. The reverse sputtering can remove particle substances (also referred to as particles or dust) attached to a surface where the oxide semiconductor film 103 is formed.

[0101]

As the planarization treatment, polishing treatment, dry-etching treatment, or plasma treatment may be performed plural times and/or in combination. In the case where the treatments are combined, the order of steps is not particularly limited and may be set as appropriate in accordance with roughness of the surface where the oxide semiconductor film 103 is formed.

[0102]

Further, in order that hydrogen or water may be contained in the oxide semiconductor film 103 as little as possible in a formation step of the oxide semiconductor film 103, it is preferable that the substrate 100 on which the gate insulating film 102 is already formed be preheated in a preheating chamber of a sputtering apparatus as pretreatment for formation of the oxide semiconductor film 103 so that impurities such as hydrogen and moisture adsorbed to the substrate 100 and the gate insulating film 102 are removed and evacuated. As an evacuation unit provided in the preheating chamber, a cryopump is preferable.

[0103]

Next, over the gate insulating film 102, the oxide semiconductor film 103

having a thickness greater than 5 nm and less than or equal to 200 nm, preferably greater than or equal to 10 nm and less than or equal to 30 nm is formed (see FIG. 4B). The oxide semiconductor film 103 preferably has a structure with crystallinity of single crystal or microcrystal. Further, the oxide semiconductor film 103 is preferably a CAAC-OS film. Note that it is preferable that the gate insulating film 102 and the oxide semiconductor film 103 be formed successively without being exposed to air.

[0104]

In this embodiment, as the oxide semiconductor film 103, an oxide semiconductor film is formed using an In-Ga-Zn-based oxide target by a sputtering method. Alternatively, the oxide semiconductor film 103 can be formed by a sputtering method in a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere of a rare gas and oxygen.

[0105]

As a target used for forming an In-Ga-Zn-O film as the oxide semiconductor film 103 by a sputtering method, for example, an oxide target with an atomic ratio where In: Ga: Zn =1:1:1, an oxide target with an atomic ratio where In: Ga: Zn =3:1:2, or an oxide target with an atomic ratio where In: Ga: Zn =2:1:3 can be used. However, a material and composition of a target used for formation of the oxide semiconductor film 103 is not limited to the above.

[0106]

The relative density of the oxide target is higher than or equal to 90 % and lower than or equal to 100 %, preferably higher than or equal to 95 % and lower than or equal to 99.9 %. By using the oxide target with high relative density, the oxide semiconductor film 103 can be a dense film.

[0107]

It is preferable that a high-purity gas from which impurities such as hydrogen, water, a hydroxyl group, or a hydride is removed be used as the sputtering gas for the formation of the oxide semiconductor film 103.

[0108]

There are three heating methods for forming a CAAC-OS film when the CAAC-OS film is used as the oxide semiconductor film 103. One of the methods

(first method) is to form an oxide semiconductor film at a temperature higher than or equal to 200 °C and lower than or equal to 450 °C to form, in the oxide semiconductor film, crystal portions in which the c-axes are aligned in the direction perpendicular to a surface where the oxide semiconductor film is formed or a surface of the oxide semiconductor film. Another method (second method) is to form an oxide semiconductor film with a small thickness and then heat it at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C, to form, in the oxide semiconductor film, crystal portions in which the c-axes are aligned in the direction perpendicular to a surface where the oxide semiconductor film is formed or a surface of the oxide semiconductor film. The other method (third method) is to form a first oxide semiconductor film with a small thickness, then heat it at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C, and form a second oxide semiconductor film, to form, in the oxide semiconductor film, crystal portions in which the c-axes are aligned in the direction perpendicular to a surface where the oxide semiconductor film is formed or a surface of the oxide semiconductor film.

[0109]

By heating the substrate 100 during film formation, the concentration of impurities such as hydrogen or water in the oxide semiconductor film 103 can be reduced. In addition, damage by sputtering can be reduced, which is preferable.

[0110]

Note that when an oxide semiconductor film having crystallinity (single crystal or microcrystal) different from the CAAC-OS film is formed as the oxide semiconductor film 103, the film formation temperature is not particularly limited.

[0111]

In the case where a CAAC-OS film is used as the oxide semiconductor film 103, for example, the CAAC-OS film is deposited by a sputtering method with a polycrystalline oxide semiconductor sputtering target. When ions collide with the sputtering target, a crystal region included in the sputtering target may be separated from the target along an a-b plane; in other words, a sputtered particle having a plane parallel to an a-b plane (flat-plate-like sputtered particle or pellet-like sputtered particle) may flake off from the sputtering target. In that case, the flat-plate-like sputtered

particle reaches a substrate while keeping their crystal state, whereby the CAAC-OS film can be formed.

[0112]

For the deposition of the CAAC-OS film, the following conditions are preferably used.

[0113]

By reducing the amount of impurities entering the CAAC-OS film during the deposition, the crystal state can be prevented from being broken by the impurities. For example, the concentration of impurities (e.g., hydrogen, water, carbon dioxide, or nitrogen) which exist in the deposition chamber may be reduced. Furthermore, the concentration of impurities in a deposition gas may be reduced. Specifically, a deposition gas whose dew point is −80 °C or lower, preferably −100 °C or lower is used.

[0114]

By increasing the substrate heating temperature during the deposition, migration of a sputtered particle is likely to occur after the sputtered particle reaches a substrate surface. Specifically, the substrate heating temperature during the deposition is higher than or equal to 100 °C and lower than or equal to 740 °C, preferably higher than or equal to 200 °C and lower than or equal to 500 °C. By increasing the substrate heating temperature during the deposition, when the flat-plate-like sputtered particle reaches the substrate, migration occurs on the substrate surface, so that a flat plane of the flat-plate-like sputtered particle is attached to the substrate.

[0115]

Furthermore, it is preferable that the proportion of oxygen in the deposition gas be increased and the power be optimized in order to reduce plasma damage at the deposition. The proportion of oxygen in the deposition gas is 30 vol.% or higher, preferably 100 vol.%.

[0116]

As an example of the sputtering target, a polycrystalline In-Ga-Zn-based oxide target is described below.

[0117]

The In-Ga-Zn-based oxide target, which is polycrystalline, is made by mixing InO_X powder, GaO_Y powder, and ZnO_Z powder in a predetermined molar ratio, applying pressure, and performing heat treatment at a temperature higher than or equal to 1000 °C and lower than or equal to 1500 °C. Note that X, Y, and Z are each a given positive number. Here, the predetermined molar ratio of InO_X powder to GaO_Y powder and ZnO_Z powder is, for example, 2:2:1, 8:4:3, 3:1:1, 1:1:1, 4:2:3, or 3:1:2. The kinds of powder and the molar ratio for mixing powder may be determined as appropriate depending on the desired sputtering target.

[0118]

Then, a sputtering gas from which hydrogen and moisture have been removed is introduced into the deposition chamber while moisture remaining therein is removed, and the oxide semiconductor film 103 is deposited over the substrate 100 with the use of the above target. In order to remove moisture remaining in the deposition chamber, an entrapment vacuum pump such as a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo pump provided with a cold trap. From the deposition chamber which is evacuated with a cryopump, a hydrogen atom, a compound containing a hydrogen atom such as water (H_2O) (more preferably, also a compound containing a carbon atom), and the like are removed, whereby the concentration of impurities such as hydrogen or moisture in the oxide semiconductor film 103 formed in the deposition chamber can be reduced.

[0119]

Note that in the case where the oxide semiconductor film 103 is formed by a sputtering method, when a particle for forming the oxide semiconductor film 103 collides with the gate insulating film 102, an element that is a constituent element of the gate insulating film 102 enters the oxide semiconductor film 103 (this phenomenon is called mixing or mixing effect). Such a mixing phenomenon significantly occurs in the oxide semiconductor film 103 in the vicinity of the interface with the gate insulating film 102, specifically occurs in the above-described region 103a. Since in the transistor described in this embodiment, a channel region is formed in the oxide semiconductor film 103 in the vicinity of the gate insulating film 102, a constituent element of the gate insulating film 102, which enters the region and serves as an impurity therein, may be a cause of a reduction in on-state characteristics (e.g., on-state

current) of the transistor.

[0120]

The possibility of mixing occurring in the vicinity of an interface between the gate insulating film 102 and the oxide semiconductor film 103 when the oxide semiconductor film 103 is formed over the gate insulating film 102 was examined by classical molecular dynamics calculation. Here, the results thereof are described. Note that simulation software "SCIGRESS ME" manufactured by Fujitsu Limited was used for the calculation.

[0121]

A model shown in FIG. 6 was formed using an amorphous silicon oxide (hereinafter, referred to as a-SiO_2) film as a gate insulating film. The size of a unit cell (a calculation unit cell) used in calculation is set to be 3 nm in the x-axis direction, 3 nm in the y-axis direction, and 7.5 nm in the z-axis direction. The x-axis and the y-axis refer to the directions parallel to the a-SiO_2 film, and the z-axis refers to the thickness direction of the a-SiO_2 film. Note that in the calculation, the periodic boundary condition is applied in the x-axis direction and the y-axis direction so that a film which is sufficiently large in the x-axis direction and the y-axis direction can be assumed.

[0122]

Next, indium atoms, gallium atoms, zinc atoms, and oxygen atoms whose ratio is 1:1:1:4 (the total number of atoms is 840) were ejected from the upper portion (in FIG. 6, an atom-generation portion) over the a-SiO_2 film toward the lower portion, and classical molecular dynamics calculation was performed at a temperature of 300 °C for 2 nsec (the time step: 0.2 fs, the number of steps: ten million). Note that one atom has an enrgy of 1 eV.

[0123]

FIGS. 7A to 7C and FIGS. 8A to 8C show the calculation results. FIG. 7A shows arrangement of oxygen atoms and silicon atoms at 0 sec; FIG. 7B shows arrangement of oxygen atoms, silicon atoms, gallium atoms, and zinc atoms after 1 nsec; and FIG. 7C shows arrangement of oxygen atoms, silicon atoms, gallium atoms, and zinc atoms after 2 nsec. FIG. 8A shows arrangement of oxygen atoms, silicon atoms, gallium atoms, and zinc atoms after 2 nsec; FIG. 8B shows arrangement of only

silicon atoms after 2 nsec; and FIG. 8C shows arrangement of indium atoms, gallium atoms, and zinc atoms after 2 nsec.

[0124]

By comparing the arrangement of only silicon atoms shown in FIG. 8B and the arrangement of indium atoms, gallium atoms, and zinc atoms shown in FIG. 8C, it was confirmed that the indium atoms, the gallium atoms, and the zinc atoms entered a layer of silicon atoms.

[0125]

The above calculation results indicate that by injecting indium atoms, gallium atoms, zinc atoms, and oxygen atoms into the a-SiO_2 film, a layer in which silicon atoms, indium atoms, gallium atoms, zinc atoms, and oxygen atoms are mixed is formed between the a-SiO_2 film and an IGZO film. Note that one atom has an enrgy of 1 eV.

[0126]

According to the above results, in order to prevent formation of a layer in which the oxide semiconductor film 103 and the gate insulating film 102 are mixed, it is effective to reduce an impact caused by collision of a particle for forming the oxide semiconductor film 103 with the gate insulating film 102. For achieving the above, a method in which the power for deposition of the oxide semiconductor film 103 is low or a method in which the pressure for deposition thereof is high can be used, for example. Alternatively, a distance between a target and a substrate over which the film is deposited (hereinafter, referred to as a T-S distance) may be increased.

[0127]

Note that mixing caused by sputtering is likely to be generated in the oxide semiconductor film 103 in the vicinity of the interface with the gate insulating film 102 as described above. Thus, part of the oxide semiconductor film in the vicinity of the interface is deposited by sputtering under the condition that the impact caused by a particle for forming the oxide semiconductor film 103, which collides with the gate insulating film 102 is low, and accordingly the mixing effect is reduced; after that, in performing the rest of deposition, the impact of collision may be increased. For example, part of the oxide semiconductor film 103 in the vicinity of the interface may be deposited under the condition that the power for depositing the oxide semiconductor film 103 is low, and then, deposition of the oxide semiconductor film may be carried on

under the condition that the deposition power is increased. Alternatively, part of the oxide semiconductor film 103 in the vicinity of the interface may be deposited under the condition that the pressure for depositing the oxide semiconductor film 103 is high, and then, deposition of the oxide semiconductor film may be carried on under the condition that the deposition pressure is reduced. Further alternatively, part of the oxide semiconductor film 103 in the vicinity of the interface may be deposited under the condition that the T-S distance is large, and then, deposition of the oxide semiconductor film may be carried on under the condition that the T-S distance is decreased.

[0128]

The specific value of the deposition power is 5 kW or lower, preferably, 1 kW or lower, further preferably 500 W or lower, furthermore preferably, 200 W or lower. However, as the deposition power is reduced, the deposition rate of the oxide semiconductor film 103 is decreased. Further, in the case where the deposition power is significantly low, plasma is less likely to be generated in a sputtering apparatus, and the possibility that normal deposition treatment cannot be performed is increased. Thus, it is preferable that the deposition power be 5 % (or higher) of the maximum power that can be applied in the sputtering apparatus. In considering a reduction in the deposition power, a practitioner may select the optimum power value as appropriate in terms of performance of the sputtering apparatus or the thickness of the oxide semiconductor film 103 so that deposition can be normally performed, as long as the manufacturing process of the transistor 110 (cycle time) is not significantly affected by the deposition time.

[0129]

The specific value of the deposition pressure is 0.4 Pa or higher, preferably, 1.0 Pa or higher, further preferably 2.0 Pa or higher, furthermore preferably, 5.0 Pa or higher. However, as the deposition pressure is increased, quality of a film that is to be deposited tends to deteriorate (e.g., the film quality is sparse). Thus, it is preferable that the deposition pressure is 100 Pa or lower. In considering an increase in the deposition pressure, a practitioner may select the optimum pressure value as appropriate in terms of characteristics necessary for the oxide semiconductor film 103 (e.g., field-effect mobility or the like).

[0130]

The specific value of the T-S distance is 30 mm or more, preferably 50 mm or more, further preferably 100 mm or more, furthermore preferably 300 mm or more. Note that as the T-S distance is extremely increased, the deposition rate of the oxide semiconductor film 103 is decreased. Thus, it is preferable that the T-S distance be 500 mm or less. In considering an increase in the T-S distance, a practitioner may select the optimum T-S distance as appropriate as long as the manufacturing process of the transistor 110 (cycle time) is not significantly affected by the deposition time.

[0131]

Note that in order to reduce the impact of a particle for forming the oxide semiconductor film 103, which collides with the gate insulating film 102, the oxide semiconductor film 103 may be deposited in a state where one or more of the conditions of deposition power, deposition pressure, and T-S distance are set in the above range.

[0132]

In the case where as the sputtering apparatus, a magnetron-type sputtering apparatus in which a target and a substrate over which a film is to be deposited are set in substantially parallel to each other (simply the apparatus is also called a magnetron sputtering apparatus) is used, besides a particle for forming the oxide semiconductor film 103, plasma, a secondary electron, or the like collides with the gate insulating film 102; thus, an element included in the gate insulating film 102 is more likely to enter the oxide semiconductor film 103. Therefore, as a sputtering apparatus used for depositing the oxide semiconductor film 103, a facing-target-type sputtering apparatus (also called mirrortron sputtering apparatus) may be used. In the apparatus, two targets are set to face each other, a substrate over which a film is to be deposited is set in a portion other than a space sandwiched between the two targets to be in a direction substantially perpendicular to the targets. Then, high-density plasma is generated between the two targets facing each other, and surfaces of the targets (which are used for deposition of the oxide semiconductor film 103) are sputtered by the plasma, whereby the oxide semiconductor film 103 is deposited over the substrate. Thus, the substrate where a film is to be deposited is not (or hardly) exposed to plasma or a secondary electron directly.

[0133]

Further, in the case where the oxide semiconductor film 103 is deposited by

sputtering in a rare gas atmosphere, helium may be used instead of argon. When helium whose atomic weight is smaller than that of argon is used, the impact of a particle for forming the oxide semiconductor film 103, which collides with the gate insulating film 102, can be reduced. Furthermore, after part of the oxide semiconductor film 103 in the vicinity of the interface with the gate insulating film 102 is deposited in a helium atmosphere, the atmosphere in the deposition chamber is switched into an argon atmosphere, whereby the deposition rate of the oxide semiconductor film 103 can be increased.

[0134]

Alternatively, the oxide semiconductor film 103 may be deposited by a method by which the impact on the gate insulating film 102 is small, such as an atomic layer deposition (ALD) method, an evaporation method, or a coating method.

[0135]

As described above, the oxide semiconductor film 103 is deposited under the condition that the impact of a particle for forming the oxide semiconductor film 103, which collides with the gate insulating film 102 is reduced, so that in the oxide semiconductor film 103, the region 103a where a concentration of silicon distributed from an interface with the gate insulating film 102 toward the inside of the oxide semiconductor film 103 is lower than or equal to 1.0 at.% and the region 103b where silicon is lower than that in the region 103a are formed. Here, the region 103b indicates a region in the oxide semiconductor film 103 other than the region 103a. Further, the concentration of silicon included in the region 103a is preferably lower than or equal to 0.1 at.%.

[0136]

Further, when the oxide semiconductor film 103 is deposited in such a manner, entry of impurities such as carbon included in the gate insulating film 102 into the oxide semiconductor film 103 can be also reduced. Thus, the concentration of carbon included in the region 103a is lower than or equal to 1.0×10^{20} atoms/cm^3, preferably lower than or equal to 1.0×10^{19} atoms/cm^3.

[0137]

In the case where a CAAC-OS film is formed as the oxide semiconductor film

103 while being heated (the first method), the amount of impurities such as silicon entering the region 103a is reduced, so that a crystal portion in which a c-axis is aligned in a direction perpendicular to a formed film surface or a surface of the oxide semiconductor film can be formed even in the vicinity of the formed film surface of the CAAC-OS film.

[0138]

Further, when the oxide semiconductor film 103 is deposited under the conduction that the impact of a particle for forming the oxide semiconductor film 103, which collides with the gate insulating film 102 is reduced, entry of the constituent element of the oxide semiconductor film 103 into the gate insulating film 102 can be suppressed. Thus, entry of the constituent element having high conductivity, such as a metal element, of the oxide semiconductor film 103 into the gate insulating film 102 can be suppressed, and accordingly, a reduction in resistivity of the gate insulating film 102 can be prevented.

[0139]

After the oxide semiconductor film 103 is deposited, heat treatment may be performed on the oxide semiconductor film 103. The temperature of the heat treatment is higher than or equal to 200 °C and lower than or equal to 700 °C, or lower than the strain point of the substrate. When the heat treatment is performed, excess hydrogen (including water and a hydroxyl group) can be removed.

[0140]

In the case where a CAAC-OS film is formed by the second or third method, the above heat treatment is performed, so that a crystal portion in which a c-axis is aligned in a direction perpendicular to a formed film surface or a surface of the oxide semiconductor film can be formed. In addition, the concentration of impurities such as silicon is reduced in the region 103a in the oxide semiconductor film 103; thus, the crystal portion can be formed even in the vicinity of the formed film surface of the oxide semiconductor film 103.

[0141]

The heat treatment can be performed in such a manner that, for example, an object to be processed is introduced into an electric furnace in which a resistance heater

or the like is used and heated at 450 °C in a nitrogen atmosphere for one hour. During the heat treatment, the oxide semiconductor film 103 is not exposed to air to prevent entry of water and hydrogen.

[0142]

The heat treatment apparatus is not limited to the electric furnace and may be an apparatus for heating an object by thermal radiation or thermal conduction from a medium such as a heated gas. For example, a rapid thermal anneal (RTA) apparatus such as a gas rapid thermal anneal (GRTA) apparatus or a lamp rapid thermal anneal (LRTA) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for performing heat treatment using a high-temperature gas. As the gas, an inert gas which does not react with an object to be processed by heat treatment, such as nitrogen or a rare gas such as argon is used.

[0143]

For example, as the heat treatment, the GRTA process may be performed as follows. The object is put in a heated inert gas atmosphere, heated for several minutes, and taken out of the inert gas atmosphere. The GRTA process enables high-temperature heat treatment for a short time. Moreover, the GRTA process can be employed even when the temperature exceeds the upper temperature limit of the object. Note that the inert gas may be switched to a gas containing oxygen during the process.

[0144]

Note that as the inert gas atmosphere, an atmosphere that contains nitrogen or a rare gas (e.g., helium, neon, or argon) as its main component and does not contain water, hydrogen, or the like is preferably used. For example, the purity of nitrogen or a rare gas such as helium, neon, or argon introduced into a heat treatment apparatus is greater than or equal to 6N (99.9999 %), preferably greater than or equal to 7N (99.99999 %) (that is, the concentration of the impurities is less than or equal to 1 ppm, preferably less than or equal to 0.1 ppm).

[0145]

In addition, after the oxide semiconductor film 103 is heated by the heat treatment, a high-purity oxygen gas, a dinitrogen monoxide gas, a high-purity dinitrogen monoxide gas, or ultra dry air (the moisture amount is less than or equal to 20 ppm (-55 °C by conversion into a dew point), preferably less than or equal to 1 ppm, or further preferably less than or equal to 10 ppb, in the case where measurement is performed with use of a dew point meter of a cavity ring down laser spectroscopy (CRDS) system) may be introduced into the same furnace. It is preferable that water, hydrogen, or the like be not contained in the oxygen gas or the dinitrogen monoxide gas. Alternatively, the purity of the oxygen gas or the dinitrogen monoxide gas which is introduced into the heat treatment apparatus is preferably greater than or equal to 6N, further preferably greater than or equal to 7N (i.e., the impurity concentration in the oxygen gas or the dinitrogen monoxide gas is preferably less than or equal to 1 ppm, further preferably less than or equal to 0.1 ppm). By the effect of the oxygen gas or the dinitrogen monoxide gas, oxygen which is a main component of the oxide semiconductor and which has been reduced at the same time as the heat treatment is supplied, so that the oxide semiconductor film can be a high-purity and electrically i-type (intrinsic) oxide semiconductor film.

[0146]

In the case where a CAAC-OS film is formed by the third method, an oxide semiconductor film may be additionally formed. Thus, the additionally formed oxide semiconductor film can also have a crystal portion with use of the crystal portion as a seed in which a c-axis is aligned in a direction perpendicular to the formed film surface or the surface of the oxide semiconductor film.

[0147]

Note that in the case where an oxide semiconductor film having crystallinity (single crystal or microcrystalline) different from a CAAC-OS film is formed, by performing the heat treatment, the oxide semiconductor film can be crystallized. In addition, since the concentration of impurities such as silicon is reduced in the region 103a in the oxide semiconductor film 103, the oxide semiconductor film even in the vicinity of the formed film surface can be crystallized.

[0148]

Note that the case is described here in which before the oxide semiconductor

film is processed to have an island shape, the heat treatment is performed; however, one embodiment of the disclosed invention is not construed as being limited thereto. The heat treatment may be performed after the oxide semiconductor film is processed to have an island shape.

[0149]

Next, the oxide semiconductor film 103 is preferably processed into the island-shape oxide semiconductor film 103 by a photolithography step (see FIG. 4C). A resist mask which is used in the formation of the island-shaped oxide semiconductor film 103 may be formed by an ink-jet method. Formation of the resist mask by an inkjet method needs no photomask; thus, manufacturing cost can be reduced. Note that etching of the oxide semiconductor film 103 may be dry etching, wet etching, or both dry etching and wet etching.

[0150]

Here, as illustrated in FIG. 4C, an end portion of the oxide semiconductor film 103 preferably has a taper angle of 20° to 50°. When the oxide semiconductor film 103 has a perpendicular end portion, oxygen is easily released from the oxide semiconductor film 103. When the oxide semiconductor film 103 has a tapered end portion, generation of oxygen vacancies is suppressed, and thus generation of leakage current of the transistor 110 can be reduced.

[0151]

Next, a conductive film used for a source electrode and a drain electrode (as well as a wiring formed in the same layer as the gate electrode) is formed over the oxide semiconductor film 103. As the conductive film used for the source electrode and the drain electrode, for example, a metal film containing an element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, or tungsten, or a metal nitride film containing any of the above elements as its component (e.g., a titanium nitride film, a molybdenum nitride film, or a tungsten nitride film) can be used. Alternatively, the conductive film may have a structure in which a film of a high-melting-point metal such as titanium, molybdenum, or tungsten, or a nitride film of any of these metals (a titanium nitride film, a molybdenum nitride film, or a tungsten nitride film) is stacked on either or both of the bottom surface and the top surface of a metal film of aluminum, copper, or the like. Further, the conductive film used for the

source electrode and the drain electrode may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), indium tin oxide (In_2O_3-SnO_2, which is abbreviated to ITO in some cases), or indium zinc oxide (In_2O_3-ZnO) can be used. The conductive film used for the source electrode and the drain electrode can be formed using any of the above materials to have a single layer or a stacked structure. There is no particular limitation on the method for forming the conductive film, and a variety of film formation methods such as an evaporation method, a CVD method, a sputtering method, or a spin coating method can be employed.

[0152]

A resist mask is formed over the conductive film by a photolithography step, selective etching is performed so that the source electrode 105a and the drain electrode 105b are formed, and after that, the resist mask is removed (see FIG. 4D). For the light exposure for forming the resist mask in the photolithography step, ultraviolet, KrF laser, or ArF laser is preferably used. In this step, a channel length *L* of a transistor that is to be completed in a later step is determined by a distance between a lower end of the source electrode 105a and a lower end of the drain electrode 105b that are adjacent to each other over the oxide semiconductor film 103. When light exposure is performed for a channel length *L* smaller than 25 nm, the light exposure for forming the resist mask in the photolithography step may be performed using extreme ultraviolet light having an extremely short wavelength of several nanometers to several tens of nanometers, for example. In the light exposure by extreme ultraviolet light, the resolution is high and the focus depth is large. Thus, the channel length *L* of the transistor formed later can be reduced, whereby the operation speed of a circuit can be increased.

[0153]

In order to reduce the number of photomasks used in a photolithography step and reduce the number of photolithography steps, an etching step may be performed with use of a multi-tone mask which is a light-exposure mask through which light is transmitted to have a plurality of intensities. A resist mask formed with use of a multi-tone mask has a plurality of thicknesses and further can be changed in shape by etching; therefore, the resist mask can be used in a plurality of etching steps for

processing into different patterns. Therefore, a resist mask corresponding to at least two kinds or more of different patterns can be formed by one multi-tone mask. Thus, the number of light-exposure masks can be reduced and the number of corresponding photolithography steps can be also reduced, whereby simplification of a process can be achieved.

[0154]

Note that it is preferable that etching conditions be optimized so as not to etch and divide the oxide semiconductor film 103 when the conductive film is etched. However, it is difficult to obtain etching conditions in which only the conductive film is etched and the oxide semiconductor film 103 is not etched at all. In some cases, only part of the oxide semiconductor film 103, e.g., 5 % to 50 % in thickness of the oxide semiconductor film 103, is etched, so that the oxide semiconductor film 103 has a groove portion (a recessed portion) when the conductive film is etched.

[0155]

Next, the protective insulating film 109 which covers the source electrode 105a and the drain electrode 105b and is in contact with part of the oxide semiconductor film 103 is formed (see FIG. 4E). The protective insulating film 109 may be formed using an inorganic insulating film as a single layer or a stacked layer of any of oxide insulating films such as a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, a gallium oxide film, and a hafnium oxide film. Further, over the above oxide insulating film, a single layer or a stacked layer of any of nitride insulating films such as a silicon nitride film, a silicon nitride oxide film, an aluminum nitride film, and an aluminum nitride oxide film may be formed. For example, a silicon oxide film and an aluminum oxide film are sequentially formed to be stacked on the source electrode 105a and the drain electrode 105b side by a sputtering method.

[0156]

Note that in this step, in the case where the protective insulating film 109 is formed by a sputtering method, it is effective to reduce the impact of a particle for forming the protective insulating film 109, which collides with the oxide semiconductor film 103, as like formation of the oxide semiconductor film 103. Thus, the region 103c is formed in the vicinity of the interface between the oxide semiconductor film

103 and the protective insulating film 109. Through this step, the transistor 120 illustrated in FIGS. 2A and 2B can be obtained. The region 103c in the oxide semiconductor film 103 is a region where a concentration of silicon distributed from an interface with the protective insulating film 109 toward the inside of the oxide semiconductor film 103 is lower than or equal to 1.0 at.%. The region 103c is preferably provided to be in contact with the protective insulating film 109 and have a thickness less than or equal to 5 nm.

[0157]

Here, as the protective insulating film 109, an insulating film similar to the gate insulating film 102 can be used. In order to prevent impurities such as silicon from entering the oxide semiconductor film 103, mixing may be suppressed in the vicinity of the interface between the oxide semiconductor film 103 and the protective insulating film 109; thus, the impact of silicon included in the protective insulating film 109 colliding with the oxide semiconductor film 103 may be reduced. For example, as an applicable method, the power for depositing the protective insulating film 109 is reduced, the pressure for depositing the protective insulating film 109 is increased, or the T-S distance is increased.

[0158]

As described above, the concentration of impurities such as silicon can also be reduced in the region 103c corresponding to the back channel of the oxide semiconductor film 103.

[0159]

After the above steps, the manufacturing method of the transistor 110 and that of the transistor 120 are similar to each other.

[0160]

After the protective insulating film 109 is formed, heat treatment is preferably performed on the oxide semiconductor film 103. The temperature of the heat treatment is higher than or equal to 300 °C and lower than or equal to 700 °C, or lower than the strain point of the substrate.

[0161]

The heat treatment may be performed in an atmosphere of nitrogen, oxygen,

ultra-dry air (the moisture content is less than or equal to 20 ppm, preferably less than or equal to 1 ppm, further preferably less than or equal to 10 ppb), or a rare gas (such as argon or helium). Note that it is preferable that water, hydrogen, and the like be not contained in the atmosphere of nitrogen, oxygen, ultra-dry air, a rare gas, or the like. It is also preferable that the purity of nitrogen, oxygen, or the rare gas which is introduced into a heat treatment apparatus be set to greater than or equal to 6N (99.9999 %), preferably greater than or equal to 7N (99.99999 %) (that is, the impurity concentration is lower than or equal to 1 ppm, preferably lower than or equal to 0.1 ppm).

[0162]

In the case of performing heat treatment after formation of the oxide semiconductor film, oxygen that is one of main component materials included in the oxide semiconductor might be reduced. However, during the heat treatment in this step, oxygen can be supplied to the oxide semiconductor film 103 from the gate insulating film 102 which is formed using oxidized material containing silicon; thus, oxygen vacancies in the oxide semiconductor film 103 can be filled.

[0163]

By performing the heat treatment as described above, the oxide semiconductor film 103 can be highly purified so as not to contain impurities other than main components as little as possible. In addition, the highly purified oxide semiconductor film 103 includes extremely few (close to zero) carriers derived from a donor, and the carrier concentration thereof is lower than 1×10^{14} /cm^3, preferably lower than 1×10^{12} /cm^3, further preferably lower than 1×10^{11} /cm^3. In such a manner, the oxide semiconductor film 103 that becomes an i-type (intrinsic) oxide semiconductor can be formed.

[0164]

Through the above steps, the transistor 110 is formed (see FIG. 4E). In the transistor 110, the concentration of impurities such as silicon taken into the region 103a of the oxide semiconductor film 103 is small. Thus, the transistor 110 can have stable electric characteristics.

[0165]

A planarization insulating film may be formed over the transistor 110. For the

planarization insulating film, a heat-resistant organic material such as an acrylic resin, a polyimide resin, a benzocyclobutene-based resin, a polyamide resin, or an epoxy resin can be used. Other than such organic materials, it is also possible to use a low-dielectric constant material (a low-k material), a siloxane-based resin, PSG (phosphosilicate glass), BPSG (borophosphosilicate glass), or the like. Note that the planarization insulating film may be formed by stacking a plurality of insulating films formed of any of these materials.

[0166]

<Manufacturing Process of Transistor 130>

Next, an example of a manufacturing process of the transistor 130 in FIG. 3A and 3B will be described with reference to FIGS. 5A to 5E.

[0167]

First, over the substrate 100, the gate electrode 101, the gate insulating film 102, and the oxide semiconductor film 103 including the region 103a and the region 103b are formed by steps similar to those (up to the step illustrated in FIG. 4C) of the transistor 110 (see FIG. 5A). For the details of the substrate 100, the gate electrode 101, the gate insulating film 102, and the oxide semiconductor film 103, the description with reference to FIGS. 4A to 4C can be referred to.

[0168]

Next, an insulating film 107 used for a channel protective film is formed to a thickness greater than or equal to 5 nm and less than or equal to 300 nm (see FIG. 5B). As the insulating film 107, an inorganic insulating film containing oxygen is preferably used. For example, an insulating film such as a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, a gallium oxide film, or a hafnium oxide film can be used. There is no particular limitation on a method for forming the insulating film 107; for example, a sputtering method, a MBE method, a CVD method, a pulse laser deposition method, an ALD method, or the like can be used as appropriate.

[0169]

Next, a resist mask is formed over the insulating film 107 by a photolithography step, the channel protective film 108 is formed by etching, and then, the resist mask is removed (see FIG. 5C). Note that a resist mask used for forming the

channel protective film 108 may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask; thus, manufacturing cost can be reduced. Note that the etching of the channel protective film 108 may be performed using either dry etching or wet etching, or using both dry etching and wet etching.

[0170]

As illustrated in FIG. 5C, an end portion of the channel protective film 108 preferably has a taper angle greater than or equal to 10 ° less than or equal to 60 °. The channel protective film 108 is formed to have such a shape, whereby the field concentration in the vicinity of a lower end portion of the channel protective film 108 can be relaxed.

[0171]

As described above, the channel protective film 108 is provided over and in contact with the oxide semiconductor film 103, so that damage on the back channel side of the oxide semiconductor film 103, which is caused by etching the source electrode 105a and the drain electrode 105b (e.g., damage caused by plasma or an etchant in the etching step), can be prevented. Accordingly, a semiconductor device including an oxide semiconductor and having stable electric characteristics can be provided.

[0172]

Next, a conductive film used for a source electrode and a drain electrode (as well as a wiring formed in the same layer as the gate electrode) is formed over the channel protective film 108 and the oxide semiconductor film 103. Then, the conductive film is selectively etched by a photolithography step, so that the source electrode 105a and the drain electrode 105b are formed (see FIG. 5D). This step can be performed in a manner similar to the step illustrated in FIG. 4D; thus, for the details of the source electrode 105a and the drain electrode 105b, the description with reference to FIG. 4D can be referred to.

[0173]

Next, the protective insulating film 109 is formed to cover the source electrode 105a, the drain electrode 105b, and the channel protective film 108 (see FIG. 5E). This step can be performed in a manner similar to the step illustrated in FIG. 4E; thus for the details of the protective insulating film 109, the description with reference to FIG. 4E can be referred to.

[0174]

As described above, the oxide semiconductor film is formed, whereby the concentration of impurities included in the oxide semiconductor film in the vicinity of the formed film surface can be reduced. In addition, crystallization of the oxide semiconductor film 103 can be progressed in the vicinity of the formed film surface; thus, crystallinity of the oxide semiconductor film 103 can be improved. In the case where the oxide semiconductor film 103 is a CAAC-OS film, a crystal portion can be formed even in the vicinity of the formed film surface. Note that in the crystal portion, a c-axis is aligned in a direction perpendicular to the interface between the oxide semiconductor film 103 and the gate insulating film 102 or the interface between the oxide semiconductor film 103 and the protective insulating film 109. By using such an oxide semiconductor film, a highly reliable semiconductor device having stable electric characteristics can be provided.

[0175]

The methods and structures described in this embodiment can be combined as appropriate with any of the methods and structures described in the other embodiments.

[0176]

(Embodiment 2)

A semiconductor device (also referred to as a display device) with a display function can be manufactured using the transistor an example of which is described in Embodiment 1. Moreover, some or all of the driver circuits which include the transistor can be formed over a substrate where the pixel portion is formed, whereby a system-on-panel can be obtained.

[0177]

In FIG. 9A, a sealant 4005 is provided so as to surround a pixel portion 4002 provided over a first substrate 4001, and the pixel portion 4002 is sealed by using a second substrate 4006. In FIG. 9A, a signal line driver circuit 4003 and a scan line driver circuit 4004 which are each formed using a single crystal semiconductor film or a polycrystalline semiconductor film over a substrate separately prepared are mounted in a region that is different from the region surrounded by the sealant 4005 over the first substrate 4001. Further, a variety of signals and potentials are supplied to the signal line driver circuit 4003 and the scan line driver circuit 4004, which are separately

formed, or the pixel portion 4002 from flexible printed circuits (FPCs) 4018a and 4018b.

[0178]

In FIGS. 9B and 9C, the sealant 4005 is provided so as to surround the pixel portion 4002 and the scan line driver circuit 4004 which are provided over the first substrate 4001. The second substrate 4006 is provided over the pixel portion 4002 and the scan line driver circuit 4004. Consequently, the pixel portion 4002 and the scan line driver circuit 4004 are sealed together with the display element, by the first substrate 4001, the sealant 4005, and the second substrate 4006. In FIGS. 9B and 9C, the signal line driver circuit 4003 which is formed using a single crystal semiconductor film or a polycrystalline semiconductor film over a substrate separately prepared is mounted in a region that is different from the region surrounded by the sealant 4005 over the first substrate 4001. In FIGS. 9B and 9C, various signals and potential are supplied to the signal line driver circuit 4003 which is separately formed, the scan line driver circuit 4004, and the pixel portion 4002 from an FPC 4018.

[0179]

Although FIGS. 9B and 9C each illustrate an example in which the signal line driver circuit 4003 is formed separately and mounted on the first substrate 4001, one embodiment of the present invention is not limited to this structure. The scan line driver circuit may be separately formed and then mounted, or only part of the signal line driver circuit or part of the scan line driver circuit may be separately formed and then mounted.

[0180]

Note that a connection method of a separately formed driver circuit is not particularly limited, and a chip on glass (COG) method, a wire bonding method, a tape automated bonding (TAB) method or the like can be used. FIG. 9A illustrates an example in which the signal line driver circuit 4003 and the scan line driver circuit 4004 are mounted by a COG method. FIG. 9B illustrates an example in which the signal line driver circuit 4003 is mounted by a COG method. FIG. 9C illustrates an example in which the signal line driver circuit 4003 is mounted by a TAB method.

[0181]

In addition, the display device includes a panel in which the display element is

sealed, and a module in which an IC or the like including a controller is mounted on the panel.

[0182]

Note that a display device in this specification means an image display device, a display device, or a light source (including a lighting device).

[0183]

Furthermore, the display device also includes the following modules in its category: a module to which a connector such as an FPC, a TAB tape, or a TCP is attached; a module having a TAB tape or a TCP at the tip of which a printed wiring board is provided; and a module in which an integrated circuit (IC) is directly mounted on a display element by a COG method.

[0184]

The pixel portion and the scan line driver circuit provided over the first substrate include a plurality of transistors, and the transistor described in Embodiment 1 can be applied thereto.

[0185]

As the display element provided in the display device, a liquid crystal element (also referred to as a liquid crystal display element) or a light-emitting element (also referred to as a light-emitting display element) can be used. The light-emitting element includes, in its category, an element whose luminance is controlled by a current or a voltage, and specifically includes, in its category, an inorganic electroluminescent (EL) element, an organic EL element, and the like. Furthermore, a display medium whose contrast is changed by an electric effect, such as electronic ink, can be used.

[0186]

Embodiments of the semiconductor device will be described with reference to FIG. 10, FIG. 11, and FIG. 12. FIG. 10, FIG. 11, and FIG. 12 correspond to cross-sectional views taken along line M-N in FIG. 9B.

[0187]

As illustrated in FIG. 10, FIG. 11, and FIG. 12, the semiconductor device includes a connection terminal electrode 4015 and a terminal electrode 4016. The connection terminal electrode 4015 and the terminal electrode 4016 are electrically connected to a terminal included in the FPC 4018 through an anisotropic conductive

film 4019.

[0188]

The connection terminal electrode 4015 is formed of the same conductive film as a first electrode layer 4030. The terminal electrode 4016 is formed of the same conductive film as a source electrode and a drain electrode of transistors 4010 and 4011.

[0189]

Further, the pixel portion 4002 and the scan line driver circuit 4004 provided over the first substrate 4001 each include a plurality of transistors. FIG. 10, FIG. 11, and FIG. 12 each illustrate the transistor 4010 included in the pixel portion 4002 and the transistor 4011 included in the scan line driver circuit 4004.

[0190]

In this embodiment, any of the transistors described in Embodiment 1 can be employed for the transistors 4010 and 4011. Variation in the electric characteristics of the transistors 4010 and 4011 is suppressed and the transistors 4010 and 4011 are electrically stable. Thus, as the semiconductor devices of this embodiment illustrated in FIG. 10, FIG. 11, and FIG. 12, a highly reliable semiconductor device can be provided.

[0191]

The transistor 4011 included in the scan line driver circuit 4004 has a structure in which a second gate electrode is formed over an insulating film 4034. A voltage applied to the second gate electrode is controlled, whereby the threshold voltage of the transistor 4011 can be controlled.

[0192]

The transistor 4010 included in the pixel portion 4002 is electrically connected to a display element to form a display panel. A variety of display elements can be used as the display element as long as display can be performed.

[0193]

An example of a liquid crystal display device using a liquid crystal element as a display element is illustrated in FIG. 10. In FIG. 10, a liquid crystal element 4013 which is a display element includes a first electrode layer 4030, a second electrode layer 4031, and a liquid crystal layer 4008. Note that the insulating films 4032 and 4033 functioning as alignment films are provided so that the liquid crystal layer 4008 is

interposed therebetween. The second electrode layer 4031 is provided on the second substrate 4006 side, and the first electrode layer 4030 and the second electrode layer 4031 are stacked, with the liquid crystal layer 4008 interposed therebetween.

[0194]

A spacer 4035 is a columnar spacer which is obtained by selective etching of an insulating film and is provided in order to control the thickness (a cell gap) of the liquid crystal layer 4008. Alternatively, a spherical spacer may be used.

[0195]

In the case where a liquid crystal element is used as the display element, a thermotropic liquid crystal, a low-molecular liquid crystal, a high-molecular liquid crystal, a polymer dispersed liquid crystal, a ferroelectric liquid crystal, an anti-ferroelectric liquid crystal, or the like can be used. Such a liquid crystal material exhibits a cholesteric phase, a smectic phase, a cubic phase, a chiral nematic phase, an isotropic phase, or the like depending on a condition.

[0196]

Alternatively, liquid crystal exhibiting a blue phase for which an alignment film is unnecessary may be used. A blue phase is one of liquid crystal phases, which is generated just before a cholesteric phase changes into an isotropic phase while temperature of cholesteric liquid crystal is increased. Since the blue phase appears only in a narrow temperature range, a liquid crystal composition in which several weight percent or more of a chiral material is mixed is used for the liquid crystal layer in order to improve the temperature range. The liquid crystal composition which includes a liquid crystal exhibiting a blue phase and a chiral material has a short response time of 1 msec or less and has optical isotropy, which contributes to the exclusion of the alignment process and reduction of viewing angle dependence. In addition, since an alignment film does not need to be provided and rubbing treatment is also unnecessary, electrostatic discharge damage caused by the rubbing treatment can be prevented and defects and damage of the liquid crystal display device in the manufacturing process can be reduced. Thus, productivity of the liquid crystal display device can be increased.

[0197]

The specific resistivity of the liquid crystal material is 1×10^9 Ω·cm or more,

preferably 1×10^{11} Ω·cm or more, much preferably 1×10^{12} Ω·cm or more. The value of the specific resistivity in this specification is measured at 20 °C.

[0198]

The size of storage capacitor formed in the liquid crystal display device is set considering the leakage current of the transistor provided in the pixel portion or the like so that charge can be held for a predetermined period. By using the transistor including the high-purity oxide semiconductor film, it is enough to provide a storage capacitor having a capacitance that is 1/3 or less, preferably 1/5 or less of a liquid crystal capacitance of each pixel.

[0199]

In the transistor used in this embodiment, which includes the highly purified oxide semiconductor film, the current in an off state (the off-state current) can be made small. Accordingly, an electrical signal such as an image signal can be held for a longer period in the pixel, and a writing interval can be set longer in an on state. Therefore, frequency of refresh operation can be reduced, which leads to an effect of suppressing power consumption.

[0200]

In addition, the transistor including the highly purified oxide semiconductor film used in this embodiment can have relatively high field-effect mobility and thus can operate at high speed. Therefore, by using the transistor in a pixel portion of a liquid crystal display device, a high-quality image can be provided. In addition, since the transistors can be separately provided in a driver circuit portion and a pixel portion over one substrate, the number of components of the liquid crystal display device can be reduced.

[0201]

For the liquid crystal display device, a twisted nematic (TN) mode, an in-plane-switching (IPS) mode, a fringe field switching (FFS) mode, an axially symmetric aligned micro-cell (ASM) mode, an optical compensated birefringence (OCB) mode, a ferroelectric liquid crystal (FLC) mode, an antiferroelectric liquid crystal (AFLC) mode, or the like can be used.

[0202]

A normally black liquid crystal display device such as a transmissive liquid crystal display device utilizing a vertical alignment (VA) mode is preferable. The vertical alignment mode is a method of controlling alignment of liquid crystal molecules of a liquid crystal display panel, in which liquid crystal molecules are aligned vertically to a panel surface when no voltage is applied. Some examples are given as the vertical alignment mode; for example, a multi-domain vertical alignment (MVA) mode, a patterned vertical alignment (PVA) mode, an advanced super-view (ASV) mode, or the like can be employed. Moreover, it is possible to use a method called domain multiplication or multi-domain design, in which a pixel is divided into some regions (subpixels) and molecules are aligned in different directions in their respective regions.

[0203]

In the display device, a black matrix (a light-blocking layer), an optical member (an optical substrate) such as a polarizing member, a retardation member, or an anti-reflection member, and the like are provided as appropriate. For example, circular polarization may be obtained by using a polarizing substrate and a retardation substrate. In addition, a backlight, a side light, or the like may be used as a light source.

[0204]

In addition, it is possible to employ a time-division display method (also called a field-sequential driving method) with use of a plurality of light-emitting diodes (LEDs) as a backlight. By employing a field-sequential driving method, color display can be performed without using a color filter.

[0205]

As a display method in the pixel portion, a progressive method, an interlace method or the like can be employed. Further, color elements controlled in a pixel at the time of color display are not limited to three colors: R, G, and B (R, G, and B correspond to red, green, and blue, respectively). For example, R, G, B, and W (W corresponds to white); R, G, B, and one or more of yellow, cyan, magenta, and the like; or the like can be used. Further, the sizes of display regions may be different between respective dots of color elements. However, one embodiment of the present invention is not limited to a color display device and can be applied to a monochrome display device.

[0206]

Alternatively, as the display element included in the display device, a light-emitting element utilizing electroluminescence can be used. Light-emitting elements utilizing electroluminescence are classified in accordance with whether a light-emitting material is an organic compound or an inorganic compound. In general, the former is referred to as an organic EL element, and the latter is referred to as an inorganic EL element.

[0207]

In an organic EL element, by application of voltage to a light-emitting element, electrons and holes are separately injected from a pair of electrodes into a layer containing a light-emitting organic compound, and current flows. The carriers (electrons and holes) are recombined, and thus, the light-emitting organic compound is excited. The light-emitting organic compound returns to a ground state from the excited state, thereby emitting light. Owing to such a mechanism, this light-emitting element is referred to as a current-excitation light-emitting element.

[0208]

The inorganic EL elements are classified in accordance with their element structures into a dispersion-type inorganic EL element and a thin-film inorganic EL element. A transistor and a light-emitting element are formed over a substrate. A dispersion-type inorganic EL element has a light-emitting layer where particles of a light-emitting material are dispersed in a binder, and its light emission mechanism is donor-acceptor recombination type light emission that utilizes a donor level and an acceptor level. A thin-film inorganic EL element has a structure where a light-emitting layer is sandwiched between dielectric layers, which are further sandwiched between electrodes, and its light emission mechanism is localized type light emission that utilizes inner-shell electron transition of metal ions. Note that an example of an organic EL element as a light-emitting element is described here.

[0209]

In order to extract light emitted from the light-emitting element, it is acceptable as long as at least one of a pair of electrodes is transparent. The light-emitting element can have a top emission structure in which light emission is extracted through the surface opposite to the substrate; a bottom emission structure in which light emission is extracted through the surface on the substrate side; or a dual emission structure in which

light emission is extracted through the surface opposite to the substrate and the surface on the substrate side, and a light-emitting element having any of these emission structures can be used.

[0210]

An example of a light-emitting device using a light-emitting element as a display element is illustrated in FIG. 11. A light-emitting element 4513 that is a display element is electrically connected to the transistor 4010 provided in the pixel portion 4002. A structure of the light-emitting element 4513 is not limited to the illustrated stacked-layer structure including the first electrode layer 4030, an electroluminescent layer 4511, and the second electrode layer 4031. The structure of the light-emitting element 4513 can be changed as appropriate depending on a direction in which light is extracted from the light-emitting element 4513, or the like.

[0211]

A partition wall 4510 can be formed using an organic insulating material or an inorganic insulating material. It is particularly preferable that the partition wall 4510 be formed using a photosensitive resin material to have an opening over the first electrode layer 4030 so that a sidewall of the opening is formed as a tilted surface with continuous curvature.

[0212]

The electroluminescent layer 4511 may be formed using a single layer or a plurality of layers stacked.

[0213]

A protective film may be formed over the second electrode layer 4031 and the partition wall 4510 in order to prevent entry of oxygen, hydrogen, moisture, carbon dioxide, or the like into the light-emitting element 4513. As the protective film, a silicon nitride film, a silicon nitride oxide film, a DLC film, or the like can be formed. In addition, in a space which is formed with the first substrate 4001, the second substrate 4006, and the sealant 4005, a filler 4514 is provided for sealing. It is preferable that a panel be packaged (sealed) with a protective film (such as a laminate film or an ultraviolet curable resin film) or a cover material with high air-tightness and little degasification so that the panel is not exposed to the outside air, in this manner.

[0214]

As the filler 4514, an ultraviolet curable resin or a thermosetting resin can be used as well as an inert gas such as nitrogen or argon. Examples of such a resin include polyvinyl chloride (PVC), an acrylic resin, a polyimide resin, an epoxy resin, a silicone resin, polyvinyl butyral (PVB), and ethylene vinyl acetate (EVA). For example, nitrogen is used for the filler.

[0215]

In addition, if needed, an optical film such as a polarizing plate, a circularly polarizing plate (including an elliptically polarizing plate), a retardation plate (a quarter-wave plate or a half-wave plate), or a color filter may be provided as appropriate on a light-emitting surface of the light-emitting element. Further, the polarizing plate or the circularly polarizing plate may be provided with an anti-reflection film. For example, anti-glare treatment by which reflected light can be diffused by projections and depressions on the surface so as to reduce the glare can be performed.

[0216]

Further, an electronic paper in which electronic ink is driven can be provided as the display device. The electronic paper is also referred to as an electrophoretic display device (an electrophoretic display) and is advantageous in that it has the same level of readability as plain paper, it has lower power consumption than other display devices, and it can be made thin and lightweight.

[0217]

An electrophoretic display device can have various modes. An electrophoretic display device contains a plurality of microcapsules dispersed in a solvent or a solute, and each microcapsule contains first particles which are positively charged and second particles which are negatively charged. By applying an electric field to the microcapsules, the particles in the microcapsules move in opposite directions to each other and only the color of the particles gathering on one side is displayed. Note that the first particles and the second particles each contain pigment and do not move without an electric field. Moreover, the first particles and the second particles have different colors (which may be colorless).

[0218]

Thus, an electrophoretic display device is a display device that utilizes a so-called dielectrophoretic effect by which a substance having a high dielectric constant

moves to a high-electric field region.

[0219]

A solution in which the above microcapsules are dispersed in a solvent is referred to as electronic ink. This electronic ink can be printed on a surface of glass, plastic, cloth, paper, or the like. Furthermore, by using a color filter or particles that have a pigment, color display can also be achieved.

[0220]

Note that the first particles and the second particles in the microcapsules may each be formed of a single material selected from a conductive material, an insulating material, a semiconductor material, a magnetic material, a liquid crystal material, a ferroelectric material, an electroluminescent material, an electrochromic material, and a magnetophoretic material, or formed of a composite material of any of these.

[0221]

As the electronic paper, a display device using a twisting ball display system can be used. The twisting ball display system refers to a method in which spherical particles each colored in black and white are arranged between a first electrode layer and a second electrode layer which are electrode layers used for a display element, and a potential difference is generated between the first electrode layer and the second electrode layer to control orientation of the spherical particles, so that display is performed.

[0222]

FIG. 12 illustrates an active matrix electronic paper as one embodiment of a semiconductor device. The electronic paper in FIG. 12 is an example of a display device using a twisting ball display system.

[0223]

Between the first electrode layer 4030 connected to the transistor 4010 and the second electrode layer 4031 provided on the second substrate 4006, spherical particles 4613 each of which includes a black region 4615a, a white region 4615b, and a cavity 4612 which is filled with liquid around the black region 4615a and the white region 4615b, are provided. A space around the spherical particles 4613 is filled with a filler 4614 such as a resin. The second electrode layer 4031 corresponds to a common electrode (counter electrode). The second electrode layer 4031 is electrically

connected to a common potential line.

[0224]

Note that in FIG. 10, FIG. 11, and FIG. 12, a flexible substrate as well as a glass substrate can be used as the first substrate 4001 and the second substrate 4006. For example, a light-transmitting plastic substrate or the like can be used. As plastic, a fiberglass-reinforced plastics (FRP) plate, a polyvinyl fluoride (PVF) film, a polyester film, or an acrylic resin film can be used. In addition, a sheet with a structure in which an aluminum foil is sandwiched between PVF films or polyester films can be used.

[0225]

An insulating layer 4021 can be formed using an inorganic insulating material or an organic insulating material. Note that the insulating layer 4021 formed using a heat-resistant organic insulating material such as an acrylic resin, a polyimide resin, a benzocyclobutene resin, a polyamide resin, or an epoxy resin is preferably used as a planarizing insulating film. Other than such organic insulating materials, it is possible to use a low-dielectric constant material (a low-k material), a siloxane-based resin, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), or the like. The insulating layer may be formed by stacking a plurality of insulating films formed of these materials.

[0226]

There is no particular limitation on the method for forming the insulating layer 4021, and the insulating layer can be formed, depending on the material, by a sputtering method, a spin coating method, a dipping method, spray coating, a droplet discharge method (e.g., an inkjet method or the like), a printing method (e.g., screen printing, offset printing, or the like), roll coating, curtain coating, knife coating, or the like.

[0227]

The display device displays an image by transmitting light from a light source or a display element. Thus, the substrates and the thin films such as insulating films and conductive films provided in the pixel portion where light is transmitted have light-transmitting properties with respect to light in the visible-light wavelength range.

[0228]

The first electrode layer 4030 and the second electrode layer 4031 (each of which may be called a pixel electrode layer, a common electrode layer, a counter

electrode layer, or the like) for applying voltage to the display element may have light-transmitting properties or light-reflecting properties, which depends on the direction in which light is extracted, the position where the electrode layer is provided, the pattern structure of the electrode layer, and the like.

[0229]

The first electrode layer 4030 and the second electrode layer 4031 can be formed using a light-transmitting conductive material such as indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium tin oxide (hereinafter referred to as ITO), indium zinc oxide, or indium tin oxide to which silicon oxide is added.

[0230]

The first electrode layer 4030 and the second electrode layer 4031 can be formed of one or more kinds of materials selected from metals such as tungsten (W), molybdenum (Mo), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), cobalt (Co), nickel (Ni), titanium (Ti), platinum (Pt), aluminum (Al), copper (Cu), and silver (Ag); alloys of these metals; and nitrides of these metals.

[0231]

A conductive composition containing a conductive high molecule (also referred to as conductive polymer) can be used for the first electrode layer 4030 and the second electrode layer 4031. As the conductive high molecule, a so-called π-electron conjugated conductive polymer can be used. For example, polyaniline or a derivative thereof, polypyrrole or a derivative thereof, polythiophene or a derivative thereof, and a copolymer of two or more of aniline, pyrrole, and thiophene or a derivative thereof can be given.

[0232]

Since the transistor is easily broken owing to static electricity or the like, a protective circuit for protecting the driver circuit is preferably provided. The protective circuit is preferably formed using a nonlinear element.

[0233]

As described above, by using any of the transistors described in Embodiment 1,

a semiconductor device having a high reliability can be provided. Note that the transistors described in Embodiment 1 can be applied to not only semiconductor devices having the display functions described above but also semiconductor devices having a variety of functions, such as a power device which is mounted on a power supply circuit, a semiconductor integrated circuit such as an LSI, and a semiconductor device having an image sensor function of reading information of an object.

[0234]

The methods and structures described in this embodiment can be combined as appropriate with any of the methods and structures described in the other embodiments.

[0235]

(Embodiment 3)

A semiconductor device disclosed in this specification and the like can be applied to a variety of electronic devices (including game machines). Examples of electronic devices are a television set (also referred to as a television or a television receiver), a monitor of a computer or the like, a camera such as a digital camera or a digital video camera, a digital photo frame, a mobile phone handset (also referred to as a mobile phone or a mobile phone device), a portable game machine, a portable information terminal, an audio reproducing device, a large-sized game machine such as a pachinko machine, and the like. Examples of electronic devices each including the liquid crystal display device described in the above embodiment are described.

[0236]

FIG. 13A illustrates a laptop personal computer, which includes a main body 3001, a housing 3002, a display portion 3003, a keyboard 3004, and the like. By applying the semiconductor device described in Embodiment 1 or 2, the laptop personal computer can have high reliability.

[0237]

FIG. 13B illustrates a personal digital assistant (PDA) including a display portion 3023, an external interface 3025, an operation button 3024, and the like in a main body 3021. A stylus 3022 is included as an accessory for operation. By applying the semiconductor device described in Embodiment 1 or 2, the portable digital assistant (PDA) can have higher reliability.

[0238]

FIG. 13C illustrates an example of an e-book reader. For example, an e-book reader 2700 includes two housings, a housing 2701 and a housing 2703. The housing 2701 and the housing 2703 are combined with a hinge 2711 so that the e-book reader 2700 can be opened and closed with the hinge 2711 as an axis. With such a structure, the e-book reader 2700 can operate like a paper book.

[0239]

A display portion 2705 and a display portion 2707 are incorporated in the housing 2701 and the housing 2703, respectively. The display portion 2705 and the display portion 2707 may display one image or different images. In the case where the display portion 2705 and the display portion 2707 display different images, for example, a display portion on the right side (the display portion 2705 in FIG. 13C) can display text and a display portion on the left side (the display portion 2707 in FIG. 13C) can display images. By applying the semiconductor device described in Embodiment 1 or 2, the electronic book reader 2700 can have high reliability.

[0240]

In FIG. 13C, the housing 2701 includes an operation portion and the like as an example. For example, the housing 2701 is provided with a power switch 2721, operation keys 2723, a speaker 2725, and the like. With the operation key 2723, pages can be turned. Note that a keyboard, a pointing device, or the like may also be provided on the surface of the housing, on which the display portion is provided. Furthermore, an external connection terminal (an earphone terminal, a USB terminal, or the like), a recording medium insertion portion, and the like may be provided on the back surface or the side surface of the housing. Moreover, the e-book reader 2700 may have a function of an electronic dictionary.

[0241]

The e-book reader 2700 may have a configuration capable of wirelessly transmitting and receiving data. Through wireless communication, desired book data or the like can be purchased and downloaded from an electronic book server.

[0242]

FIG. 13D illustrates a smartphone, which includes a housing 2800, a button 2801, a microphone 2802, a display portion 2803 provided with a touch panel, a speaker 2804, and a camera lens 2805 and functions as a mobile phone. By applying the

semiconductor device described in Embodiment 1 or 2, the smartphone can have high reliability.

[0243]

The display direction of the display portion 2803 can be changed depending on a usage pattern. Since the camera lens 2805 is provided on the same plane as the display portion 2803, videophone is possible. The speaker 2804 and the microphone 2802 can be used for operations such as video calls, sound recording, and playback without being limited to the voice call function.

[0244]

An external connection terminal 2806 can be connected to an AC adapter and various types of cables such as a USB cable, and charging and data communication with a personal computer are possible. Furthermore, a large amount of data can be stored and moved by inserting a storage medium into the external memory slot (not illustrated).

[0245]

Further, in addition to the above functions, an infrared communication function, a television reception function, or the like may be provided.

[0246]

FIG. 13E illustrates a digital video camera which includes a main body 3051, a display portion A 3057, an eyepiece 3053, an operation switch 3054, a display portion B 3055, a battery 3056, and the like. By applying the semiconductor device described in Embodiment 1 or 2, the digital video camera can have high reliability.

[0247]

FIG. 13F illustrates an example of a television set. In a television set 9600, a display portion 9603 is incorporated in a housing 9601. The display portion 9603 can display images. Here, the housing 9601 is supported by a stand 9605. By applying the semiconductor device described in Embodiment 1 or 2, the television set 9600 can have high reliability.

[0248]

The television set 9600 can be operated by an operation switch of the housing 9601 or a separate remote controller. Further, the remote controller may be provided with a display portion for displaying data output from the remote controller.

[0249]

Note that the television set 9600 is provided with a receiver, a modem, and the like. With use of the receiver, general television broadcasting can be received. Moreover, when the display device is connected to a communication network with or without wires via the modem, one-way (from a sender to a receiver) or two-way (between a sender and a receiver or between receivers) information communication can be performed.

[0250]

The methods and structures described in this embodiment can be combined as appropriate with any of the methods and structures described in the other embodiments.

[Example 1]

[0251]

In this example, results of SIMS measurement of the concentration of silicon included in an oxide target will be described.

[0252]

First, oxide targets used in this example are described.

[0253]

As Sample A, an In-Ga-Zn-based oxide target (atomic ratio: In:Ga:Zn = 2:1:3) was used. As Sample B, an In-Ga-Zn-based oxide target (atomic ratio: In:Ga:Zn = 3:1:2) was used. As Sample C, an In-Sn-Zn-based oxide (atomic ratio: In:Sn:Zn = 2:1:3) was used. In addition, as Standard Sample D, an In-Ga-Zn-based oxide target (atomic ratio: In:Ga:Zn = 1:1:1) to which silicon is added was used.

[0254]

SIMS measurement was performed on Sample A, Sample B, Sample C, and Standard Sample D, so that the concentration of silicon included in each sample was measured.

[0255]

FIG. 14 shows results of SIMS measurement of Samples A to C and Standard Sample D.

[0256]

As seen in FIG. 14, the concentration of silicon in Sample A is 4×10^{18}

atoms/cm^3, the concentration of silicon in Sample B is 3×10^{17} atoms/cm^3, the concentration of silicon in Sample C is 2×10^{17} atoms/cm^3, and the concentration of silicon in Standard Sample D is 2×10^{18} atoms/cm^3. Note that the results of SIMS measurement of Samples A to C were quantified using Standard Sample D.

[0257]

In the case where an oxide semiconductor film is deposited using any of Samples A to C and Standard Sample D, the above data can be used as a material for estimating whether silicon other than silicon in a target (e.g., silicon entered the oxide semiconductor film from an insulating film by mixing) is included in the oxide semiconductor film or not.

[0258]

For example, in the case where in an oxide semiconductor film deposited using Sample A (an oxide target where In:Ga:Zn = 2:1:3 (atomic ratio)) as a target, the concentration of silicon in the film is higher than 4×10^{18} atoms/cm^3, it is found that silicon enters the oxide semiconductor film from a portion other than the target.

[Example 2]

[0259]

The above embodiment describes that entry of an element that is a constituent element of an insulating film into an oxide semiconductor film is caused by mixing occurring in deposition of the oxide semiconductor film. However, as another cause, it can be considered that an element that is a constituent element of an insulating film diffuses into the oxide semiconductor film by heating a substrate after deposition of the oxide semiconductor film. Thus, in this example, experiment for examining whether entry of an element that is a constituent element of an insulating film into an oxide semiconductor film is caused by thermal diffusion will be described.

[0260]

For the experiment, first, three substrates (over each of the substrates, an insulating film and an oxide semiconductor film were formed) were prepared. Then, a sample which was not subjected to heat treatment (hereinafter, called Sample E), a sample which was subjected to heat treatment at 450 °C (hereinafter, called Sample F), and a sample which was subjected to heat treatment at 650 °C (hereinafter, called

Sample G) were manufactured. After that, in each sample, the concentration of silicon in the oxide semiconductor film in the vicinity of an interface with the gate insulating film was measured using a time-of-flight secondary ion mass spectrometer (ToF-SIMS).

[0261]

A structure of a sample used for ToF-SIMS measurement is illustrated in FIG. 15.

[0262]

The sample illustrated in FIG. 15 was obtained by depositing a silicon oxide film 202 over a silicon substrate 200, improving planarity of a surface with use of a chemical mechanical polishing (CMP) apparatus, depositing an IGZO film 204, and performing heat treatment.

[0263]

The silicon oxide film 202 was deposited with a sputtering apparatus. The conditions for depositing the silicon oxide film 202 were as follows: substrate temperature, 100 °C; gas flow rate, Ar/O_2 = 25 sccm/25 sccm; deposition power, 1.5 kW (RF power supply); deposition pressure, 0.4 Pa; and thickness, 300 nm. As a sputtering target, a silicon oxide target was used. Note that before the silicon oxide film 202 was formed, an oxide film formed over the surface of the silicon substrate 200 was removed using diluted hydrofluoric acid.

[0264]

The IGZO film 204 was deposited with a sputtering apparatus. The conditions for depositing the IGZO film 204 were as follows: substrate temperature, 200 °C; gas flow rate, Ar/O_2 = 30 sccm/15 sccm; deposition power, 0.5 kW (DC power supply); deposition pressure, 0.4 Pa; and thickness, 15 nm. Note that as a sputtering target, an oxide target (In:Ga:Zn = 3:1:2 (atomic ratio)) was used.

[0265]

The substrate was introduced into an electric furnace using a resistance heater or the like, and then the heat treatment was performed. The treatment conditions of Sample F were as follows: heating temperature, 450 °C; and heating time, one hour. The treatment conditions of Sample G were as follows: heating temperature, 650 °C; and heating time, one hour. Note that the heating atmosphere of both samples was a

mixed atmosphere of nitrogen and oxygen. Sample E was not subjected to heat treatment.

[0266]

Next, Samples E to G were subjected to ToF-SIMS measurement from the substrate surface side (on the IGZO film 204 side), so that the concentration of silicon in the IGZO film in the vicinity of the interface with the silicon oxide film was measured. FIG. 16 shows results thereof.

[0267]

The results shown in FIG. 16 indicates that in all the samples, the concentration of silicon in the oxide semiconductor film in the vicinity of the interface with the silicon oxide film is higher than 3×10^{17} atoms/cm^3, the value of which is the concentration of silicon included in the In-Ga-Zn-based oxide target (In:Ga:Zn = 3:1:2 (atomic ratio)) described in Example 1. Thus, it is found that silicon measured in the oxide semiconductor film in the vicinity of the interface with the silicon oxide film is not derived from the In-Ga-Zn-based oxide target.

[0268]

In addition, as seen in FIG. 16, a significant difference of the inclination of the concentration of silicon (also referred to as silicon concentration gradient) in the IGZO film in the vicinity of the interface is not observed, between the sample which was not subjected to heat treatment (Sample E) and the samples which were subjected to heat treatment (Sample F and Sample G). Thus, entry of an element that is a constituent element of the insulating film into the oxide semiconductor film is caused not by thermal diffusion but by mixing.

[Example 3]

[0269]

An experiment was conducted to examine whether entry of a constituent element of an insulating film into an oxide semiconductor film, which is caused by mixing, can be suppressed by decreasing the power for depositing the oxide semiconductor film. In this example, the experiment will be described.

[0270]

In the experiment, four samples were manufactured in the following manner:

first, insulating films were formed over substrates; four oxide semiconductor films were deposited over the respective insulating films with different power conditions (1 kW, 5 kW, 9 kW, and (1 kW + 5 kW)); and heat treatment was performed on each substrate. Then, the concentration of silicon in the oxide semiconductor film in the vicinity of an interface with a gate insulating film of each sample was measured with a ToF-SIMS method.

[0271]

FIG. 17 illustrates a structure of the sample used for ToF-SIMS measurement.

[0272]

The sample illustrated in FIG. 17 was obtained by depositing a silicon oxynitride film 302 over a substrate 300, depositing an IGZO film 304, and performing heat treatment.

[0273]

The silicon oxynitride film 302 was deposited with use of a high-density plasma CVD apparatus. The conditions for depositing the silicon oxynitride film 302 were as follows: substrate temperature, 325 °C; gas flow rate, $SiH_4/N_2O/Ar$ = 250 sccm/2500 sccm/2500 sccm; deposition power, 5 kW (four microwave power sources were used for the respective samples); deposition pressure, 30 Pa; and thickness, 100 nm. Note that the surface of the glass substrate 300 was cleaned to remove particles and the like before formation of the silicon oxynitride film 302.

[0274]

The IGZO film 304 was deposited with use of a sputtering apparatus. The conditions for depositing the IGZO film 304 were as follows: substrate temperature, 170 °C; gas flow rate, Ar/O_2 = 100 sccm/100 sccm; deposition pressure, 0.6 Pa; thickness, 35 nm; and deposition power, four conditions of 1 kW, 5 kW, 9 kW, and (1 kW + 5 kW) (an AC power source was used for each sample). Note that as a sputtering target, an oxide target (In:Ga:Zn = 1:1:1 [atomic ratio]) was used.

[0275]

Note that the above deposition power "1 kW + 5 kW" means that a power of 1 kW was used for a 5-nm-thick film deposition and then a power of 5 kW was used for a 30-nm-thick film deposition. Hereinafter, a sample in which an oxide semiconductor

film was deposited with 9 kW is referred to as Sample H, a sample in which an oxide semiconductor film was deposited with 5 kW is referred to as Sample I, a sample in which an oxide semiconductor film was deposited with 1 kW is referred to as Sample J, and a sample in which an oxide semiconductor film was deposited with (1 kW + 5 kW) is referred to as Sample K.

[0276]

The substrates were introduced into an electric furnace using a resistance heater or the like, and heat treatment was performed. The heat treatment was performed first for one hour at a temperature of 450 °C in an N_2 atmosphere, and then performed for one hour at a temperature of 650 °C in a (N_2 + O_2) atmosphere.

[0277]

Next, Sample H to Sample K were subjected to ToF-SIMS measurement from the substrate surface side (the IGZO film 304 side) to measure the silicon concentration in the IGZO film in the vicinity of an interface with the silicon oxynitride film. The results are shown in FIGS. 18A and 18B. Note that FIG. 18B shows part of FIG. 18A which is enlarged.

[0278]

From FIGS. 18A and 18B, it can be found that in all of the samples, the silicon concentration in the IGZO film in the vicinity of the interface with the silicon oxynitride film is higher than 2×10^{18} atoms/cm^3, the value of which is the silicon concentration in the In-Ga-Zn-based oxide target (In:Ga:Zn = 1:1:1 [atomic ratio]) described in Example 1. Thus, silicon measured in the IGZO film in the vicinity of the interface with the silicon oxynitride film is not derived from an In-Ga-Zn-based oxide target.

[0279]

In addition, as can be seen from FIGS. 18A and 18B, the concentration of silicon in the IGZO film in the vicinity with the interface with the silicon oxynitride film tends to decrease as the deposition power is decreased. According to the above, entry of a constituent element of the insulating film into the oxide semiconductor film, which is caused by mixing, can be suppressed by decreasing the power for depositing the oxide semiconductor film.

[0280]

Furthermore, the silicon concentrations of Sample J and Sample K are substantially the same, which indicates that entry of a constituent element of the insulating film into the oxide semiconductor film, which is caused by mixing, can be suppressed even when deposition of the oxide semiconductor film is performed with a low power in the initial stage and then the rest of deposition is performed with the increased power.

[Example 4]

[0281]

In this example, the measurement results of crystal states in oxide semiconductor films will be described. The crystal states are generated by entering an element that is a constituent element of an insulating film into the oxide semiconductor films.

[0282]

First, two substrates over which oxide semiconductor films were formed with use of targets having different compositions were prepared, and then each substrate was divided into three. After that, the substrates each of which has been divided into three were subjected to heat treatment under different conditions from each other. As a result, six samples were manufactured, in total, under different conditions. Then, a crystal state of the oxide semiconductor film in each sample was measured with X-ray diffraction (XRD).

[0283]

First, a structure of the samples used for XRD measurement is illustrated in FIG. 19A.

[0284]

The sample illustrated in FIG. 19A was obtained by depositing an IGZO film 402 with use of an IGZO (In:Ga:Zn = 1:1:1 (atomic ratio)) target to which SiO_2 was added over a substrate 400 and performing heat treatment.

[0285]

The IGZO film 402 was deposited with a sputtering apparatus. The conditions for depositing the IGZO film 402 were as follows: substrate temperature, 200 °C; deposition power, 100 W; deposition pressure, 0.4 Pa; gas flow rate, O_2 = 10 sccm;

and thickness, 100 nm. Note that as sputtering targets, a target (In:Ga:Zn = 1:1:1 (atomic ratio)) to which SiO_2 was added at 2 wt.% and a target (In:Ga:Zn = 1:1:1 (atomic ratio)) to which SiO_2 was added at 5 wt.% were used. Note that before the IGZO film 402 was deposited, the surface of the glass substrate 400 was cleaned, so that particles and the like were removed.

[0286]

Each substrate was introduced into an electric furnace using a resistance heater or the like, and then the heat treatment was performed. One of the three substrates which had been obtained by division after deposition of the IGZO film was subjected to heat treatment at 650 °C for one hour in an N_2 atmosphere, and then subjected to heat treatment at 650 °C for one hour in an O_2 atmosphere. Another of the three substrates obtained by division was subjected to heat treatment at 450 °C for one hour in an N_2 atmosphere, and then subjected to heat treatment at 450 °C for one hour in an O_2 atmosphere. Further, the other of the three substrates obtained by division was not subjected to heat treatment.

[0287]

With use of the above targets, heat treatment was performed under the above conditions, so that six kinds of samples (Samples L to Q shown in Table 1) were made.

[0288]

[Table 1]

Sample	Target	Heat Condition
L	In:Ga:Zn=1:1:1+SiO_2 (2wt%)	<<650°C, N_2 atmosphere, one hour>> + <<650°C, O_2 atmosphere, one hour>>
M	In:Ga:Zn=1:1:1+SiO_2 (2wt%)	<<450°C, N_2 atmosphere, one hour>> + <<450°C, O_2 atmosphere, one hour>>
N	In:Ga:Zn=1:1:1+SiO_2 (2wt%)	No Heat Treatment
O	In:Ga:Zn=1:1:1+SiO_2 (5wt%)	<<650°C, N_2 atmosphere, one hour>> + <<650°C, O_2 atmosphere, one hour>>

P	In:Ga:Zn=1:1:1+SiO_2 (5wt%)	<<450°C, N_2 atmosphere, one hour>> + <<450°C, O_2 atmosphere, one hour>>
Q	In:Ga:Zn=1:1:1+SiO_2 (5wt%)	No Heat Treatment

[0289]

Next, XRD measurement was performed on the IGZO films in Samples L to Q, so that a crystal state of each film was measured. Results thereof are shown in FIGS. 20A and 20B. FIG. 20A shows XRD measurement results of Samples L to N, and FIG. 20B shows XRD measurement results of Samples O to Q.

[0290]

As seen in FIG. 20A, Sample L which was subjected to heat treatment at 650 °C within the temperature range described in the above has a peak attributed to crystal at around 31° (= 2θ). On the other hand, all the samples shown in FIG. 20B has no peak attributed to crystal. According to the above results, in the IGZO film, crystallization by heat treatment is inhibited when excess silicon is included as impurities.

[0291]

Next, in order to measure the rate of silicon in an IGZO film deposited with use of a target to which silicon is added at 2wt.%, composition of elements included in the IGZO film were measured with X-ray photoelectron spectroscopy (XPS).

[0292]

Each sample used for XPS measurement has a structure in which an IGZO film 502 is deposited over a silicon substrate 500 as illustrated in FIG. 19B.

[0293]

The IGZO film 502 was deposited with a sputtering apparatus. The conditions for depositing the IGZO film 502 were as follows: substrate temperature, 200 °C; deposition power, 100 W; deposition pressure, 0.4 Pa; gas flow rate, O_2 = 10 sccm; and thickness, 15 nm. Note that as a sputtering target, a target (In:Ga:Zn = 1:1:1 (atomic ratio)) to which SiO_2 was added at 2 wt.% was used. Note that before the IGZO film 502 was deposited, an oxide film formed over the surface of the silicon

substrate 500 was removed with use of diluted hydrofluoric acid.

[0294]

By the XPS measurement, it was observed that silicon was included, at 1.1 at.%, in the IGZO film deposited with use of the target to which SiO_2 was added at 2 wt.%.

[0295]

According to the above, when impurities such as silicon enter, by mixing or the like, the oxide semiconductor film in the vicinity of the interface with the gate insulating film, crystallization of a channel formation region in the oxide semiconductor film is potentially inhibited. As a result, this example shows that it is important to reduce the concentration of silicon in the oxide semiconductor film in the vicinity of the interface with the gate insulating film.

EXPLANATION OF REFERENCE

[0296]

100: substrate, 101: gate electrode, 102: gate insulating film, 103: oxide semiconductor film, 103a: region, 103b: region, 103c: region, 105a: source electrode, 105b: drain electrode, 107: insulating film, 108: channel protective film, 109: protective insulating film, 110: transistor, 120: transistor, 130: transistor, 200: silicon substrate, 202: silicon oxide film, 204: IGZO film, 300: glass substrate, 302: silicon oxynitride film, 304: IGZO film, 400: glass substrate, 402: IGZO film, 500: silicon substrate, 502: IGZO film, 2700: e-book reader, 2701: housing, 2703: housing, 2705: display portion, 2707: display portion, 2711: hinge, 2721: power switch, 2723: operation key, 2725: speaker, 2800: housing, 2801: button, 2802: microphone, 2803: display portion, 2804: speaker, 2805: camera lens, 2806: external connection terminal, 3001: main body, 3002: housing, 3003: display portion, 3004: keyboard, 3021: main body, 3022: stylus, 3023: display portion, 3024: operation button, 3025: external interface, 3051: main body, 3053: eyepiece, 3054: operation switch, 3056: battery, 4001: substrate, 4002: pixel portion, 4003: signal line driver circuit, 4004: scan line driver circuit, 4005: sealant, 4006: substrate, 4008: liquid crystal layer, 4010: transistor, 4011: transistor, 4013: liquid crystal element, 4015: connection terminal electrode, 4016: terminal electrode, 4019: anisotropic conductive

film, 4021: insulating layer, 4030: electrode layer, 4031: electrode layer, 4032: insulating film, 4033: insulating film, 4034: insulating film, 4510: partition wall, 4511: electroluminescent layer, 4513: light-emitting element, 4514: filler, 4612: cavity, 4613: spherical particle, 4614: filler, 4615a: black region, 4615b: white region, 9600: television set, 9601: housing, 9603: display portion, 9605: stand

This application is based on Japanese Patent Application serial no. 2011-215682 filed with Japan Patent Office on September 29, 2011, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. An oxide semiconductor film in contact with an insulating film including silicon,

wherein the oxide semiconductor film includes indium and zinc, and

wherein the oxide semiconductor film includes a first region in which a concentration of silicon distributed from an interface on the insulating film side toward an inside of the oxide semiconductor film is lower than or equal to 1.0 at.%.

2. An oxide semiconductor film in contact with an insulating film including silicon,

wherein the oxide semiconductor film includes indium and zinc,

wherein the oxide semiconductor film includes a first region in which a concentration of silicon distributed from an interface on the insulating film side toward an inside of the oxide semiconductor film is lower than or equal to 1.0 at.%,

wherein the oxide semiconductor film includes a second region different from the first region, and

wherein a concentration of silicon included in the second region is lower than a concentration of silicon included in the first region.

3. An oxide semiconductor film in contact with an insulating film including silicon,

wherein the oxide semiconductor film includes indium and zinc,

wherein the oxide semiconductor film includes a first region and a second region,

wherein a concentration of silicon included in the first region is lower than or equal to 1.0 at.%, and

wherein a concentration of silicon included in the second region is lower than the concentration of silicon included in the first region.