

Claims

1. A system for analyzing targets, comprising: at least one of a metrology tool or a semiconductor process tool; and one or more processors configured to execute a plurality of computer-readable instructions, wherein the plurality of computer-readable instructions is configured to cause the one or more processors to: generate target data from at least one of a plurality of target parameters for a plurality of targets, a plurality of target metrology conditions for a plurality of metrology processes performable by the metrology tool, or a plurality of production processes performable by the semiconductor process tool; simulate one or more metrology measurements of the plurality of targets from the target data via a metrology simulation device; generate a plurality of metrics that quantify the one or more metrology measurements via the metrology simulation device; derive one or more functional dependencies of the plurality of metrics on the plurality of target parameters via a sensitivity analysis device; define one or more uncertainties of the plurality of target parameters with respect to the one or more functional dependencies via the sensitivity analysis device; coarse-filter the plurality of targets according to the simulated one or more metrology measurements to determine one or more coarse-filtered targets; rank the one or more coarse-filtered targets and the plurality of target metrology conditions with respect to the one or more metrology measurements via a target optimization device; provide data corresponding to at least one of the one or more functional dependencies, the one or more uncertainties, or the one or more rankings to the at least one of the metrology tool or the semiconductor process tool; and configure at least one of the plurality of metrology processes of the metrology tool to characterize the one or more target metrology conditions or the plurality of production processes of the semiconductor process tool to generate a semiconductor device design based on the data corresponding to at least one of the one or more functional dependencies, the one or more uncertainties, or the one or more rankings.
2. The system of claim 1, wherein the plurality of computer-readable instructions is further configured to cause the one or more processors to: generate one or more suggested changes to at least one of the plurality of target parameters via at least one of the sensitivity analysis device or the target optimization device.
3. The system of claim 1, wherein the plurality of computer-readable instructions is further configured to cause the one or more processors to: perform stack and topography verification prior to target optimization to determine one or more process parameters with a predetermined level of influence on the plurality of metrics via the sensitivity analysis device.
4. The system of claim 1, wherein the plurality of computer-readable instructions is further configured to cause the one or more processors to: eliminate insensitive process variation parameters prior to target optimization to enhance the simulation process via the sensitivity analysis device.
5. The system of claim 1, wherein the plurality of computer-readable instructions is further configured to cause the one or more processors to: provide quantitative data on an impact of process variations on metrology performance via the sensitivity analysis device.
6. The system of claim 1, wherein the plurality of computer-readable instructions is further configured to cause the one or more processors to: receive metrology data for a first metrology step via a feed forward loop; and determine one or more metrology excursions during a subsequent metrology step via the sensitivity analysis device.
7. The system of claim 1, wherein the plurality of computer-readable instructions is further configured to cause the one or more processors to: correlate one or more observed metrology metrics with a variation of a specific process parameter of the one or more process parameters via the sensitivity analysis device.
8. The system of claim 1, wherein the plurality of computer-readable instructions is further configured to cause the one or more processors to: receive at least one or more plurality of target parameters for the plurality of targets, the plurality of target metrology conditions, or the plurality of production processes from the semiconductor process tool.

9. A method, comprising: simulating one or more metrology measurements of a plurality of targets based on target data, wherein the target data is generated from at least one of a plurality of target parameters for the plurality of targets, a plurality of target metrology conditions for a plurality of metrology processes performable by a metrology tool, or a plurality of production processes performable by a semiconductor process tool; generating a plurality of metrics to quantify the one or more metrology measurements; deriving one or more functional dependencies of the plurality of metrics on the plurality of target parameters; defining one or more uncertainties of the plurality of target parameters with respect to the one or more functional dependencies; coarse-filtering the plurality of targets according to the simulated one or more metrology measurements to determine one or more coarse-filtered targets; ranking the one or more coarse-filtered targets and the plurality of target metrology conditions with respect to the one or more metrology measurements via a target optimization device; providing data corresponding to at least one of the one or more functional dependencies, the one or more uncertainties, or the one or more rankings to at least one of the metrology tool or the semiconductor process tool; and configuring at least one of the plurality of metrology processes of the metrology tool to characterize the one or more target metrology conditions or the plurality of production processes of the semiconductor process tool to generate a semiconductor device design based on the data corresponding to at least one of the one or more functional dependencies, or the one or more uncertainties, or the one or more rankings, wherein at least one of the simulating the one or more metrology measurements, the generating the plurality of metrics, the deriving the one or more functional dependencies, or the defining one or more uncertainties is carried out by at least one computer processor.

10. The method of claim 9, further comprising: eliminating insensitive process variation parameters prior to the ranking of the at least one of the plurality of targets or the plurality of target metrology conditions to enhance the simulating the one or more metrology measurements.

11. The method of claim 9, further comprising: providing quantitative data on an impact of process variations on metrology performance.

12. The method of claim 9, further comprising: correlating one or more observed metrology metrics with a variation of a specific process parameter of the one or more process parameters.

13. The method of claim 9, further comprising: generating one or more suggested changes to at least one of the plurality of target parameters.

14. The method of claim 9, further comprising: defining one or more uncertainties of the plurality of target parameters with respect to the one or more functional dependencies.

15. The method of claim 9, further comprising: receiving at least one or more plurality of target parameters for the plurality of targets, the plurality of target metrology conditions, or the plurality of production processes from the semiconductor process tool.

16. A apparatus to analyze targets, comprising: a non-transitory memory element configured to store a plurality of computer-readable instructions; and one or more processors configured to execute the plurality of computer-readable instructions, the plurality of computer-readable instructions is configured to cause the one or more processors to: simulate one or more metrology measurements of a plurality of targets based on target data, wherein the target data is generated from at least one of a plurality of target parameters for the plurality of targets, a plurality of target metrology conditions for a plurality of metrology processes performable by a metrology tool, or a plurality of production processes performable by a semiconductor process tool; generate a plurality of metrics to quantify the one or more metrology measurements; derive one or more functional dependencies of the plurality of metrics on the plurality of target parameters; define one or more uncertainties of the plurality of target parameters with respect to the one or more functional dependencies; coarse-filter the plurality of targets according to the simulated one or more metrology measurements to determine one or more coarse-filtered targets; rank the one or more coarse-filtered targets and the plurality of target metrology conditions with respect to the one or more metrology measurements via a target optimization device; provide data corresponding to at least one of the one or more functional dependencies or the one or more uncertainties to at least one of the metrology tool or the

semiconductor process tool; and configure at least one of the plurality of metrology processes of the metrology tool to characterize the plurality of target metrology conditions or the plurality of production processes of the semiconductor process tool to generate a semiconductor device design based on the data corresponding to at least one of the one or more functional dependencies, the one or more uncertainties, or the one or more rankings.

17. The apparatus of claim 16, wherein the plurality of computer-readable instructions is further configured to cause the one or more processors to: receive at least one or more plurality of target parameters for the plurality of targets, the plurality of target metrology conditions, or the plurality of production processes from the semiconductor process tool.