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Title An Improved Salicide Process Technology.

Inventors: Water Lur, Tony Lin.

Assigned To: United Microelectronics Corporation.

This application claims priority from provisional application Serial No. 60/013,641, filed March 18, 1996.

Background of the Invention.

1. Field of the Invention.

The present invention relates to semiconductor devices incorporating electrodes consisting of a layer of polysilicon covered by a self-aligned layer of metal silicide.

2. Description of the Related Art.

As line widths and geometries for semiconductor devices are made smaller, the polysilicon electrodes that form the gates of MOS devices and wiring lines within semiconductor devices become undesirably resistive. Multilayer electrodes in which a layer of polysilicon is covered by one or more layers of metals or metal silicides are used to provide electrodes having a lower resistance than electrodes consisting solely of polysilicon. Silicide electrodes may consist, for example, of a layer of polysilicon having a thickness of approximately 1000 Å to 3000 Å covered by titanium silicide to a thickness of greater than 100 Å.

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A typical implementation of such a multilayer electrode is the so-called self-aligned silicide structure, illustrated in idealized form in Figs. 1-4. Figs. 1-4 show cross-sectional views of MOS devices at an early stage of manufacture. The illustrated MOS devices are formed on a P-type substrate 10 and include thick field oxide regions 12 to provide isolation from other, adjacent MOS devices. A gate oxide layer 14, formed by thermal oxidation, covers the active device region of the illustrated device and a polysilicon gate electrode 16 is formed on the gate oxide layer 14. The polysilicon gate electrode 16 is formed by depositing a layer of undoped polysilicon over the substrate, typically using low pressure chemical vapor deposition (LPCVD), implanting and activating impurities into the polysilicon to render it conductive, and patterning the polysilicon using photolithography. Polysilicon wiring line 18 is formed on the field oxide region 12 at the same time as the gate electrode 16.

Doped source/drain regions 20 are formed on either side of the polysilicon gate electrode to define the channel region of the illustrated MOS transistor. Generally, a lightly doped drain (LDD) structure is used in small design rule MOS transistors of the type that are primarily used in modern memory and logic devices. LDD source/drain regions 20 are typically formed in a two step process, beginning with a relatively low level dopant implantation made self-aligned to a polysilicon gate electrode 16 as illustrated in Fig. 1. Subsequently, spacer oxide regions 22 (Fig. 2) are formed on either side of the gate electrode by first depositing a layer of CVD oxide over the Fig. 1 structure and then anisotropically etching back the oxide layer to expose the substrate over the source/drain regions 20. Etching back the CVD oxide layer produces the spacer oxide regions 22 on either side of the polysilicon gate electrode 16. This process also provides spacer regions 24 on either side of the polysilicon wiring line 18, if the wiring line 18 is exposed during

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the oxide deposition and etch back process. After the spacer oxide regions 22 are provided on either side of the polysilicon gate electrode 16, a second, heavier ion implantation is made into the source/drain regions 20 self-aligned to the spacer oxide regions 22 (not shown).

The structure illustrated in Fig. 2 includes a polysilicon gate electrode 16 and a polysilicon wiring line 18. For smaller line widths, even highly doped polysilicon is sufficiently resistive to diminish the performance of MOS circuits due to decreased signal levels and longer RC time constants. To reduce the resistance of these gate electrodes and wiring lines, further processing of the Fig. 2 device continues to convert the gate electrode 16 and wiring line 18 into silicide structures using self-aligned silicide (salicide) techniques. Although a variety of different silicides are known to be acceptable, the silicide most commonly used at this time is titanium silicide, and that structure is described herein. Referring now to Fig. 3, silicide lines are formed by first sputtering a layer of titanium over the surface of the device to a thickness of, for example, 500 Å. This titanium layer 26 is converted into titanium silicide at the surface of the polysilicon layers 16, 18 and at the exposed portions of the substrate, including the source/drain regions 20, in a two step process. In the first process step, the device is subjected to a rapid thermal anneal (RTA) by heating the device to a temperature of up to about 700°C for about thirty seconds, converting the titanium layer 26 into titanium silicide (nominally $TiSi_2$) where the titanium layer is in contact with a silicon (crystalline or polycrystalline) surface. The device is then etched using a wet etch consisting of H_2O_2 and NH_4OH diluted in water, removing unreacted titanium from the surface of the device, exposing the oxide regions of the device. Layers of titanium silicide 30, 32 are left over the polysilicon gate electrode 16 and over the wiring line 18. When the source/drain regions 20 are exposed during the silicidation process, titanium silicide regions 34 are also formed on the

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surface of the source/drain regions 20. Such titanium silicide regions 34 provide lower sheet resistance over the source/drain regions and provide better contacts to the source/drain regions 20. Titanium silicide contacts on the source/drain regions are thus preferred so long as the amount of silicon consumed in the silicidation process does not alter the gate performance or result in excessive junction leakage at the source/drain regions.

After the unreacted titanium is etched from the device, further processing is necessary to provide suitable self-aligned silicide (salicide) structures for the gate electrodes and wiring lines of the device. The process steps described to this point form a relatively high resistivity phase of titanium silicide on the silicon surfaces, so that the illustrated salicide structure does not have as low of resistivity as is desirable. It is accordingly necessary to expose the device to a second rapid thermal anneal at a temperature in excess of 800°C for at least ten seconds to convert the titanium silicide to the lower resistivity phase of titanium silicide. The device is then subjected to further processing to complete the fabrication.

A number of the processing steps necessary to the formation of salicide structures are critical. For example, if the temperature control is poor for the initial RTA step of converting the titanium in contact with silicon to titanium silicide, then it is possible that the temperature of the device may get high enough for rapid silicon transport laterally along the titanium layer (26 in Fig. 3), which could convert titanium to titanium silicide in undesirable regions. For example, if silicon is transported along the portion of the titanium layer extending over the oxide spacers 22 on either side of the gate electrode 16, then a "stringer" may be formed bridging between the gate electrode and the source/drain regions 20. Such a stringer 36 bridging between the gate silicide layer 30 and the source/drain silicide region 34 is illustrated in Fig. 5. The formation of the Fig. 5

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structure is obviously undesirable in that it shorts the gate to the source/drain region and renders the transistor inoperative.

For smaller device geometries, gate electrodes and wiring lines become narrower and it becomes increasingly more necessary to provide sufficiently low resistivity gate electrodes and wiring lines within memory and logic devices. On the other hand, as narrower gate electrodes and wiring lines are implemented, it is increasingly more difficult to form appropriate salicide electrode structures. In particular, it is difficult to provide the low resistivity phase of titanium silicide for narrow line width gate electrodes and wiring lines. It is accordingly desirable to develop better designs and more robust processing techniques for forming low resistance salicide structures.

Brief Description of the Drawings.

Figs. 1-4 illustrate the process steps for forming a salicide structure in accordance with conventional teachings.

Fig. 5 illustrates a stringer formed on a transistor, shorting the gate to the drain of the transistor.

Fig. 6 illustrates a difficulty in producing acceptable salicide structures.

Figs. 7-15 illustrate stages in the manufacture of MOS devices incorporating salicide structures in accordance with the present invention.

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Summary of the Preferred Embodiments.

A first aspect of the present invention provides a semiconductor circuit having a wiring line and a MOS device incorporating a gate electrode. The MOS device is formed over a semiconductor substrate. Each of the wiring line and the gate electrode have a salicide structure comprising a polysilicon lower layer having sidewalls and a layer of metal silicide overlying the polysilicon lower layer and extending laterally beyond each of the sidewalls of the polysilicon lower layer.

Another aspect of the invention provides a semiconductor circuit comprising a semiconductor substrate, a layer of insulating material on the semiconductor substrate, and a polysilicon structure on the layer of insulating material formed to have two sidewalls extending above the semiconductor substrate. A layer of conductive material is formed on the polysilicon structure extending laterally beyond both sidewalls of the polysilicon structure.

Still another aspect of the invention provides a semiconductor circuit comprising a semiconductor substrate and a layer of insulating material on the semiconductor substrate. A polysilicon structure is formed on the layer of insulating material so as to have two sidewalls extending above the semiconductor substrate. A layer of conductive material on the polysilicon structure extends laterally beyond both sidewalls of the polysilicon structure, and a first LDD source/drain region formed within the semiconductor substrate having a first lightly doped region and a first heavily doped region, the first lightly doped region having a boundary adjacent to a lower edge of a first one of the sidewalls of the polysilicon structure and the first heavily doped region having a boundary formed self aligned to a first edge of the layer of conductive material.

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A different aspect of the present invention includes a method of forming a semiconductor device including a MOS transistor, including the steps of forming an insulator on a semiconductor substrate and forming a shaped polysilicon electrode on the insulator, the shaped polysilicon electrode having protrusions extending laterally over the semiconductor substrate. The method includes the further steps of forming, by ion implantation, LDD source/drain regions within the substrate on either side of the shaped polysilicon electrode using the protrusions of the shaped polysilicon electrode as a mask for the ion implantation to define the LDD source/drain region dopant distribution, and forming a metal silicide layer over the shaped polysilicon electrode.

For a particularly preferred embodiment of this aspect of the invention, the step of forming the shaped polysilicon electrode structure includes the steps of depositing a first layer of masking material on the semiconductor device and a second layer of masking material on the first layer of masking material and forming an opening by removing a portion of the first and the second layers of masking material. The second layer of masking material is etched laterally so that the opening is wider at the second layer than at the first layer. Polysilicon is deposited within the opening and the first and second layers of masking material are removed.

Still another aspect of the invention provides a method of making a semiconductor device by providing a semiconductor substrate and providing a layer of insulating material over at least a portion of the semiconductor substrate. A shaped polysilicon structure is formed over the layer of insulating material, the shaped polysilicon structure having protrusions extending laterally over a surface of the semiconductor substrate. A metal layer is deposited on the shaped polysilicon structure and the semiconductor device is annealed to produce a layer of metal silicide on the shaped polysilicon structure.

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Detailed Description of the Preferred Embodiments.

Preferred embodiments of the present invention form semiconductor devices incorporating salicide (self-aligned silicide) structures in a process that preferably does not form oxide spacer structures alongside the polysilicon gate electrodes and wiring lines. Rather, a shaped polysilicon gate electrode is formed having an upper surface that can be converted to a silicide such as titanium silicide. The shaped polysilicon electrode preferably includes protrusions that extend away from the body of the electrode and extend over the silicon substrate. The polysilicon gate electrode may, for example, have a cross section in the shape of a "t". By first performing low dopant level ion implantation at an angle to reach the substrate regions shadowed by the protrusions from the gate electrode, an appropriate light ion implantation can be made for the source/drain regions. A subsequent, high dopant level ion implantation is made using an implantation direction perpendicular to the surface of the substrate so that the protrusions extending from the gate electrode act as a mask for the high dopant level ion implantation that completes the source/drain structure. In this way, a lightly doped drain (LDD) type structure can be formed for both of the source/drain regions without using spacer oxide regions. Gate electrodes and wiring lines having this structure are more consistently of a higher quality, and generally have lower resistance than gate electrodes and wiring lines formed using conventional salicide techniques.

The present inventors believe that the observed improvements in salicide electrode and wiring line formation and performance achieved by using preferred embodiments of the present invention relate to forming the salicide structure so that the silicide layer of the gate electrode is grown in such a manner as to have a low level of stress. It becomes increasingly difficult to form

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acceptable low resistivity salicide electrodes and wiring lines when these structures are made using polysilicon lines that are less than one half micron across In particular, the resistivity of gate electrodes and wiring lines rises precipitously for line widths of less than one half micron. The increase in the resistivity for smaller line widths reflects the fact that the second annealing step conventionally used to produce the low resistivity phase of silicide can be ineffective for such narrow line widths. To understand why this happens, it is useful to consider a more realistic model of what happens during the formation of conventional salicide structures.

Fig. 6 illustrates a mechanism that is believed to explain the difficulty in converting silicide layers formed on narrow line width polysilicon layers to the low resistivity silicide phase. Fig. 4, discussed above, shows a well defined titanium silicide layer extending uniformly across a polysilicon gate electrode. This is an idealized representation of what is produced during the rapid thermal anneal that converts titanium in contact with a layer of silicon into a layer of titanium silicide. The inventors have observed that this process step more typically forms a titanium silicide structure 38 such as that illustrated in Fig. 6. Near the edge of the polysilicon gate electrode, the gate oxide spacers 22 appear to "clamp" the edges of the titanium silicide layer 38, limiting the growth of the titanium silicide layer which typically must expand to a thickness greater than the silicon layer consumed during the growth process. Thus, titanium silicide grows most freely near the center of the gate electrode so that the thickest part of the titanium silicide layer 38 is formed above the center of the polysilicon gate electrode 16. Titanium silicide along the edges of the layer 38 has a high level of stress, as it is formed, while the more central portion of the titanium silicide has a relatively lower level of stress. If the width of the titanium silicide layer 38 is sufficiently small, then a considerable level of stress will exist even at the center of the

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titanium silicide layer 38. If too high of a stress level exists across the entire titanium silicide layer as it is formed, then a subsequent annealing step may not be successful in converting enough of the titanium silicide layer 38 to the low resistivity phase. A salicide structure in which the as grown silicide layer has too high of a level of stress may thus produce an undesirably resistive salicide structure which is poorly suited for use as a gate electrode or a wiring line.

The present inventors accordingly believe that, at least for small line widths, it is desirable to form salicide structures using silicide layers having a reduced stress level. Salicide structures that are formed incorporating a reduced stress silicide layer and a preferred method of making such structures are now described with reference to Figs. 7-15. While these figures illustrate particularly preferred embodiments of the present invention within MOS transistors and wiring lines in a particular configuration of a semiconductor device, embodiments of the present invention can be used to form gate electrodes and wiring lines in a wide variety of semiconductor devices. In addition, while the description of the following embodiments emphasizes the formation of NMOS devices, salicide structures in accordance with the present invention may be implemented to advantage in PMOS devices as well. This is true whether the polysilicon of the PMOS gate is doped N-type or P-type. Although it is possible to use the salicide structure described herein only for the gate electrodes (or, conversely, only for the wiring lines) of a device, it is presently believed that it is most desirable to use the described salicide structure for all of the first level polysilicon lines, at least for those devices in which high conductivity electrodes and wiring lines are desirable.

Fig. 7 illustrates in cross section a small portion of a semiconductor circuit incorporating a MOS device at an early stage in the manufacturing process. A P-type substrate 10 is provided

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and device isolation regions such as field oxide regions 12 are provided as necessary. A pad oxide 40 is grown thermally or deposited by chemical vapor deposition (CVD) over the active device regions of the device to a thickness of between about 50 to 300 Å. The channel threshold adjust implantation is then performed in the typical manner using, for example, boron or boron fluoride ions for NMOS devices or, for example, arsenic or phosphorus ions for PMOS devices to a dose of between about 3×10^{11} ions/cm^2 to about 5×10^{13} ions/cm^2 at an energy of between about 5 to 50 KeV. Next, a series of layers of material are deposited at least over the regions of the device where salicide gate structures and wiring lines are to be formed. The series of layers will be patterned into a form or mask structure to be used in forming a shaped polysilicon line which will undergo further processing to form a salicide structure. As such, it is possible to use a variety of different combinations of layers to provide the desired form or mask structure. In a preferred embodiment, a layer 42 of silicon nitride Si_3N_4 is deposited first, a layer 44 of silicon oxide SiO_2 is deposited next, and then a second layer 46 of silicon nitride is deposited. Each of these layers can be deposited using one of the conventional CVD processes well known in the art, with each of the layers having a thickness of between about 1000 Å to 3000 Å. The total thickness of the layers is preferably about 3000 Å, but this may be readily varied to form salicide structures of different thicknesses.

After the layers 42, 44, 46 that will be formed into the polysilicon form have been deposited, photolithography is performed to provide openings through the three layers at the regions where salicide structures are to be formed. This photolithography may use a mask that is the reverse of the conventional first polysilicon mask pattern so that, after the photoresist is exposed and removed, openings through the photoresist will leave the layer 46 exposed over the

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regions where the salicide structures are to be formed. Then, the layers 42, 44 and 46 are etched in a substantially anisotropic manner using, for example, plasma etching with SF_6 and He for the Si_3N_4 layers 46 and 42 and using CHF_3 and O_2 for the SiO_2 layer 44. After the photoresist is stripped, the device will appear as shown in Fig. 8 with an opening 48 over the illustrated active device region and an opening 50 on top of the field oxide region 12. A lateral etch of the middle SiO_2 layer 44 is then performed by dipping the device in a dilute HF solution (*e.g.*, $HF:H_2O$ = 1:10) for between about two to about seven minutes. This will result in an undercut 52 being formed laterally across layer 44 within opening 48 and an undercut 54 being formed across layer 44 within opening 50. The undercut etch will also result in the removal of the pad oxide 40 where it is exposed to the dilute HF solution, as well as a slight undercut beneath layer 42. The extent of the undercut of layer 44 determines how far polysilicon protrusions will overhang the substrate for the shaped polysilicon structure that is to be formed. Accordingly, as will be described in greater detail below, the extent of the undercut will establish the position of the edge of the heavily doped portion of the LDD source/drain regions of the device. Thus, the extent of the undercut may desirably be adjusted in accordance with the particular structure that is desired for the source/drain regions. The presently preferred extent of the undercuts 52, 54 is between about 500 Å to about 2000 Å.

After the undercut etching has been performed, the substrate 10 will be exposed within the opening 48. A gate oxide layer 56 (Fig. 10) is then thermally grown in the conventional manner to a thickness of between about 30 Å to about 300 Å. Polysilicon is deposited by CVD to a sufficient depth to extend above the first layer 42 and more preferably to extend above layer 44. The thickness of the polysilicon layer will typically be about the thickness of the three layers 42,

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44 and 46. CVD polysilicon will readily deposit within the undercut regions 52, 54 (Fig 9) to form shaped polysilicon structures 58, 60 as shown in Fig. 10. The polysilicon structures are preferably doped *in situ* during deposition by the addition of the appropriate dopant gas during the CVD process, or the polysilicon structures may alternately be doped later by ion implantation The stack of layers 42, 44, 46 is then removed using conventional etchants, such as hot H_3PO_4 for the Si_3N_4 layer 46 and 42 and a dilute HF (in H_2O) solution for the SiO_2 layer 44, to provide the structure shown in Fig. 11.

Next, the anti-punchthrough implantations are formed and the lightly doped portions of the source/drain regions are formed. These implantations are made in a self-aligned manner using the protrusions 62 extending from the polysilicon electrode 58 as a mask during oblique angle ion implantation. The implantation angles are readily determined by the length by which the protrusions 62 extend over the surface of the substrate 10 and the angle necessary for the implantation to have "line of sight" to the base of the polysilicon electrode 58. Typically, the implantation angle will be between about 15° to about 60°. The anti-punchthrough implantations 64 and lightly doped drain implantations 66 are made in the well known manner using implantations of boron, boron fluoride, arsenic or phosphorus ions to a dose of between about 5 x 10^{12} ions/cm^2 to about 2 x 10^{14} ions/cm^2 at an energy of between about 5 to 80 KeV. The resulting structure is illustrated in Fig. 12.

The heavily doped portions of the source/drain regions are then formed by implantation perpendicular to the surface of the substrate (*i.e.*, no tilt angle), using the protrusions 62 extending from the polysilicon electrode 58 as a mask for the heavy implantation. Because the edge of heavily doped region is determined by where the "shadows" of the protrusions 62 fall on

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the substrate, the heavily doped regions (68, Fig. 13) are formed self-aligned to the protrusions. Typically, the heavily doped regions are formed by an implantation of boron, boron fluoride, arsenic, antimony or phosphorus ions to a dose of between about 1 x 10^{14} ions/cm^2 to about 1 x 10^{16} ions/cm^2 at an energy of between about 5 to 200 KeV. The source/drain regions are then activated by heating the device to a temperature of between about 800°C to 1100°C for between 10 seconds (RTA, higher temperature) and 60 minutes (lower temperature).

Next, the silicide portion of the salicide structure is formed. As is known in the art, acceptable silicide layers can be formed using a number of different base metals, including titanium, cobalt, nickel, platinum and palladium. At the present time, titanium silicide is the most widely implemented, but both cobalt and nickel silicides are believed to have desirable characteristics for reduced line width devices. The processing steps characteristic to each of these different silicides are well known and reported in the literature. Accordingly, while the following description is made in terms of titanium silicide, other silicides can also be utilized in this process, as is known in the art.

After thermal activation of the dopants, the device is as illustrated in Fig. 13. The native (thermal) oxide formed in this process is removed using a dilute HF solution, and then a thin layer of the metal to be silicided is deposited over the device using physical vapor deposition (*e.g.*, sputtering). In the illustrated embodiment, titanium is deposited to a thickness of between about 200 Å to 800 Å, producing thin layers 70 over the surface of the device, as shown in Fig. 14. The thickness of metal to be deposited is determined by balancing the need to deposit sufficient titanium to form a uniform layer with sufficient metal to provide a desirably conductive titanium silicide layer against the need to leave sufficient silicon below the silicided structures. Excessive

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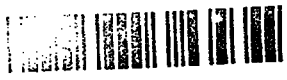
silicon consumption during silicidation can lead to unacceptable junction leakage from the source/drain regions, among other problems. As is illustrated in Fig. 14, there is poor metal coverage in the region where the substrate is shadowed by the protrusions 62 from the polysilicon electrode 58.

The discontinuities in the metal layer 70 adjacent the gate electrode ensure that bridging (such as that illustrated in Fig. 5) should not occur. Thus, it is possible to perform the initial silicidation at a temperature sufficiently high to produce the low resistivity phase of titanium silicide. Accordingly, titanium silicide could be formed by performing a rapid thermal anneal (RTA) of the Fig. 14 device at a temperature of about 750°C for about twenty seconds. A subsequent etch would remove the unreacted titanium. In this process, however, there may be considerable silicon transport along the titanium layer 70, which could result in titanium silicide stringers extending over portions of the device in an undesirable fashion. It is therefore still likely preferred that silicidation be performed in a two-step process. Regardless, the existence of the discontinuities in the sputtered titanium layer reduce the criticality of the temperature and other controls for the processing steps in the two-step annealing process. Preferably, the Fig. 14 structure is subjected to a first RTA at a temperature within the range of 600-750°C, more preferably of about 700°C, for 10 to 120 seconds, more preferably 20 to 60 seconds, in a nitrogen ambient. For cobalt silicide, a temperature of about 550-600°C is preferably used for the initial silicidation step. Titanium nitride, titanium-rich titanium silicide, titanium oxide and unreacted titanium are then etched from the surface of the device in a solution of NH_4OH, H_2O_2 and H_2O (for example, at a ratio of 1:1:5), leaving titanium silicide layers 72 over the heavily doped portions 68 of the source/drain regions. Titanium silicide regions 74, 76 also remain over the

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polysilicon portion 58 of the gate electrode and over the polysilicon portion 60 of the wiring line. The remaining titanium silicide is then converted to the lower resistivity phase in a RTA at a temperature within a range of about 700°C to 900°C for between about 10 to 60 seconds. Most preferably, the second RTA is performed at a temperature of about 850°C for about 20 seconds.

In this embodiment, the titanium silicide regions 74, 76 are less constrained than in the conventional salicide process. Ideally, the titanium silicide will be essentially unconstrained in the vertical direction, since there are no spacer oxide regions to vertically compress the titanium silicide in the regions where the silicon is consumed. The titanium silicide regions 74, 76 are thus formed with much lower stress levels than occur in the conventional silicidation process (illustrated in Figs. 1-4). There will still be stress introduced into the titanium silicide layer along the horizontal direction due to the mismatch between the titanium silicide and the underlying (unconsumed) silicon, but the structure should nevertheless have a much reduced stress level after the initial silicidation process than in conventional salicide processes. As such, the second RTA has a much improved likelihood of converting the titanium silicide to the preferred low resistivity phase. The titanium silicide structures 74, 76 have approximately the same width (*i.e.*, approximately 500 Å to approximately 2000Å) as the silicon protrusions 62 that exist prior to the silicidation process.

Subsequent processing proceeds in the conventional manner, with the deposition of a interpolysilicon or pre-metal dielectric layer such as atmospheric pressure CVD SiO_2 or borophosphosilicate glass (BPSG) over the Fig. 15 structure. Thus, CVD SiO_2 or BPSG will typically be disposed adjacent the lower sidewalls of the polysilicon electrode 58 (between the protrusions of silicide layer 74 and the substrate 10) and adjacent the lower sidewalls of

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polysilicon wiring line 60 (between the protrusions of silicide layer 76 and the field oxide 12). Vias are formed through the CVD SiO_2 or BPSG down to the silicide regions as necessary, forming polysilicon or metal contacts and first metal or second polysilicon wiring lines and interconnects. The remaining structures and processes are conventional and so are not described further herein. It should be noted that certain configurations of gate electrodes, wiring lines and silicided regions of the substrates sometimes include additional layers of conductive materials such as refractory metals or nitrides of metals (*e.g.*, titanium nitride) formed on top of the salicide structure.

The present invention has been described in terms of certain preferred embodiments. The invention is not, however, limited to the specific embodiments described, but also includes such modifications and variations as fall within the scope of the following claims.

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What is claimed:

1. A semiconductor circuit comprising:

a semiconductor substrate;

a layer of insulating material on the semiconductor substrate;

a polysilicon structure on the layer of insulating material formed to have two sidewalls extending above the semiconductor substrate; and

a layer of conductive material on the polysilicon structure extending laterally beyond both sidewalls of the polysilicon structure.

2. The semiconductor circuit of claim 1, wherein the layer of conductive material is a metal silicide.

3. The semiconductor circuit of claim 2, wherein the metal silicide comprises silicon and at least one metal from the group consisting of titanium, cobalt, nickel, platinum and palladium.

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4. A semiconductor circuit comprising:

a semiconductor substrate;

a layer of insulating material on the semiconductor substrate;

a polysilicon structure on the layer of insulating material formed to have two sidewalls extending above the semiconductor substrate;

a layer of conductive material on the polysilicon structure extending laterally beyond both sidewalls of the polysilicon structure; and

a first LDD source/drain region formed within the semiconductor substrate having a first lightly doped region and a first heavily doped region, the first lightly doped region having a boundary adjacent to a lower edge of a first one of the sidewalls of the polysilicon structure and the first heavily doped region having a boundary formed self aligned to a first edge of the layer of conductive material.

5. The semiconductor circuit of claim 4, wherein the layer of conductive material is a metal silicide.

6. The semiconductor circuit of claim 5, wherein the metal silicide comprises silicon and at least one metal from the group consisting of titanium, cobalt, nickel, platinum and palladium.

7. The semiconductor circuit of claim 6, wherein the metal silicide is in a phase having a lower resistivity than other phases of the metal silicide.

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8. The semiconductor circuit of claim 5, wherein the layer of conductive material is titanium silicide.

9. The semiconductor circuit of claim 5, further comprising a second LDD source/drain region formed within the semiconductor substrate having a second lightly doped region and a second heavily doped region, the second lightly doped region having a boundary adjacent to a lower edge of the second of the sidewalls of the polysilicon structure and the second heavily doped region having a boundary formed self aligned to a second edge of the layer of conductive material.

10. A semiconductor circuit having a wiring line and a MOS device incorporating a gate electrode, the MOS device formed over a semiconductor substrate, the wiring line and the gate electrode each having a salicide structure comprising:

a polysilicon lower layer having sidewalls;

a layer of metal silicide overlying the polysilicon lower layer and extending laterally beyond each of the sidewalls of the polysilicon lower layer.

11. The semiconductor circuit of claim 10, wherein the layer of metal silicide extends laterally at least 500 Å beyond the upper edge of each of the sidewalls of the polysilicon lower layer.

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12. The semiconductor circuit of claim 11, wherein the MOS device further comprises a first and a second LDD source/drain region formed within the semiconductor substrate on either side of the gate electrode, each of the first and second LDD source/drain regions having a lightly doped region and a heavily doped region, each of the lightly doped regions having a boundary adjacent to a lower edge of the sidewalls of the polysilicon lower layer and each of the heavily doped regions having a boundary formed self aligned to an edge of the layer of metal silicide.

13. The semiconductor circuit of claim 12, wherein the metal silicide comprises titanium, cobalt or nickel.

14. A method of making a semiconductor device, comprising the steps of:

providing a semiconductor substrate and providing a layer of insulating material over at least a portion of the semiconductor substrate;

forming a shaped polysilicon structure over the layer of insulating material, the shaped polysilicon structure having protrusions extending laterally over a surface of the semiconductor substrate;

depositing a metal layer on the shaped polysilicon structure; and

annealing the semiconductor device to produce a layer of metal silicide on the shaped polysilicon structure.

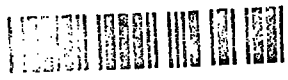
15. The method of claim 14, wherein the metal layer is deposited by physical vapor deposition.

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16. The method of claim 14, wherein the metal layer is deposited in such a manner that there is a discontinuity in the deposited metal layer at or near the protrusions of the polysilicon structure.

17. The method of claim 14, wherein the step of annealing the semiconductor device consists of a rapid thermal anneal performed at a temperature within the range of 600°C to 750°C.

18. The method of claim 17, wherein the rapid thermal anneal is performed at a temperature of about 700°C.

19. The method of claim 17, wherein the rapid thermal anneal continues for a time between 10 to 120 seconds.

20. The method of claim 18, wherein the rapid thermal anneal continues for 20 to 60 seconds.

21. The method of claim 14, further comprising the step of etching the device in a solution of NH_4OH, H_2O_2 and H_2O subsequent to the step of annealing the semiconductor device.

22. The method of claim 21, further comprising a second step of annealing the semiconductor device at a temperature of about 850°C for about 20 seconds.

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23. The method of claim 14, further comprising a second step of annealing the semiconductor device at a temperature of greater than 700°C for about 10 to about 120 seconds.

24. A method of forming a semiconductor device including a MOS transistor, the method of making the MOS transistor comprising the steps of:

forming an insulator on a semiconductor substrate;

forming a shaped polysilicon electrode on the insulator, the shaped polysilicon electrode having protrusions extending laterally over the semiconductor substrate;

forming by ion implantation LDD source/drain regions within the substrate on either side of the shaped polysilicon electrode using the protrusions of the shaped polysilicon electrode as a mask for the ion implantation to define the LDD source/drain region dopant distribution; and

forming a metal silicide layer over the shaped polysilicon electrode.

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25. The method of claim 24, wherein the step of forming the shaped polysilicon electrode structure comprises the steps of:

depositing a first layer of masking material on the semiconductor device and a second layer of masking material on the first layer of masking material;

forming an opening by removing a portion of the first and the second layers of masking material;

laterally etching the second layer of masking material so that the opening is wider at the second layer than at the first layer;

depositing polysilicon within the opening; and

removing the first and second layers of masking material.

26. The method of claim 25, further comprising the step of depositing a third layer of masking material on the second layer of masking material before the step of forming an opening.

27. The method of claim 26, wherein the first and third layers of masking material are formed of the same material.

28. The method of claim 27, wherein the second layer of masking material comprises silicon oxide.

29. The method of claim 26, wherein the polysilicon is deposited by chemical vapor deposition and is doped *in situ*.

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30. The method of claim 24, wherein the step of forming a metal silicide layer comprises the steps of:

depositing a layer of metal on the semiconductor device;

annealing the semiconductor device to form metal silicide on the shaped polysilicon electrode; and

etching unreacted metal from the semiconductor device.

31. The method of claim 30, wherein the deposited metal is selected from the group consisting of titanium, cobalt, nickel, platinum and palladium.