IN THE CLAIMS

What is claimed is:

1. A method comprising;

forming a cavity in a carrier material, wherein the carrier material comprises a top layer and a bottom layer separated by an etch stop layer;

attaching a die in the cavity;

forming a dielectric material adjacent the die and on the carrier material bottom layer;

forming a coreless substrate by building up layers on the dielectric material; and

removing the carrier material top layer and etch stop layer from the bottom layer of the carrier material.

2. The method of claim 1 further comprising wherein the bottom layer of the carrier material remains attached to the coreless substrate.

3. The method of claim 2 further comprising wherein the bottom layer of the carrier material comprises at least one of a heat spreader, an EMI shield structure, and a stiffener.

4. The method of claim 3 further comprising wherein the stiffener comprises a copper ring around the die.

5. The method of claim 1 further comprising removing the carrier material top layer and etch stop layer while they are disposed on the coreless substrate.

6. The method of claim 4 further comprising wherein the stiffener is attached to the substrate with no adhesive.

7. The method of claim 1 further comprising wherein the carrier material

comprises copper.

8. The method of claim 1 further comprising wherein the coreless substrate comprises a portion of a coreless, bumpless, build up layer package.

9. A method comprising;

attaching a die to a carrier material, wherein the carrier material comprises a top layer and a bottom layer separated by an etch stop layer;

forming a dielectric material adjacent the die and on the bottom layer of the carrier material;

forming die pad interconnect structures in the die area;

forming vias in a non-die area to connect with the bottom layer carrier material;

forming a coreless substrate by building up layers on the dielectric material; and

removing the top layer carrier material and etch stop layer from the bottom layer carrier material.

10. The method of claim 9 further comprising patterning the bottom layer carrier material to form at least one of an inductor and a PoP land structure.

11. The method of claim 9 further comprising wherein the bottom layer carrier material is attached to the coreless package without an adhesive.

12. The method of claim 9 wherein the coreless substrate comprises a portion of a coreless, bumpless, build up layer package.

13. The method of claim 10 further comprising wherein a top surface of the PoP land structure is coplanar with a top surface of the coreless bumpless buildup package

14. A structure comprising:

a die embedded in a coreless substrate;

a dielectric material adjacent the die;

die pad interconnect structures disposed in a die pad area of the die; and

at least one functionalized carrier structure disposed within the coreless substrate, wherein a top surface of the at least one functionalized carrier structure is coplanar with a top surface of the coreless substrate.

15. The structure of claim 14 wherein the at least one functionalized structure comprises a copper material.

16. The structure of claim 14 wherein the coreless substrate comprises a portion of a coreless bumpless buildup package structure.

17. The structure of claim 14 wherein the at least one functionalized carrier structure comprises at least one of a stiffener, a heat spreader and an EMI shield.

18. The structure of claim 14 wherein the functionalized carrier structure is attached to the coreless package without an adhesive.

19. The structure of claim 18 wherein functionalized carrier structure comprises copper.

20. The structure of claim 16 wherein the die is coplanar with a top surface of the functionalized carrier structure, and wherein the die is fully embedded in the coreless substrate.

21. A structure comprising:

a die embedded in a coreless substrate;

a dielectric material adjacent the die;

die pad interconnect structures disposed in a die pad area of the die;

vias in the coreless substrate disposed in a non-die area that are connected to a functionalized carrier structure, wherein the functionalized carrier structure is disposed within the coreless substrate, and wherein a top

surface of the functionalized carrier structure is coplanar with a top surface of the coreless substrate.

22. The structure of claim 21 wherein the functionalized carrier structure comprises a copper material.

23. The structure of claim 21 wherein the coreless substrate comprises a portion of a coreless bumpless buildup package structure.

24. The structure of claim 21 wherein the functionalized carrier structure comprises at least one of an inductor and a PoP land structure.

25. The structure of claim 24 wherein a top surface of the PoP land structure is coplanar with a top surface of the coreless bumpless buildup package.

26. The structure of claim 25 wherein the coreless bumpless buildup package does not comprise an interposer.

27. The structure of claim 24 wherein the at least one inductor comprises at least one spiral inductor adjacent the die, wherein a top surface of the at least one spiral inductor is coplanar with a top surface of the die.

28. The structure of claim 21 further comprising a system comprising:
a bus is communicatively coupled to the structure; and
a DRAM communicatively coupled to the bus.

29. The structure of claim 21 wherein the die is coplanar with a top surface of the functionalized carrier structure, and wherein the die is fully embedded in the coreless substrate.

30. The structure of claim 21 wherein the functionalized carrier structure is attached to the coreless package without an adhesive.

What is claimed is:

1. A method comprising;

forming a cavity in a carrier material, wherein the carrier material comprises a top layer and a bottom layer separated by an etch stop layer;

attaching a die in the cavity;

forming a dielectric material adjacent the die and on the carrier material bottom layer;

forming a coreless substrate by building up layers on the dielectric material; and

removing the carrier material top layer and etch stop layer from the bottom layer of the carrier material.

2. The method of claim 1 further comprising wherein the bottom layer of the carrier material remains attached to the coreless substrate.

3. The method of claim 2 further comprising wherein the bottom layer of the carrier material comprises at least one of a heat spreader, an EMI shield structure, and a stiffener.

4. The method of claim 3 further comprising wherein the stiffener comprises a copper ring around the die.

5. The method of claim 1 further comprising removing the carrier material top layer and etch stop layer while they are disposed on the coreless substrate.

6. The method of claim 4 further comprising wherein the stiffener is attached to the substrate with no adhesive.

7. The method of claim 1 further comprising wherein the carrier material comprises copper.

8. The method of claim 1 further comprising wherein the coreless substrate comprises a portion of a coreless, bumpless, build up layer package.

9. A structure comprising:

a die embedded in a coreless substrate;

the coreless substrate including a dielectric material adjacent the die;

die pad interconnect structures disposed in a die pad area of the die; and

at least one functionalized carrier structure disposed within the coreless substrate, wherein a top surface of the at least one functionalized carrier structure is coplanar with a top surface of the coreless substrate and a back side of the microelectronic die.

10. The structure of claim 9 wherein the at least one functionalized carrier structure comprises a copper material.

11. The structure of claim 9 wherein the coreless substrate comprises a portion of a coreless bumpless buildup package structure.

12. The structure of claim 9 wherein the at least one functionalized carrier structure comprises at least one of a stiffener, a heat spreader and an EMI shield.

13. The structure of claim 9 wherein the functionalized carrier structure is attached to the coreless package without an adhesive.

14. The structure of claim 13 wherein the functionalized carrier structure comprises copper.

15. The structure of claim 11 wherein the die is fully embedded in the coreless substrate.