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ABSTRACT

A test system using direct digital synthesis for generation of a spectrally pure, agile clock. The clock is used in analog and digital instruments in automatic test system. A DDS circuit is synchronized to the tester system clock because it is
5 clocked by a DDS clock generated from the system clock. Accumulated phase error is reduced through the use of a parallel accumulator that tracks accumulated phase relative to the system clock. At coincidence points, the accumulated phase in the DDS accumulator is reset to the value in the system accumulator.