communication link 114, e.g., a cable. Moreover, the SDD module 104 includes a 60 MHz PSPI, which is connected to a PSPI of a 60 MHz RF generator 116 via a communication link 118, e.g., a cable. A cable that connects one PSPI to another PSPI may communicate signals using a protocol, e.g., an RS-232 protocol, a Universal Serial Bus (USB) protocol, etc.

[0028] The RF generators 108, 112, and 116 are connected to an impedance (Z) matching circuit 120. For example, the RF generator 108 is connected to the impedance matching circuit 120 via a communication medium 122, e.g., cable, etc., the RF generator 112 is connected to the impedance matching circuit 120 via a communication medium 124, and the RF generator ~~126~~ 116 is connected to the impedance matching circuit 120 via a communication medium 126.

[0029] In some embodiments, an impedance matching circuit matches an impedance of a load connected to the impedance matching circuit with an impedance of a source, also connected to the impedance matching circuit. For example, the impedance matching circuit 120 matches an impedance of a plasma chamber 128 that is connected to the impedance matching circuit 120 via an RF transmission line 130 with impedances of the RF generators 108, 112, and 116. In several embodiments, the impedance matching circuit 120 includes electrical components, e.g., capacitors, inductors, etc., to match impedances. In various embodiments, an RF transmission line includes an RF tunnel that is connected to an RF strap, which is connected to an RF rod.

[0030] The PSPIs of the SDD module 104 sends power set points, e.g., power, etc., and frequency set points, frequencies, etc., to the PSPIs of the RF generators 108, 112, and 116 via the links 110, 114, and 118. For example, the 2 MHz PSPI of the SDD module 104 sends a power set point and a frequency set point via the link 110 to the PSPI of the RF generator 108, the 27 MHz PSPI of the SDD module 104 sends a power set point and a frequency set point via the link 114 to the PSPI of the RF generator 112, and the 60 MHz

the PSPI 203, an SS signal is sent via the communication channel C7. When the PSPI 203 is selected, a set point may be sent to the PSPI 203 and/or read back from the PSPI 203 is performed. As another example, to select a semiconductor chip on which the RF controller 204 and the PSPI 205 are implemented, a SS signal is sent via a communication channel C16 from a 27 MHz SS port of the PSPI 212 to a 27 MHz SS port of the PSPI ~~203~~ 205. Moreover, to select a semiconductor chip on which the RF controller 206 and the PSPI 207 are implemented, a SS signal is sent via a communication channel C25 from a 60 MHz SS port of the PSPI 214 to a ~~27~~ 60 MHz SS port of the PSPI 207.

[0052] A clock signal is sent from an RF Control (Ctrl)-CLK port of the PSPI 210 via a communication channel C8 to an RF Ctrl-CLK port of the PSPI 203. Also, a ground signal, e.g., a reference signal, a zero voltage signal, etc., is communicated between an RF Ctrl-Ground (GND) port of the PSPI 210 and an RF Ctrl-GND port of the PSPI 203. The ground signal establishes a reference for all signals, except for a clock signal, communicated between the VMAP controller 208 and the PSPIs 203, 205, and 207.

[0053] Similarly, signals similar to that communicated between the PSPI 210 and the PSPI 203 are communicated between the PSPI 212 and the PSPI 205 via communication channels C10 thru C18. Moreover, signals similar to that communicated between the PSPI 210 and the PSPI 203 are communicated between the PSPI 214 and the PSPI 207 via communication channels C19 thru C27. In several embodiments, the communication channels C1 thru C9 are included within a cable, e.g., an RS-232 cable, etc., the communication channels C10 thru C18 are included within another cable, e.g., an RS-232 cable, etc., and the communication channels C19 thru C27 are includes within yet another cable, e.g., an RS-232 cable, etc.

[0054] Moreover, a TTL signal is sent from a TTL Output port of the RF controller 206 to a TTL input port of the VMAP controller 208. It should be noted that the

back serial data in port, the port HP4 is a frequency read back serial data in port, the port HP5 is a real portion of load impedance serial data in port, the port HP6 is an imaginary portion of load impedance serial data in port, the port HP7 is a slave select signal port, the port HP8 is a clock signal port, and the port HP9 is a ground signal port.

[0069] In various embodiments, the port GP1 is a power set point serial data in port, the port GP2 is a frequency set point serial data in port, the port GP3 is a power read back serial data out port, the port GP4 is a frequency read back serial data out port, the port GP5 is a real portion of load impedance serial data out port, the port GP6 is an imaginary portion of load impedance serial data out port, the port GP7 is a slave select signal port, the port GP8 is a clock signal port, and the port GP9 is a ground signal port.

[0070] The port HP1 sends a power component setting, e.g., a power magnitude, etc., to the port GP1. Moreover, the port HP2 sends a frequency component setting, e.g., a frequency, etc., to the port GP2. Moreover, the ports HP2 thru HP6 receive, e.g., read back, access, etc., four distinct variables, VR1 thru VR4, that change over time. For example, complex load impedance, complex V&I, complex voltage, complex current, complex power, complex gamma, etc., have a positive frequency. As another example, in practicality, frequency is not a constant. For example, a frequency has a standard deviation, a variance, etc., that changes the frequency over time. In some embodiments, a frequency is maintained constant.

[0071] The port GP3 sends a power read back value, e.g., a power magnitude, etc., to the port HP3. Moreover, the port GP4 sends a frequency read back value, e.g., a frequency, etc., to the host system 102.

[0072] The PSPI of the host system 102 includes a sampler circuit ~~254~~ 256. The sampler circuit ~~254~~ 256 is integrated with the host system 102, e.g., is configured within an integrated circuit of the host system102. In several embodiments, each port that samples a

signal includes a sampler circuit. For example, the port HP3 includes a sampler circuit, the port HP4 includes a sampler circuit, the port HP5 includes a sampler circuit, and the port HP6 includes a sampler circuit, the port GP1 includes a sampler circuit, and the port GP2 includes a sampler circuit.

[0073] The sampler circuit ~~254~~ 256 samples signals received, e.g., the variables VR1 thru VR4, etc., at the ports HP3 thru HP6 at selected clock edges, e.g., rising clock edges, falling clock edges, etc. The sampler circuit ~~254~~ 256 samples the signals to capture operating state data, e.g., frequency, load impedance, the variables V1 thru V4, complex voltage, complex current, complex V&I, of the plasma chamber 128 (Figure 1) and of the RF generator 108, 112, and/or 116 (Figure 1) . The operating state data of the plasma chamber 128 is detected, e.g., measured, sensed, etc., by a sensor, e.g., a voltage and current sensor, a voltage sensor, a current sensor, a power sensor, etc., of an RF generator that includes the RF generator controller 252. In some embodiments, the operating state data, e.g., complex gamma, complex delivered power, etc., of the plasma chamber 128 is determined by a DSP of the RF generator that includes the RF controller 252. In various embodiments, the operating state data of an RF generator includes frequency, power, etc., set by the RF generator. It should be noted that the host system 102 provides a set point, e.g., a frequency set point, a power set point, etc. to an RF generator. When the RF generator receives a set point, the RF generator sets power and/or frequency based on the set point. For example, the RF generator looks up a set point in a storage device of the RF generator to determine an associated, e.g., linked, etc., drive power and/or frequency with the set point. The set power and/or frequency, e.g., the drive power and/or frequency, etc., is provided to a drive of the RF generator to generate an RF signal having the power and/or frequency.

[0074] In embodiments in which five variables are transferred over communication channels between the host system 102 and the RF controller 252, an example of the five variables include frequency, complex forward power, and complex reflected

any other integrated circuit, e.g., ASIC, etc., may be used. Moreover, instead of the microprocessor 404, any other integrated circuit, e.g., FPGA, ASIC, etc., may be used.

[0092] The FPGA 402 includes a multiple SPI (MSPI) 406, which is also referred to herein as a PSPI. The MSPI 406 includes 27 pins, which includes 9 pins each for a PSPI. For example, the MSPI 406 includes the PSPI 210, the PSPI 212, and the PSPI 214 (Figure 2A). The MSPI 406 receives data, e.g., power read back from an SDO port, frequency read back from an SDO port, real portion of load impedance read back from an SDO port, imaginary portion of load impedance read back from an SDO port, variables, etc., from the PSPIs 203, 205, and 206 (Figure 3A), and sends the data to a soft-core DSP 408 and/or to a high-speed port 410.

[0093] The soft-core DSP 408 includes an RF transmission model, which is a computer-generated model of the RF transmission line 130 (Figure 1). For example, the FPGA 402 implements an electrical circuit that includes elements, which are electrical components, e.g., capacitors, inductors, etc., of the RF transmission line 130. To illustrate, when the RF transmission line 130 includes an inductor having an inductance of L Henry and a capacitor having a capacitance of C Farad, the soft-core DSP 408 includes an inductor having an inductance of L Henry and a capacitor having a capacitance of C Farad. Moreover, the FPGA 402 connects the elements within the electrical circuit in the same manner, e.g., serial, parallel, etc., as that in which the electrical components are connected. For example, when an inductor is connected in parallel with a capacitor within the RF transmission line 130, the soft-core DSP 408 includes an inductor ~~connector~~ connected in parallel with ~~an inductor~~ a capacitor.

[0094] In some embodiments, instead of the RF transmission model, an impedance matching model or a combination of the impedance matching model and the RF transmission model are included within the soft-core DSP 408. The impedance matching model is implemented within the FPGA 402 based on the impedance matching circuit 120

(Figure 1) in a similar manner as that of generating the RF transmission model from the RF transmission line 130.

[0095] The variables received by the MSPI 406 are sent from the MSPI 406 via the high-speed port 410 and a high-speed bus 412 to a high-speed ~~bus~~ port 415 ~~412~~ of the microprocessor 404. Examples of a high-speed bus include a bus that transfers data at 500 MHz, at 400 MHz, at 300 MHz, at 600 MHz, between 5 MHz and 500 MHz, etc. The variables are communicated via the high-speed port 415 to an SDD logic block 416. A logic block is a computer program that is executed by one or more processors, e.g., the SDD logic block 416 is executed by the microprocessor 404. In several embodiments, a logic block is implemented within an integrated circuit.

[0096] The SDD logic block 416 applies a statistical transformation over a time window, e.g., 2 microseconds, 10 seconds, 5 seconds, 5 microseconds, etc., to variables received via the high-speed port 415 to generate statistical data. For example, the SDD logic block 416 generates a mean, rolling variance, median, mode, standard deviation, maximum, minimum, interquartile range (IQR), etc., from variables received via the high-speed port 415 to generate statistical data. To illustrate, the SDD logic block 416 generates a mean of multiple values of power received via the communication channel C10. In this illustration, the multiple values of power are received over a time window of ten microseconds. As another illustration, the SDD logic block 416 generates a median of multiple values of real portion of load impedance received via the communication channel C5. In this illustration, the multiple values of load impedance are received over a time window of five microseconds.

[0097] As another illustration, a first weight is assigned to a first variance of a first variable value, e.g., power magnitude, phase, etc., received in a first time window. In this example, a second weight is assigned to a second variance of a second variable value received within the first time window, and so on until an Nth weight is assigned to an Nth

Tx/Rx (Figure 1), etc., to one or more devices, e.g., the RF generator 108, the RF generator 112, the RF generator 116, a remote computer system, etc. Examples of the remote computer system include a computer, a server, a processor, a cell phone, a smart phone, a tablet, etc., which is operated by a user. The user views the indication on a display device, e.g., a cathode ray tube display, a liquid crystal display device, a light emitting diode display device, a plasma display device, etc., of the remote computer system and may decide to take action to resolve the fault.

[00102] Figure 4B is a block diagram of an embodiment of a host system 450, which is another example of the host system 102 (Figure 1). The host system 450 is similar to the host system 400 (Figure 4A) except that the host system 450 includes a microprocessor 452. The microprocessor 452 is similar to the microprocessor 404 (Figure 4A) except that the microprocessor 452 includes a variable module 454.

[00103] The variable module 454 receives the RF transmission model via the high-speed port 410, the high-speed bus 412, and the high-speed port 415, and receives the variables, e.g., load impedance, complex V&I, complex voltage, complex current, etc., from the MSPI 406 via the high-speed port 410, the high-speed bus 412, and the high-speed port 415. The variable module 454 determines variables, e.g., complex V&I, complex voltage, wafer bias, ion energy, plasma potential, complex current, load impedance, etc., at an output of the soft-core DSP 408 based on variables received from the MSPI 406 and characteristics, e.g., capacitance, impedance, etc., of the RF transmission model. For example, when load impedance received via the communication channels C5 and C6 (Figure 2A) is Z1 and an impedance of elements of the RF transmission model is Z2, the variable module 454 determines an impedance at an output of the RF transmission model to be a directional sum of Z1 and Z2. As another example, when a complex V&I received via three communication channels is complex V&I1 and a complex V&I of the RF transmission model is complex

2A), etc. The user views the indication on the display device of the remote computer system and may decide to take action to resolve the fault.

[00106] Figure 5 is a diagram of embodiments of graphs 502, 504, and 506 used to illustrate that the variables help in determining an event, e.g., unconfinement of plasma within the plasma chamber 128 (Figure 1). Examples of other events include arcing, change in load impedance, change in health of plasma chamber 128, etc.

[00107] The graph 502 plots a wafer bias, which is bias at the ESC, versus time. The graph 502 includes a plot 508 of wafer bias determined based on a model, e.g., the RF transmission model, the impedance matching model, etc. Moreover, the graph 502 includes a plot 510 of wafer bias measured by a sensor. It should be noted that a potential plasma unconfinement is visible in the graph 502 at points of discontinuity within plots 508 and 510.

[00108] The graph 504 plots a root mean square (RMS) voltage determined at an output of a model versus time when the 2 MHz RF generator 108 (Figure 1) is operational, e.g., powered on, etc., and the remaining RF generators, e.g., the 27 MHz RF generator 112 (Figure 1), the 60 MHz RF generator 116 (Figure 1), etc., are nonoperational, e.g., powered off. It is visible in the graph 504 from a discontinuity in a plot 505 that there is a potential plasma unconfinement.

[00109] The graph 506 plots a magnitude of impedance at the output of the soft-core DSP 408 (Figure 4A), plots a magnitude, e.g., root mean square, etc., of complex current, and plots a magnitude of power versus time. The graph 506 includes a plot 512, which plots the magnitude of impedance at the output of the soft-core DSP 408 versus time. The graph 506 further includes a plot 514, which plots the magnitude of complex current determined at an output of the soft-core DSP 408versus time. Moreover, the graph ~~508~~ 506 includes a plot 516, which plots the magnitude of power determined at an output of the soft-core DSP 408versus time. Based on a change in three RF parameters, e.g., a decrease in the

19. A plasma system comprising:

a host system for providing data signals;

a radio frequency (RF) generator coupled to the host system, the RF generator for generating an RF signal based on the data signals;

an impedance matching circuit for matching an impedance of the RF generator with an impedance of a plasma chamber;

an RF transmission line coupling the impedance matching circuit to the plasma chamber;

a bus interface connecting the host system to the RF generator, the bus interface including:

a first set of host ports, the first set of host ports used to provide a power component setting and a frequency component setting to the RF generator, and the first set of host ports used to receive distinct variables that change over time;

a second set of generator ports used to send a power read back value and a frequency read back value to the host system; and

a sampler circuit integrated with the host system, the sampler circuit configured to sample signals at the ports of the first set at selected clock edges to capture operating state data of the plasma chamber and the RF generator.

20. The plasma system of claim 19, wherein the signals sampled at the ports of the first set are resampled a set number of times to capture a full parallel data set.

21. The plasma system of claim 19, wherein the signals sampled at a clock edge are less than a full parallel data set.