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(71) Applicant *(for all designated States except US)*: **LAM RESEARCH CORPORATION** [US/US]; 4650 Cushing Parkway, CA-1, Fremont, CA 94538 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **ANNAPRAGADA, Rao** [IN/US]; 34268 Pinnacles Drive, Union City, CA 94587 (US). **ZHU, Helen** [US/US]; 300 Tiffany Terace, Fremont, CA 94536 (US).

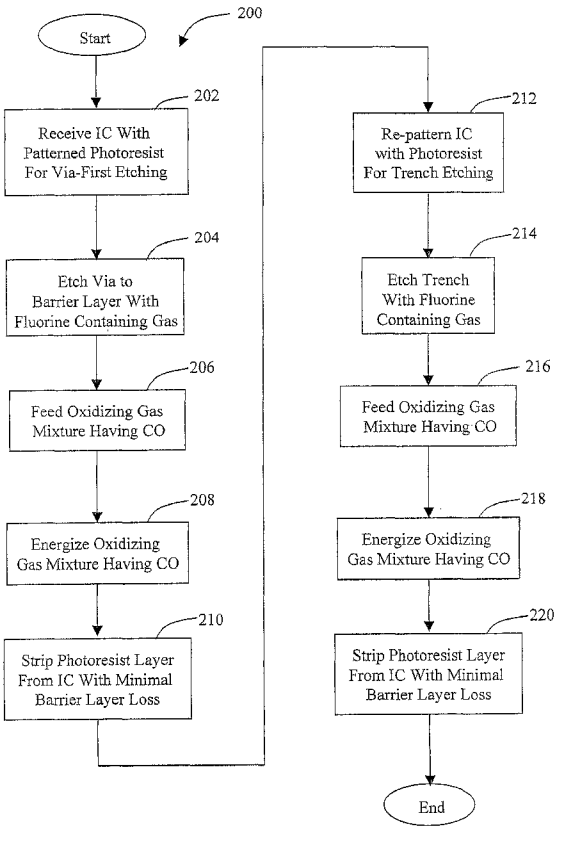
(74) Agent: **KERR, Michael, A.**; Virtual Legal, P.C., 777 E. William St., Ste. 211, Carson City, NV 89701 (US).

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(54) Title: MINIMIZING THE LOSS OF BARRIER MATERIALS DURING PHOTORESIST STRIPPING



(57) Abstract: A method of removing a photoresist layer from an integrated circuit (IC) structure having an etched dielectric material with an exposed barrier layer that covers a copper interconnect. The barrier layer is composed of a material such as silicon 5 nitride or silicon carbide. The method includes feeding a gas mixture that compromises carbon monoxide (CO) into a reactor. A plasma is then generated within the reactor. The photoresist layer is then selectively removed with little or no etching of the exposed barrier layer.

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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)*

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