

HIGH PERFORMANCE SUB-SYSTEM DESIGN AND ASSEMBLY

Abstract of the Disclosure

A multiple integrated circuit chip structure provides interchip communication between integrated circuit chips of the structure with no ESD protection circuits and no input/output circuitry. The interchip communication is between internal circuits of the integrated circuit chips. The multiple integrated circuit chip structure has an interchip interface circuit to selectively connect internal circuits of the integrated circuits to test interface circuits having ESD protection circuits and input/output circuitry designed to communicate with external test systems during test and burn-in procedures. The multiple interconnected integrated circuit chip structure has a first integrated circuit chip mounted a second integrated circuit chip to physically and electrically connect the first integrated circuit chip to the second integrated circuit chip. The first integrated circuit chip has interchip interface circuits connected to the second integrated circuit chip to selectively communicate between internal circuits of the first and second integrated circuit chips or test interface circuits connected to the internal circuits of the first integrated circuit chip to provide stimulus and response to said internal circuits during testing procedures. The second integrated circuit chip has input/output interface circuitry to communicate with external circuitry connected to the second integrated circuit chip and to protect said second integrated circuit chip from electrostatic discharge voltages. Further, the second integrated circuit has interchip interface circuits connected to the first integrated circuit chip to communicate between the internal circuits of the first and second integrated circuit chips.

(Fig. 3)