This Sheet Has Been Replaced



AN INTEGRATED CIRCUIT DEVICE HAVING A PLANAR INTERLEVEL DIELECTRIC LAYER

Abstract

An integrated circuit includes a conductive layer adjacent a semiconductor substrate. The conductive layer includes conductive lines having gaps therebetween. A fluoro-silicate glass (FSG) layer is over the patterned conductive layer fills the gaps between conductive lines. Also, an undoped oxide layer is on the FSG layer. Peaks of the FSG layer which overlie the conductive metal lines have been reduced by CMP. Thus, a subsequent conductive layer is substantially protected from exposure to fluorine from the FSG layer.