Literal Translation

Apparatus and method for recognising genuine electronic IC cards

The invention relates to an apparatus for recognising genuine electronic IC cards in card readers in accordance with the preamble of claim 1, and a method for recognising the genuineness of electronic IC cards in card readers in accordance with the preamble of claim 7.

Such apparatuses and methods are suitable for card readers which carry out identification in unmonitored access control machines and which apportion a service in sales apparatuses of all types such as telephones, gas, water and electricity meters, televisions ("pay TV"), ATMs, snack and food dispensers and so forth, and make possible the recognition of false electronic IC cards which are inserted in the card reader fraudulently, in order to dishonestly obtain access or services.

In general cards made from a piece of plastics with an integrated circuit are designated as IC cards and mostly have the dimensions set out in ISO norm 7816-1 (85.4 mm x 54 mm, with a thickness of 0.76 mm). They are used in everyday payment transactions and also used as identity cards of all kinds. The IC cards carry designations such as "smart card", electronic cash cards, pre-paid cards for services, identity and service cards and so forth, depending on the capabilities of the integrated circuit. In "How 'Smart' Can We Get" by Mike Arnavutian, in British Telecommunications Engineering, Vol. 15, Jan. 1997, in addition to a brief summary of the different types of IC cards and their use, the number of IC cards manufactured and sold is indicated, wherein pre-paid memory cards for paying for telephone calls, for parking fees and so forth are by far the most frequently used.

IC cards are divided into two main groups, one group has the known contact field, by means of which a card reader makes direct electrical contact with the integrated circuit of the IC card, and the other group establishes a high-frequency connection with the card reader by means of integrated antennae. IC cards are already known which can effect exchange of data both via electrical contacts and via a high-

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frequency connection.

The IC cards represent cash values and it is thus attractive to unauthorised persons to imitate such cards. A first generation of attempts at fraud was based on the idea of imitating the operating mode of the integrated circuits using a mini-computer, wherein the mini-computer located outside the card reader is connected via supply lines to the contact fields of a defective IC card. The IC card prepared in this way is inserted into the card reader instead of a genuine IC card, and makes the connection from the mini-computer to the electronic circuit of the card reader. Card readers are protected from this type of fraud with apparatuses such as described in EP-A 468'848 and EP-A 561'124. The apparatuses have special probes for sensing the signals radiated by these supply lines. As soon as the probes receive such signals, the data exchange between the IC card and the card reader is interrupted. Other apparatuses have a flap at their entrance which must first close completely before the data exchange is received at all, such as known from German Utility Patent DE-U 89'07699.0 or EP-A 468'146. In DE-A 39'16'812, the flap is configured as a blade, which simply cuts such supply lines.

Card readers protected in this way are defrauded to an increasing extent by imitative autonomous IC cards, which contain integrated electronic circuits in the body of the card, and fake the original IC card circuit with a programmed microcomputer.

The object of the invention is to provide a cost effective apparatus for card readers and to disclose a method which can differentiate genuine IC cards from imitation cards, and rejects the imitation cards.

The objects described are solved according to the invention by the features of claim 1 and of claim 7. Advantageous configurations will be evident from the dependent claims.

Hereinafter embodiments of the invention will be explained in more detail with

reference to the drawings.

In these is shown, in:

Figure 1: a card reader,
Figure 2: a first measuring means,
Figure 3: a first time diagram for synchronous data exchange,
Figure 4: a second measuring means,
Figure 5: a second time diagram for synchronous data exchange, and
Figure 6: the time diagram for asynchronous data exchange.

In Figure 1, 1 designates a card reader, 2 an IC card with an electronic IC card circuit, 3, 4 means for data exchange between the card reader 1 and the IC card 2, 5 a coupling means for data transfer, 6 a control module of the card reader 1 for controlling data exchange, for storing data and for transmission of data and commands to an apparatus 7 arranged outside the card reader 1. The IC card circuit 3 is connected via the coupling means 5 to the means for data exchange 4 from and to the IC card circuit 3 and to the control module 6 of the card reader 1. The data exchange means 4 measure a time delay Δt between an input signal E for the IC card 2 and a response signal A given out by the IC card 2 as a response to the card reader 1. The measured values of the time delay Δt are compared with permissible limit values for the IC card, and must be within these limits so that the card 2 is recognised as genuine and authorised for further data exchange. When there is a negative comparison result, the card reader 1 rejects the IC card as being false.

The data exchange with commands from the card reader 1 to the IC card circuit 3 and with responses from the IC card 2 to the card reader 1 is done via a data path 8 which is configured as a bi-directional data path 8 as shown in Figure 1. Other configurations of the IC cards 2 have separate data lines for the responses and for the commands.

The IC cards 2 also differ in the type of data exchange, that is to say asynchronous and synchronous data exchange. In both cases, a pulse generator 10 generates the pulse sequence T in the control module 6, which synchronises the IC card circuit 3 with the data exchange means 4. When there is asynchronous data exchange between the IC card 2 and the card reader 1, the pulse sequence T has a predetermined fixed pulse frequency on the data path 8. At any time, the data appear on the data path 8 at a Baud rate which is obtained from the pulse sequence T by scaling. According to the report by Mike Arnavutian described in the introduction, the pulse sequence T prescribed for asynchronous IC cards has a frequency f of approximately 3.57 MHz, while the data exchange takes place at 9,600 Baud.

The most frequently used embodiment of the IC card 2 uses a synchronous bi-directional data transfer, wherein between the card reader 1 and the IC card 2 data are exchanged, that is to say the commands and the responses, on the data path 8 in synchronism with the pulse sequence T of the pulse path 9, and the data are indeed sent during a command phase to the IC card 2, and during one of the command phases subsequent response phases are received from the IC card 2. For each period of the pulse sequence T, a bit of the command or of the response is transferred.

The coupling means 5 of the card reader 1 is configured according to the embodiment of the IC cards 2 to be used. With a first embodiment of the card reader 1, an IC card 2 is inserted into a card receiving bay 11, wherein direct contacting of a contact field on the IC card 2 by the coupling means 5 is done such that connections are made to the card reader 1 for the data path 8 and the pulse path 9 as well as for the lines of a power supply of the IC card 2 and a reset signal to the IC card circuit 3, not shown here. The IC cards suitable for this have, for example, the contact field set out according to ISO norm 7816-2. If, on the other hand, data transfer is to be carried out without contact, the coupling means 5 is provided at least with antennae for the data path 8. The IC cards 2 designed for data exchange without contact have an antenna means in the body of the card, so the

data exchange with the card reader 1 can take place by means of electromagnetic high frequency radiation.

The data exchange means 4 include a measuring means 12, which comprises at least a measuring circuit 13, a computing unit 14, a limit value memory 15 and a signal switch 16. Two inputs of the measuring circuit 13 are connected to the data path 8 and to the pulse path 9. The measuring circuit 13 determines delays Δt between an input signal E sent to the IC card circuit 3 on the pulse path 9 and a response signal A transmitted by the IC card 2 as a response to the card reader 1 on the data path 8. An output of the measuring circuit 13 transfers the measured values of the time delay Δt to the computing unit 14, where the measured values are compared to limit values or limit value ranges from the limit value memory 15. If the measured values exceed the permissible limit value or values, or if they are outside the permissible limit value ranges, the computing unit 14 generates an alarm signal on a signal line 17 leading to the signal switch 16. The signal switch 16 interrupts data exchange with the IC card 2 when the alarm signal is received. The signal switch 16 is shown purely symbolically as an interruptor, in reality the signal line leads to the control module 6, which, after receiving the alarm signal interrupts data exchange with the IC card 2. An IC card 2 triggering an alarm signal is removed by the card reader 1 from the card receiving bay 11 and returned to the user or else is retained (that is to say confiscated). The data traffic monitored by the measuring circuit is preferably the first command and response phases in which the card must identify itself. The functions of the data exchange means 4 and of the control module 6 can also be undertaken by a programmed microprocessor or an integrated and hard-wired fast logic circuit (ASIC).

For example, a first embodiment of the measuring circuit 13 in Figure 2 has two edge detectors 18 and 19 registering a falling edge, a start-stop counter 20 and an oscillator 22 controlled by a quartz control crystal for generating a pulse sequence Z representing a time unit. Time cycles of the pulse sequence Z are conducted via a line to the time cycle input 23 of the start-stop counter 20. An input of the first

edge detector 18 is connected to the pulse path 9. Each falling edge of the pulse sequence T, that is to say of the input signal E, triggers a square-wave pulse in the first edge detector 18 as the start signal which, via a supply line, reaches a start signal input 24 of the start-stop counter 20. The bi-directional data path 8 is connected to an input of the second edge detector 19. Each falling edge of the response signal A triggers a square-wave pulse in the second edge detector 19 as a stop signal which reaches, via a supply line, a stop signal input 25 of the start-stop counter 20. When the start signal is received, the start-stop counter 20 begins to count the time cycles of the pulse sequence Z arriving at the time cycle input 23 as time units, until the stop signal interrupts the counting procedure. The total of time units counted between the start signal and the stop signal in the start-stop counter 20 is the measured value of the delay Δt. A measured value line 26 transfers the measured value, for example, parallel to a measured value input 27 of the computer unit 14, where the measured value is taken over by an interrupt signal I for further processing. Lastly, the counter status of the start-stop counter 20 is returned to zero by means of a reset signal R transmitted to the reset input 28 of the start-stop counter 20. A reset circuit 29 generates the reset signal R which is conducted from the output of the reset circuit 29 to the reset input 28. The two inputs of the reset circuit 29 are connected to the data path 8 and the pulse path 9.

As only the response signal A is of importance for the monitoring of the genuineness of an IC card, during the response phase an enable signal F can be sent by the control module 6 (Figure 1) via an enable line 31 to an input of an interrupt circuit 32 of the measuring circuit 13. If the data appear on the data path 8 during the command phase with delays compared with the pulse sequence T, which are smaller than with the response signal A, the enable signal F is superfluous. The two other inputs of the interrupt circuit 32 are connected to the data path 8 and the pulse path 9. An interrupt signal I generated at an output of the interrupt circuit 32 is supplied to an interrupt line 33 which transfers the interrupt signal I to an interrupt input 34 of the computer unit 14.

The computer unit 14 compares the measured values of the delay Δt with the predetermined permissible limits stored in the limit value memory 15 and supplies the alarm signal via the signal line 17 if the measured values do not satisfy the criteria for a genuine IC card 2 (Figure 1).

In Figure 3 diagrams of the signals A, I, R and T as a function of the time t for the measuring circuit 13 are shown, and the mode of operation of the measuring circuit 13 (Figure 2) is explained. The example shown of the response signal A firstly transfers a logic value "0", then the logic values "1, 0, 0, 1, 0" and so forth follow. The delay Δt is measured during the transfer of the logic values "0". The first measured value t_1 extends from the first falling edge of the pulse signal T to the first falling edge of the response signal A. The measured value t_1 stored in the start-stop counter 20 (Figure 2) is taken up from the computer unit 14 (Figure 2) during the interrupt signal I, that is to say here in the time interval in which the response signal is at logical zero and the pulse sequence T and the enable signal F are at logical one. The reset signal R for resetting the counter status in the start-stop counter 20 is done in time intervals in which both the response signal A and the pulse sequence T are at logical one. If a value "1" is transferred with the response signal A, the start-stop counter 20 counts from the falling edge of the pulse signal T, until the reset signal R is active. As the interrupt criterion (response signal A at logical zero and the pulse sequence T and optionally the enable signal F at logical one) for an interrupt signal I is not satisfied, no interrupt signal I is generated and the counter status of the start-stop counter 20 is not taken up by the computing unit 14.

In Figure 4 the circuit modules of a second embodiment of the measuring circuit 13 are synchronised with the clock pulses of the pulse sequence Z of the oscillator 22. This embodiment allows measurement of time delays Δt which exceed a half-period of the pulse sequence T. A clock pulse line 25 connects the clock pulse input 23 to pulse inputs of the two edge detectors 18 and 19 and the interrupt circuit 32. The pulse generator 10 is a scaling circuit with M steps, the counting input of which can be connected via a pulse line 36 to the clock pulse input 23 for receiving pulse

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signals of the pulse sequence Z. In another embodiment, the scaling circuit of the pulse generator 10 receives the pulse signals from the control module 6 (Figure 1). The pulse generator 10 scales down the pulse signals 2^M times, and gives out the pulse sequence T with a frequency 2^M times lower to an output connected to the pulse path 9. Each period of the pulse sequence T consequently includes 2^M clock pulses of the pulse sequence Z, wherein in the case of an exemplary pulse duty factor of 1:1, during the first $2^{(M-1)}$ pulses in each period the signal of the pulse sequence T is at logical "0" and during the second $2^{(M-1)}$ clock pulses of the period the signal is at logical "1". Pulse duty factors deviating from this, with a longer phase in which the signal is at logical "0", increase the measuring period following the falling edge of the pulse sequence T. The pulse generator 10 itself generates the reset signal R instead of the reset circuit 29 (Figure 2). A second output of the pulse generator 10 is thus connected to the reset input 28 via the reset line 30, which, for example, conducts the (2^M-2)th pulse of each period 37 (Figure 5) of the pulse sequence T as the reset signal R from the pulse generator 10 to the reset input 28.

The edge detector 18 and respectively 19 (synchronous one-shot type) gives, at its output, the start signal to the start signal input 24 and respectively the stop signal to the stop signal input 25 during a pulse which directly follows a falling edge of the signal on the pulse path 9 and respectively the data path 8.

The interrupt circuit 32 is, for example, a shift register with S steps, wherein S = 1, 2, 3, ... can be set. The input is connected to the stop signal input 25. The stop signal is taken up and stored in the shift register of the interrupt circuit 32. After S clock pulses the stop signal appears at the output of the interrupt circuit 32 and is supplied as an interrupt signal I via the interrupt line 33 to the interrupt input 34 of the computing unit 14. If the enable signal F is to be taken into account, the enable signal F is coupled to the stop signal by means of a logical AND function and the result of the AND function instead of the stop signal is taken up in the shift register of the interrupt circuit 32.

Figure 5 shows a time diagram of the signals T, A, I and R for the measuring circuit 13 of Figure 4. The interrupt signal I always appears S pulses after the falling edge of the response signal A and the reset signal R shortly before the end of period 37.

The frequency f_T of the pulse sequence T is nevertheless not essential to the invention per se, indeed, it need not even be constant. For example, the frequency f_T lies in the 10 kHz to 250 kHz range. However, the frequency f_o of the oscillator 22 (Figure 4) determines the accuracy with which the delay Δt is detected. Typical delays Δt of genuine IC cards 2 (Figure 1) have values of less than 400 ns, while the autonomous cards, even when very well programmed, differ considerably from the genuine ones, with values of delays Δt in the $1\mu s$ to $2\mu s$ range. The frequency f_o of the oscillator 22 should thus be selected to be at least 2.5 MHz. With a permissible limit value range of $0 < G < 600$ ns, the computing unit 14 (Figure 2) can differentiate the genuine IC cards from the autonomous cards. The permissible limit value range G can also have a lower limit $\neq 0$.

With each response signal A, which contains several bytes, for example, N logical values "0" are transferred, so the computer unit 14 takes on a sequence of N measured values t_1, t_2, t_3.....t_N. The computer unit 14 compares every measured value with the pre-determined permissible limit value range G from the limit value memory 15 (Figure 2). If at least one of the N measured values t_1, t_2, t_3.....t_N lies outside the permissible limit value range G, the computer unit 14 generates the alarm signal.

The card reader 1 (Figure 1) with the means for data exchange 4 described has the advantage that with the measuring circuit 13 it can differentiate the genuine IC cards 2 from the autonomous cards copied by unauthorised persons, which have circuits completely integrated into the body of the card, and imitate ("emulate") the original IC card circuit 3 using a programmed microcomputer, and reject them.

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A refinement of the method is in that the computer unit 14 applies statistical criteria to the sequence of measured values t_1, t_2, t_3.....t_N, and compares the statistical parameters thus calculated with the pre-determined permissible limit values P. The parameters of the arithmetic mean $<\Delta t>$ and the standard deviation p, for example, form a simple statistical criterion.

$$<\Delta t> = (\Sigma t_n)/N, \quad \text{for } n = 1 \text{ to } N \qquad (1)$$

$$p^2 = \Sigma(t_n)^2 - (\Sigma t_n)/N, \quad \text{for } n = 1 \text{ to } N. \qquad (2)$$

The formulae given are suitable for time-saving calculation of $<\Delta t>$ or respectively p^2, which can be done after each measurement of the delay t_n. At least one of the two parameters is calculated and subsequently used for comparison with the corresponding permissible limit values P_M and P_P. If one of the two parameters $<\Delta t>$ or respectively p^2 exceeds the assigned limit value P_M or respectively P_P, the computer unit 14 generates the alarm signal. In order that a sequence of measured values useable for static evaluation occurs, a value of $f_o \geq 10$ MHz is to be provided for the frequency f_o of the oscillator, as the resolution capability of the measuring circuit is then at least 100 ns. The parameters $<\Delta t>$ or respectively p^2 established on the genuine IC cards are below the permissible limit values P_M of 500 ns, and respectively P_P of 500 ns^2.

The genuine IC cards 2 which have fast logic circuits with hard wiring in the IC card circuit, give the response signal A with a smaller delay Δt compared to the pulse sequence T and an almost normally distributed sequence of the measured values t_N to the data line 8. However, in its microcomputer, in several program steps, initially the autonomous card must firstly recognise a change in the logical state in the pulse sequence T and then generate and transmit to the data line 8 the next bit of the pre-determined response signal A according to a programmed procedure. As the number of program steps necessary for this depends on the bit sequence in the response signal A, the successive measured values t_N of the delays Δt occurring with an autonomous card differ considerably and thus do not form a

normally distributed sequence of measured values t_N. Using the calculated statistical parameter $<\Delta t>$ or respectively p^2, autonomous cards can be differentiated, which on average differ only slightly from the genuine IC cards 2.

The card reader 1, which examines the genuineness of the IC card 2 with the aid of the statistical criteria has an advantage, in that the protection against fraud also rejects cards with a microcomputer significantly faster than those currently available.

As data must be exchanged with a specific IC card circuit 3 (Figure 1) according to the use of the card reader 1, the limit values P_M and P_P or/and limit value ranges G of the IC circuit 3 have to be correspondingly selected.

For the sake of completeness, it is also mentioned that a simple, analog time measurement can sort the autonomous cards currently known. The measuring circuit 13 (Figure 1) includes a capacitor with a constant current source, which is connected to the capacitor, as long as a charge condition is satisfied, that is to say the input signal E is at logical "0" and the response signal A at logical "1". The voltage U increases in the capacitor proportionally to the time interval t_N in which there is the charge condition. For example, a Schmitt trigger monitors the voltage U, which compares the voltage U with a constant voltage, the limit value G. An output of the Schmitt trigger circuit is connected by means of a gate circuit through to the signal line 17 (Figure 1) and the signal switch 16. If the voltage U over the capacitor exceeds the limit value G, the Schmitt trigger responds. The alarm signal is triggered at the instant of the interrupt signal I (Figure 3), when the Schmitt trigger has responded and the interrupt condition is satisfied. The capacitor is completely discharged during the reset signal R (Figure 3) and thus is ready for the next measurement. The limit value G corresponds to the voltage which is reached in the capacitor after a charging time of approximately 800 ns. In this embodiment, the limit value memory 15 (Figure 1) is a simple voltage divider. Even this type of coarse examination of the delay Δt allows the genuineness of the data carrier

exchanging data with the card reader 1 to be established in a simple manner, and optionally, data exchange with an autonomous card to be interrupted.

Figure 6 shows the operating conditions for asynchronous IC cards 2 (Figure 1). The input signal E for the IC card circuit 3 (Figure 1) includes a formatted data packet 38 with data bits carrying information in a pre-determined arrangement and grouping, a start bit "1" 39 and at least one stop bit "K" 40. The start bit "1" 39 heads the data packet 38 and the stop bit "K" 40 terminates the data packet 38. The response signal A generated by the IC card is configured in a manner similar to the input signal E and includes k bits, wherein the total number of bits is pre-determined, but does not have to be the same as for the preceding input signal E. The delay Δt is measured between a characteristic edge of the input signal E and the response signal A, for example between the falling edge of the stop bit "K" 40 of the input signal E and the falling edge of the start bit "1" 41 of the response signal A directly following. By counting the pulse sequence T in the command phase, the control module 6 (Figure 1) generates the reset signal R at the beginning of the command transmission to the IC card circuit 3 at the first instant 42 and the start signal at the second instant 43 at the end of this command transmission, which is determined by the falling edge of the stop bit "K" 40. The end of the command phase is indicated by a change of the levels from logical "0" to "1" of the enable signal E. The time interval until the response signal A is received at the third instant 44 is measured by the measuring circuit 13 (Figure 1), and processed in the computing unit 14 (Figure 1). The stop signal at the third instant 44 is triggered by the falling edge of the start bit "1" 41 of the response signal A, when the enable signal F is at logical "1". The stop signal is sent to the computing unit 14 as the interrupt signal at the fourth instant 45, after a delay of S clock pulses. The oscillator 22 (Figure 2) generates, at the clock pulse input 23 (Figure 2), the pulse sequence Z with a frequency of at least 10MHz, in order to obtain a sufficient resolution for differentiating the number of program steps in the IC card, although the delay Δt can be up to 10 ms.

The card reader 1 (Figure 1) identifies the design of the IC card circuit 3 installed in the IC card 2 with the aid of the first response of the IC card 2. The delay Δt of the first response depends on construction and internal programming, so IC cards with the same functions, but with IC card circuits from different manufacturers, are differentiated by means of the number of program steps needed up to the first response, that is to say in the delay Δt of the response. The limit value memory 15 (Figure 1) includes a set of limit value ranges G, which have to be previously established for each of the known types of genuine card and stored in the limit value memory (15). The measuring means 12 (Figure 1) compares the measured value of the delay Δt with the limit value range G pre-determined for the identified design of the IC card 2. If the measured value of the delay Δt lies outside the limit value range G, the alarm signal is triggered. As it is unlikely that falsified cards are programmed such that the responses are transmitted with the same delay Δt as the genuine IC cards, falsified cards are recognisable to the card reader 1.

The logic modules shown in the drawings of the circuits are described, for example, in U. Tieze and Ch. Schenk "Advanced Electronic Circuits", Springer Verlag (1978), in particular on pages 203 - 372. The level information and modifications thereto can also be read systematically reversed without affecting functioning.

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Claims

1. Apparatus for recognising genuine electronic IC cards (2) in card readers (1), with a coupling means (5) to the IC circuit (3) and with means (4) for exchanging electronic data from and to the IC card circuit (3), characterised in that,
the means for data exchange (4) are provided with a measuring means (12) for measuring a temporal delay Δt between an input signal (E) for the IC card (2) and a response signal (A) produced by the IC card (2) as a response to the card reader (1), and a limit value memory (15) for limit values (G; P) of the delay Δt,
that there is at least one pre-determined limit value range (G) of the permissible delay Δt in the limit value memory (15), and
that the means for data exchange (4) are arranged for comparing the delay Δt measured with at least one permissible limit value range (G) stored in the limit value memory (15), in order to examine the genuineness of the IC card (2), and when there is a negative result, to reject the IC card (2).

2. Apparatus according to claim 1, characterised in that the card reader (1) includes a pulse generator (10) connected to the means for data exchange (4) for generating a pulse sequence (T) for synchronising the IC card circuit (3) with the means for data exchange, and that the measuring means (12) is arranged as an input signal (E) for measuring the delay Δt of the response signal (A) compared to the pulse sequence (T).

3. Apparatus according to claim 1 or 2, characterised in that the measuring means (12) is provided with a measuring circuit (13) with a first edge detector (18) for generating a start signal when a falling edge of the input signal (E) is recognised, and a second edge detector (19) for generating a stop signal when a falling edge of the response signal (A) directly

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following the falling edge of the input signal (E) is recognised, that the measuring circuit (13) is arranged for measuring values of the delay Δt, and that the measured values are intervals of time between the start signal and the stop signal.

4. Apparatus according to claim 3, characterised in that the measuring circuit (13) is provided with an oscillator (22) for generating clock pulses and a start-stop counter (20) for measuring the delay Δt by counting the clock pulses, that lines extend from an output of the oscillator (22) to the clock pulse input (23) of the start-stop counter (20), from an output of the first edge detector (18) to the start signal input (24) of the counter (20) and from an output of the second edge detector (19) to the stop signal input (25) of the counter (20), and that each measured value is equal to the number of clock pulses counted in the counter (20) between the start signal and the stop signal.

5. Apparatus according to one of claims 1 to 4, characterised in that the means for data exchange (4) are provided with a computing unit (14) and a signal switch (16) connected via a signal line (17) to the computing unit (14),
that the computing unit (14) is arranged for comparing the measured delays Δt with the stored limit value ranges (G) and for generating an alarm signal on the signal line (17) if the delay Δt measured is outside the stored limit value range (G), and

6. Apparatus according to one of claims 1 to 5, characterised in that the means for data exchange (4) are provided with a computing unit (14) and a signal switch (16) connected via a signal line (17) to the computing unit (14),
that the computing unit (14) for evaluating the measured values of the delay Δt according to statistical criteria, is arranged for comparing at

least one calculated statistical parameter with a pre-determined limit value (P), assigned to the statistical parameter, stored in the limit value memory (15), and to generate an alarm signal when one of the statistical parameters exceeds the assigned limit value P, and

that the signal switch (16) is arranged for interrupting data exchange with the IC card (2) by means of the alarm signal.

7. Method for recognising the genuineness of electronic IC cards (2) in card readers (1) during a data exchange between means for data exchange (4) belonging to the card reader (1) and an integrated IC card circuit (3) built into the IC card (2), which are connected to one another via a coupling means (5) required for the flow of data from and to the IC card circuit (3), characterised in that

temporal delays Δt are measured using a measuring means (12) in the means for data exchange (4),

that the temporal delay Δt between an input signal E given by the means for data exchange (4) to the IC card (2) and an output signal A given by the IC card (2) as a response to the card reader (1) is measured,

that the measured values of the delay Δt are compared with at least one limit value range G of permissible values of the delay Δt which is stored in a limit value memory (15), and that when there is a negative comparison result, the data exchange is interrupted by the means for data exchange (4) and the IC card (2) is rejected as being false.

8. Method according to claim 7, characterised in that the data exchange is interrupted by a signal switch (16) in the means for data exchange (4), as soon as the measured delay Δt is outside the permissible limit value range G.

9. Method according to claim 7 or 8, characterised in that the measured values of the delay Δt are sought using a computing unit (14) in the

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means for data exchange (4) according to statistical criteria,
that at least one statistical parameter calculated by the computing unit (14) is compared with pre-determined limit values P stored in the limit value memory (15), and
that the data exchange is interrupted by a signal switch (16) in the means for data exchange (4), as soon as at least one of the calculated statistical parameters exceeds the pre-determined limit value P corresponding to it.

10. Method according to one of claims 7 to 9, characterised in that a pulse sequence T from a pulse generator (10) belonging to the card reader (1), connected to the means for data exchange (4), is used for synchronising the IC card circuit (3) with the means for data exchange (4) and as the input signal E sent to the IC card (2).

11. Method according to one of claims 7 to 9, characterised in that pre-determined and formatted data packets (38) with a start pulse (39-41) and at least one stop pulse (40) are used for the data exchange, wherein the formatted data packets (38) sent to the IC card (2) represent the input signal E and the formatted data packets (38) generated by the IC card for the card reader represent the response signal A,
that one edge of the input signal E is used as the start signal and one edge of the response signal A is used as the stop signal,
and that the temporal delay Δt between the start signal of the input signal E and the stop signal of the response signal A following the input signal E is measured.

12. Method according to claim 11, characterised in that the design of the IC card is identified by the card reader by means of at least one of the data packets of the response signal A,
and that the measured values of the delay Δt and/or the calculated statistical parameter is compared with a set of limit value ranges G

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and/or a set of limit values P, which are pre-determined for the identified design of the IC card.

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