

SEMICONDUCTOR APPARATUS AND METHOD FOR FABRICATING THEREOF

FIELD OF THE INVENTION

5 The disclosures made herein relate generally to a semiconductor apparatus, and more particularly to relates to a method for manufacturing a semiconductor apparatus (e.g., E-mode p-type gate Gallium nitride high-electron-mobility transistor (GaN HEMT) device).

10 BACKGROUND OF THE INVENTION

Ascribed to the capability of carrying large current and supporting high voltages, Gallium nitride (GaN) semiconductor devices are recognized as the next generation of semiconductor devices suitable for power applications. A GaN High Electron Mobility Transistor (HEMT) device operates based on a conductive two-
15 dimensional electron gas (2DEG), which can be modulated by a gate metal contact. The 2DEG is formed between two epitaxially grown nitride layers, which have different bandgaps. These two consecutively grown nitride layers cause polarization at an interface, which contributes to the formation of the 2DEG layer near the junction of the two layers, specifically in the layer with the narrower band
20 gap.

The nitride layers that cause polarization have different bandgaps, so the junction between these two nitride layers is called heterojunction, which typically is constituted with a barrier layer of Aluminium gallium nitride (AlGaN) adjacent to a layer of gallium nitride (GaN) to include the 2DEG, which is the flowing

charge during the operations. By making ohmic contact to drive the 2DEG and a gate contact to modulate the 2DEG, the transistors can be made out of such heterojunction. Such transistors are called as a GaN HEMT. Since the 2DEG is formed by intrinsic material properties, the GaN HEMTs is normally-on (D-
5 mode) devices without any special design. However, for power application, normally-off (E-mode) operation is indispensable. Many device designs have been tried to realize E-mode operation. Among them, devices with a p-GaN or p-AlGaN top layer is the only commercialized design.

As shown in FIG. 1a, a top p-GaN or a p-AlGaN layer (13) will deplete
10 the 2DEG (16) between an AlGaN barrier (12) and a GaN buffer layer (11). For E-mode device operation, the 2DEG (16) should be only depleted at gate region. In order to achieve this, the top p-GaN or p-AlGaN layer (13) should be removed at the access and ohmic contact region. Dry-etching was usually used. After the dry etching process, the surface passivation is very critical for achieving stable
15 device performance. Conventionally, the LP-Nitride was used for GaN device passivation for the commercial product. However, during the LP-Nitride deposition process, Mg dopants will be de-activated and the GaN HEMT will become normally-on again. Alternatively, ALD-Al₂O₃ was used as the passivation layer. However, the passivation effect of ALD-Al₂O₃ was not so
20 consistent and it's not as good as the LP-Nitride, which is widely adopted for D-mode GaN transistors in the commercial productions.

SUMMARY OF THE INVENTION

The present invention relates to a semiconductor apparatus. The semiconductor apparatus includes a Gallium nitride (GaN) buffer, an Aluminium gallium nitride (AlGaN) barrier, and at least one of a top p-GaN and a p-AlGaN, 5 wherein the at least one of the top p-GaN and the p-AlGaN depletes a two-dimensional electron gas (2DEG) between the GaN buffer and the AlGaN barrier. The 2DEG appears again at a region without the at least one of the top p-GaN and the p-AlGaN, wherein remaining p-GaN region is called as a p-GaN gate after partially removing the at least one of the top p-GaN and the p-AlGaN. A thin low 10 pressure (LP) Nitride passivation layer is deposited on a portion of the AlGaN barrier and a portion of the p-GaN gate. After the deposition of the thin LP-Nitride passivation layer on the portion of the AlGaN barrier and the portion of the p-GaN gate, the semiconductor apparatus applies at least one re-activation process.

In an embodiment, the at least one re-activation process applies a high 15 temperature to break a Mg-H bonds in the p-GaN gate of the semiconductor apparatus and recover an activity of Magnesium (Mg) dopants in the pGaN gate of the semiconductor apparatus after deposition of the thin LP-Nitride passivation layer.

In an embodiment, the high temperature is about 800 - 850°C.

20 In an embodiment, the at least one re-activation process recovers a p-type doping to a same level as before the deposition of the thin LP-nitride passivation layer, wherein the p-type doping level is about $6 - 9 \times 10^{17}$ per cm^3).

In an embodiment, the at least one re-activation process comprises at least one of an in-situ furnace annealing process, an ex-situ furnace annealing process, and an ex-situ Rapid thermal anneal (RTA) annealing process.

In an embodiment, for the in-situ furnace annealing process, the
5 semiconductor apparatus ~~undergoes an additional annealing step~~ is kept at 800 – 850 °C temperature under Nitrogen (N₂) flow for about 10 - 20 minutes right after completing LPCVD deposition process and before being unloaded from a Low Pressure Chemical Vapor Deposition (LPCVD) furnace.

In an embodiment, for the ex-situ furnace annealing process, a high
10 temperature of about 800 – 850 °C with N₂ flow annealing is applied for about 10 – 20 minutes to ensure a re-activation process on the semiconductor apparatus.

In an embodiment, for the ex-situ RTA annealing process, a high temperature of about 900 – 1000 °C) with N₂ flow annealing is applied for a time period of about 30 – 60 seconds on the semiconductor apparatus.

15 ~~In an embodiment, the very short time comprises less than 2 minutes.~~

In an embodiment, the semiconductor apparatus comprises an E-mode p-type gate Gallium nitride high-electron-mobility transistor (GaN HEMT) device.

In an embodiment, the semiconductor apparatus uses the thin LP-Nitride passivation layer as the passivation layer while keeping a normally-off
20 characteristics of the semiconductor apparatus.

The present invention relates to a method for fabricating a semiconductor apparatus. The method includes providing a GaN buffer. Further, the method includes depositing an AlGaN barrier on the GaN buffer. Further, the method includes providing at least one of a top p-GaN and a p-AlGaN, wherein the at

least one of the top p-GaN and the p-AlGaN depletes a 2DEG between the GaN buffer and the AlGaN barrier. The 2DEG appears again at a region without the at least one of the top p-GaN and the p-AlGaN, wherein remaining p-GaN region is called a p-GaN gate after partially removing the at least one of the top p-GaN and
5 the p-AlGaN. Further, the method includes providing a thin LP Nitride passivation layer, wherein the thin LP-Nitride passivation layer is deposited on a portion of the AlGaN barrier and a portion of the p-GaN gate. Further, the method includes applying at least one re-activation process on the semiconductor apparatus after the deposition of the thin LP-Nitride layer on the portion of the
10 AlGaN barrier and the portion of the p-GaN gate.

BRIEF DESCRIPTION OF THE ACCOMPANYING DRAWINGS

The present invention will be fully understood from the detailed description given herein below and the accompanying drawings which are given
15 by way of illustration only, and thus are not limitative of the present invention, wherein:

Figure 1a illustrates a conventional semiconductor apparatus.

Figure 1b and Figure 1c illustrate an example of a fabrication of a semiconductor apparatus in which an ep-stack, a p-GaN gate formation by dry-
20 etching process and a LP-Nitride passivation step are depicted, in accordance with one embodiment of the present invention.

Figure 2 is a flow chart illustrating a method for fabricating a semiconductor apparatus, according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Detailed description of preferred embodiments of the present invention is disclosed herein. It should be understood, however, that the embodiments are merely exemplary of the present invention, which may be embodied in various
5 forms. Therefore, the details disclosed herein are not to be interpreted as limiting, but merely as the basis for the claims and for teaching one skilled in the art of the invention. The numerical data or ranges used in the specification are not to be construed as limiting. The following detailed description of the preferred embodiments will now be described in accordance with the attached drawings,
10 either individually or in combination.

Accordingly, the embodiment herein is to provide a method for fabricating a semiconductor apparatus. The method includes providing a GaN buffer. Further, the method includes depositing an AlGa_N barrier on the GaN buffer. Further, the method includes providing at least one of a top p-GaN and a p-AlGa_N, wherein
15 the at least one of the top p-GaN and the p-AlGa_N depletes a 2DEG between the GaN buffer and the AlGa_N barrier. The 2DEG appears again at a region without the at least one of the top p-GaN and the p-AlGa_N, wherein remaining p-GaN region is called a p-GaN gate after partially removing the at least one of the top p-GaN and the p-AlGa_N. Further, the method includes providing a thin LP Nitride
20 passivation layer, wherein the thin LP-Nitride passivation layer is deposited on a portion of the AlGa_N barrier and a portion of the p-GaN gate. Further, the method includes applying at least one re-activation process on the semiconductor apparatus after the deposition of the thin LP-Nitride layer on the portion of the AlGa_N barrier and the portion of the p-GaN gate.

In the conventional methods, in order to fabricate the E-Mode GaN transistors, p-GaN gate technology is widely adopted. In this technology, a cap p-GaN or p-AlGaN is only kept at the gate region. All the other area of p-GaN or p-AlGaN is removed by dry etching process. After this dry etching process, proper passivation is necessary to suppress leakage current and trapping effect. Conventionally, LP-Nitride is widely adopted for GaN device passivation. However, for p-GaN gate E-mode devices, the LP-Nitride passivation will convert the device to normally-on. Instead, ALD- Al_2O_3 was usually used as the passivation layer. However, the passivation effect is not as good as LP-Nitride. In the proposed method, the proposed method can be used to achieve E-mode operation with LP-Nitride passivation with some process modification.

During the LP-Nitride process, H atoms will diffuse into the p-GaN layer under high temperature. The H atoms will form chemical bond with the Mg dopants. In this way, the Mg dopants will become de-activated (i.e., they will become electrically inactive and cannot emit holes during the device operation). In the proposed method, after the LP-Nitride deposition, the method will apply high temperature process to break the Mg-H bonds and recover the activity of Mg dopants. This is called as a re-activation process.

In the conventional methods, after pGaN layer removal, normally the user of the semiconductor apparatus uses a ALD (Atom Layer Deposition) film deposition for the surface passivation. In the proposed method, the method uses a LPCVD SiN film or the thin LP-Nitride passivation layer, the ALD film

deposition has lower temperature (~ 300C), whereas the LPCVD film has higher temperature (~ 800C), so that the higher temperature having better performance in terms of preventing surface leakage current and reduce current collapse effect.

In the proposed method, after deposition, the Mg doping in pGaN gate will be 5 deactivated by the LPCVD process, which will result HEMT device V^{th} shift, the method uses the annealing to re-activate the Mg doping in pGaN gate, so as to maintain HEMT device V^{th} performance.

Referring now to the drawings and more particularly to **Figure 1b** through **Figure 2**, where similar reference characters denote corresponding 10 features consistently throughout the figures, there are shown preferred embodiments.

Figure 1b to **Figure 1c** illustrate an example of a semiconductor apparatus (1000) in which an ep-stack, a p-GaN gate formation by dry-etching process and a LP-Nitride passivation step are depicted, in accordance with one embodiment 15 of the present invention. The semiconductor apparatus (1000) can be an E-mode p-type gate GaN HEMT device.

As shown in the **Figure 1b**, for as-grown epi wafers, the top p-GaN or p-AlGaN (130) will deplete a 2DEG (140) between a GaN buffer (110) and an AlGaN barrier (120). Preferably, the top p-GaN or p-AlGaN (130) has thickness 20 of about 60 – 120 nanometers (nm), the GaN buffer (110) has thickness of about 4.8 – 5.2 microns (μm) and the AlGaN barrier (120) has thickness of about 15 – 24 nm. After partially removing the top p-GaN layer the 2DEG (140) appears again at the region without p-GaN layer. The remaining p-GaN region is called as a p-GaN gate (150). The **Figure 1c** shows a thin LP-Nitride passivation layer

(160) is deposited on the portion of the AlGa_N barrier (120) and a portion of the p-GaN gate (150). After the deposition of the thin LP-Nitride passivation layer (160), the semiconductor apparatus (1000) uses three ways to apply the re-activation process, as shown in the following:

- 5 1. In-situ furnace annealing: the semiconductor apparatus (1000) undergoes an extra annealing step under N₂ flow before getting unloaded from a LPCVD furnace, wherein the semiconductor apparatus (1000) is kept at 800 – 850 °C temperature under Nitrogen (N₂) flow for about 10 - 20 minutes.
- 10 2. Ex-situ furnace annealing: with ex-situ furnace annealing, higher annealing temperature can be applied to ensure the re-activation effect in the semiconductor apparatus (1000), wherein the higher annealing temperature is within a range of about 800 – 850 °C.
- 15 3. Ex-situ RTA annealing: high annealing annealing of about of about 900 – 1000 °C with N₂ flow annealing is applied in very short time (i.e., within a time period of 30 – 60 seconds) in the semiconductor apparatus (1000).

Based on the re-activation process, the semiconductor apparatus (1000) can recover the p-type doping to the same level as before the LP-Nitride deposition. Preferably, the p-type doping level is within a range of about 6 – 9 x10¹⁷ per cubic centimetre (cm⁻³)

Figure 2 is a flow chart (S200) illustrating a method for fabricating the semiconductor apparatus (1000), according to one embodiment of the present invention. At S202, the method includes providing the GaN buffer (110). At S204,

the method includes depositing the AlGa_N barrier (120) on the Ga_N buffer (110).
At S206, the method includes providing at least one of the top p-Ga_N and a p-AlGa_N (130). The at least one of the top p-Ga_N and the p-AlGa_N (130) depletes the 2DEG (140) between the Ga_N buffer (110) and the AlGa_N barrier (120). The
5 2DEG (140) appears again at a region without the at least one of the top p-Ga_N and the p-AlGa_N (130). The remaining p-Ga_N region is called the p-Ga_N gate (150) after partially removing the at least one of the top p-Ga_N and the p-AlGa_N (130). Preferably, the top p-Ga_N or p-AlGa_N (130) has thickness of about 60 – 120 nanometers (nm), the Ga_N buffer (110) has thickness of about 4.8 – 5.2
10 microns (μm) and the AlGa_N barrier (120) has thickness of about 15 – 24 nm.

At S208, the method includes providing the thin LP Nitride passivation layer (160), wherein the thin LP-Nitride passivation layer (160) is deposited on a portion of the AlGa_N barrier (120) and a portion of the p-Ga_N gate (150). At S210, the method includes applying the re-activation process on the
15 semiconductor apparatus (1000) after the deposition of the thin LP-Nitride layer (160) on the portion of the AlGa_N barrier (120) and the portion of the p-Ga_N gate (150).

In the conventional methods, after pGa_N layer removal, normally the user of the semiconductor apparatus uses a ALD (Atom Layer Deposition) film
20 deposition for the surface passivation. In the proposed method, the method uses a LPCVD Si₃N₄ film or the thin LP-Nitride passivation layer (160), the ALD film deposition has lower temperature (~ 300C), whereas the LPCVD film has higher temperature (~ 800C), so that the higher temperature having better performance in terms of preventing surface leakage current and reduce current collapse effect.

In the proposed method, after deposition, the Mg doping in pGaN gate will be deactivated by the LPCVD process, which will result HEMT device V^{th} shift, the method uses the annealing to re-activate the Mg doping in pGaN gate, so as to maintain HEMT device V^{th} performance.

- 5 In the conventional methods, in order to to fabricate the E-Mode GaN transistors, p-GaN gate technology is widely adopted. In this technology, a cap p-GaN or p-AlGaN is only kept at the gate region. All the other area of p-GaN or p-AlGaN is removed by dry etching process. After this dry etching process, proper passivation is necessary to suppress leakage current and trapping effect.
- 10 Conventionally, LP-Nitride is widely adopted for GaN device passivation. However, for p-GaN gate E-mode devices, the LP-Nitride passivation will convert the device to normally-on. Instead, ALD- Al_2O_3 was usually used as the passivation layer. However, the passivation effect is not as good as LP-Nitride. In the proposed method, the proposed method can be used to achieve E-mode
- 15 operation with LP-Nitride passivation with some process modification.

During the LP-Nitride process, H atoms will diffuse into the p-GaN layer under high temperature. The H atoms will form chemical bond with the Mg dopants. In this way, the Mg dopants will become de-activated (i.e., they will become electrically inactive and cannot emit holes during the device operation).

- 20 In the proposed method, after the LP-Nitride deposition, the method will apply high temperature process to break the Mg-H bonds and recover the activity of Mg dopants. The is called as a re-activation process.

The terminology used herein is for the purpose of describing particular example embodiments only and is not intended to be limiting. As used herein, the

singular forms "a", "an" and "the" may be intended to include the plural forms as well, unless the context clearly indicates otherwise. The terms "comprises", "comprising", "including" and "having" are inclusive and therefore specify the presence of stated features, integers, steps, operations, elements and/or 5 components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components and/or groups thereof. The method steps, processes and operations described herein are not to be construed as necessarily requiring their performance in the particular order discussed or illustrated, unless specifically identified as an order of performance.

10 It is also to be understood that additional or alternative steps may be employed. The use of the expression "at least" or "at least one" suggests the use of one or more elements, as the use may be in one of the embodiments to achieve one or more of the desired objects or results.

CLAIMS

We claim:

1. A semiconductor apparatus (1000), comprises:
 - i. a Gallium nitride (GaN) buffer (110);
 - 5 ii. an Aluminium gallium nitride (AlGaN) barrier (120);
 - iii. at least one of a top p-GaN and a p-AlGaN (130), wherein the at least one of the top p-GaN and the p-AlGaN (130) depletes a two-dimensional electron gas (2DEG) (140) between the GaN buffer (110) and the AlGaN barrier (120);
- 10 wherein the 2DEG (140) appears again at a region without the at least one of the top p-GaN and the p-AlGaN (130), wherein remaining p-GaN region is called a p-GaN gate (150) after partially removing the at least one of the top p-GaN and the p-AlGaN (130);
- 15 characterized in that:
 - a thin low pressure (LP) Nitride passivation layer (160) is deposited on a portion of the AlGaN barrier (120) and on a portion of the p-GaN gate (150); and
 - 20 wherein the semiconductor apparatus (1000) applies at least one re-activation process after the deposition of the thin LP-Nitride layer (160) on the portion of the AlGaN barrier (120) and the portion of the p-GaN gate (150).

2. The semiconductor apparatus (1000) as claimed in claim 1, wherein the at least one re-activation process applies a high temperature to break a Mg-H bonds in the p-GaN gate (150) of the semiconductor apparatus (1000) and recover an activity of Magnesium (Mg) dopants in the pGaN gate (150) of the semiconductor apparatus (1000) after deposition of the thin LP-Nitride passivation layer (160).
5
3. The semiconductor apparatus (1000) as claimed in claim 2, wherein the high temperature is about 800°C.
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4. The semiconductor apparatus (1000) as claimed in claim 1, wherein the at least one re-activation process recovers a p-type doping to a same level as before the deposition of the thin LP-Nitride passivation layer (160), wherein the p-type doping level is within a range of about $6 - 9 \times 10^{17}$ per cubic centimeter.
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5. The semiconductor apparatus (1000) as claimed in claim 1, wherein the at least one re-activation process comprises at least one of an in-situ furnace annealing process, an ex-situ furnace annealing process, and an ex-situ Rapid thermal anneal (RTA) annealing process.
20
6. The semiconductor apparatus (1000) as claimed in claim 5, wherein, for the in-situ furnace annealing process, the semiconductor apparatus (1000) is kept at 800 – 850 °C temperature under Nitrogen (N₂) flow for about 10

- 20 minutes before getting unloaded from a Low Pressure Chemical Vapor Deposition (LPCVD) furnace.

5 7. The semiconductor apparatus (1000) as claimed in claim 5, wherein for the ex-situ furnace annealing process, a high annealing temperature of about 800 – 850 °C is applied to ensure a re-activation process on the semiconductor apparatus (1000).

10 8. The semiconductor apparatus (1000) as claimed in claim 5, wherein for the ex-situ RTA annealing process, a high annealing temperature of about of about 900 – 1000 °C with N₂ flow annealing is applied within a time period of 30 – 60 seconds on the semiconductor apparatus (1000).

15 9. The semiconductor apparatus (1000) as claimed in claim 8, wherein the very short time comprises less than 2 minutes.

20 10. The semiconductor apparatus (1000) as claimed in claim 1, wherein the semiconductor apparatus (1000) comprises an E-mode p-type gate Gallium nitride high-electron-mobility transistor (GaN HEMT) device.

11. The semiconductor apparatus (1000) as claimed in claim 1, wherein the semiconductor apparatus (1000) uses the thin LP-Nitride passivation layer (160) as a passivation layer while keeping a normally-off characteristics of the semiconductor apparatus (1000).

12. A method for fabricating a semiconductor apparatus (1000), comprises:

- i. providing a Gallium nitride (GaN) buffer (110);
- ii. depositing an Aluminium gallium nitride (AlGaN) barrier (120) on
5 the GaN buffer (110);
- iii. providing at least one of a top p-GaN and a p-AlGaN (130),
wherein the at least one of the top p-GaN and the p-AlGaN (130)
depletes a two-dimensional electron gas (2DEG) (140) between
the GaN buffer (110) and the AlGaN barrier (120);

10 wherein the 2DEG (140) appears again at a region without
the at least one of the top p-GaN and the p-AlGaN (130), wherein
remaining p-GaN region is called a p-GaN gate (150) after
partially removing the at least one of the top p-GaN and the p-
AlGaN (130);

15 characterized in that:

depositing a thin low pressure (LP) Nitride passivation layer (160)
on a portion of the AlGaN barrier (120) and on a portion of the p-
GaN gate (150); and

20 applying at least one re-activation process on the semiconductor
apparatus (1000) after the deposition of the thin LP-Nitride layer
(160) on the portion of the AlGaN barrier (120) and on the portion
of the p-GaN gate (150).

13. The method as claimed in claim 12, wherein the at least one re-activation process applies a high temperature to break a Mg-H bonds in the p-GaN gate (150) of the semiconductor apparatus (1000) and recover an activity of Magnesium (Mg) dopants in the pGaN gate (150) of the semiconductor apparatus (1000) after deposition of the thin LP-Nitride passivation layer (160).
14. The method as claimed in claim 13, wherein the high temperature is about 800°C.
15. The method as claimed in claim 12, wherein the at least one re-activation process recovers a p-type doping to a same level as before the deposition of the thin LP-Nitride passivation layer (160), wherein the p-type doping level is within a range of about $6 - 9 \times 10^{17}$ per cubic centimeter.
16. The method as claimed in claim 12, wherein the at least one re-activation process comprises at least one of an in-situ furnace annealing process, an ex-situ furnace annealing process, and an ex-situ Rapid thermal anneal (RTA) annealing process.
17. The method as claimed in claim 16, wherein, for the in-situ furnace annealing process, the semiconductor apparatus (1000) is kept at 800 – 850 °C temperature under Nitrogen (N₂) flow for about 10 - 20 minutes

before getting unloaded from a Low Pressure Chemical Vapor Deposition (LPCVD) furnace.

18. The method as claimed in claim 16, wherein for the ex-situ furnace
5 annealing process, a high annealing temperature of about 800 – 850 °C is applied to ensure a re-activation process on the semiconductor apparatus (1000).

19. The method as claimed in claim 16, wherein for the ex-situ RTA annealing
10 process, a high annealing temperature of about 900 – 1000 °C with N₂ flow annealing is applied in within a time period of about 30 – 60 seconds on the semiconductor apparatus (1000).

20. The method as claimed in claim 12, wherein the semiconductor apparatus
15 (1000) comprises an E-mode p-type gate Gallium nitride high-electron-mobility transistor (GaN HEMT) device.

21. The semiconductor apparatus (1000) as claimed in claim 12, wherein the
semiconductor apparatus (1000) uses the thin LP-Nitride passivation layer
20 (160) as a passivation layer while keeping a normally-off characteristics of the semiconductor apparatus (1000).