

INTEGRATED CIRCUIT SYSTEMS ~~AND METHOD~~
FOR ANALOG SIGNAL RECORDING AND PLAYBACK

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present relates to the field of integrated circuit analog signal recording and playback devices and methods wherein an analog signals are directly stored in and read out from a plurality of memory cells.

2. Prior Art

U.S. Patent No. 4,890,259 discloses a nonvolatile high density integrated circuit analog signal recording and playback system wherein an analog input signal is sampled a plurality of times and then, as additional samples are being taken and temporarily held, a prior set of samples of the analog signal are parallel loaded into a plurality of storage sites or cells, each comprising nonvolatile floating gate memory cells, preferably EEPROM cells. In that system, writing of the groups of samples into the respective storage cells is done by iteratively providing a write pulse followed by a read operation for the respective cells to compare the information stored in each cell with the information held by the respective sample and hold circuit. During the successive write read operations, the write pulse is increased in amplitude, with the write pulses to any cell being stopped or decoupled from the cell when the information read from the cell in the last read operation equaled the value held in the respective sample and hold circuit. To provide time for the successive write read operations, a plurality of sample and hold circuits are provided so that an equal plurality of cells may be loaded or written to at one time. Still, because of practical limitations in the number of sample and hold circuits which may be provided and the

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-1C

~~Figure 1~~ is a block diagram of a preferred embodiment of an integrated circuit analog signal record and playback system in accordance with the present invention.

Figure 2 is a block diagram level representation of a trimming hierarchy in the reference generation block of the circuit which makes use of certain EEPROM cells, allowing the same to be programmed to suitable digital values to set the optimum voltage reference and current reference with the proper temperature coefficients.

Figure 3 shows the dual cell differential weighted sensing scheme for the trim cells.

Figure 4 is a circuit diagram illustrating the current bias distribution scheme.

Figure 5 is a circuit diagram for the closed loop sample and hold circuits and associated circuitry which compensates for the threshold losses and other non-linearities and manufacturing variations which may exist across the die.

Figure 6 is a schematic diagram for the circuit used for the dual level iterative write of the present invention.

Figure 7 is a block diagram of the clock circuit of the present invention.

Figure 8 is a circuit diagram of the clock circuit of Figure 7.

Figure 9 is a block diagram for the circuit for detecting invalid addresses and the use of the same to control configuration bits for the integrated circuit system.

Figure 10 illustrates a variation of Figure 9 showing the addition of a latch to store the value of the configuration bits.

Figure 11 shows the analog connections for connecting several devices to a single microphone, AGC resistor and capacitor, and loudspeaker for cascading multiple devices to extend the record and/or playback time in a simple and efficient manner.

Figure 12 is a circuit diagram for the high voltage ramp up and ramp down circuit used in the preferred embodiment.

Figure 13 is a circuit diagram of a binary counter and analog switches of ^{a high voltage increment circuit called} the HV INC circuit.

Figure 14 is a circuit diagram of the capacitors and comparator of ^y the HV INC circuit.

^{a high voltage increment circuit called}

this event the external oscillator block detects the presence of an incoming frequency and steers the external clock to the 512 KHz output. If external synchronization is not required, the external clock pin is connected to either power supply pin, and the external oscillator block gates the internal oscillator to the 512 KHz output.

The internal oscillator is of the relaxation type and operates on the principle of charging a capacitor to a certain voltage by applying a certain current. Both the current and the voltage levels are obtained from the reference section - the voltage is fixed (VAGND) and the current is variable, however it would also be acceptable for this to be reversed. In fact two capacitors are used to allow for the discharge of one capacitor while the other is being charged, thus providing a more accurate discharge voltage and reduced signal propagation delays in the sections of the circuit which perform switching. The output from the oscillator is used by the 64 KHz counter and subsequently the timing circuits and sample clock. However, it is also routed through additional test logic to an output pad ($\overline{\text{EOM}}$). If the correct test mode is selected the oscillator output is directed to the EOM pad, thus allowing the oscillator frequency to be measured. The variable parameter (in this case current) is adjusted by modifying the appropriate trim bits until the oscillator frequency is at the desired value. ~~This, of course,~~
~~this of course~~ adjusts the sample frequency by the same proportions and, as described previously, since the variable current is derived from the same source as that which sets the filter roll-off frequency, the filter characteristics track the oscillator and change by the same proportion. The ability to trim the oscillator frequency allows an accurate

CLAIMS

1. A nonvolatile integrated circuit storage device having the capability of receiving, repetitively sampling, storing and reproducing an analog input signal comprising:

an array of floating gate storage cells, each for storing an analog sample of an input signal;

an input amplifier means coupled to an integrated circuit input terminal for receiving an input signal, ~~said amplifier means including an automatic gain control means for maintaining the input amplifier means output signal range within predetermined limits;~~

a plurality of sample and hold circuits, each coupled for sampling and temporarily holding a signal sample of the signal from said input amplifier means;

write means coupled to said plurality of sample and hold circuits and said array of floating gate storage cells for storing in a number of said floating gate storage cells, signal samples held in ~~said~~ the plurality of sample and hold circuits, wherein during write operations, the input signal is sequentially sampled and held in a predetermined plurality of sample and hold circuits, and then the plurality of input signal samples being held are stored in an equal plurality of storage cells while additional samples of the input signal are sequentially taken and held;

read means coupled to said array of floating gate storage cells for sequentially reading from a number of said floating gate storage cells the analog samples stored therein;

an output amplifier means coupled to an integrated circuit output terminal for providing an output signal thereto;

~~means for selectively coupling said filter between said input amplifier means output and said plurality of sample and hold circuits, whereby said filter means may provide antialiasing for the input signal during write operations; and,~~

row and column address means coupled to the array of floating gate storage cells for addressing specific cells within said array of floating gate storage cells during read and write operations;

address counter means coupled to the row and column address means for addressing the array of floating gate storage cells in logical sequences during read and write operations;

reference voltage means for providing a reference voltage;

reference storage cells also forming part of the array of floating gate storage cells, each for storing an analog sample of the reference voltage;

sample and hold circuits associated with said reference storage cells;

means for causing the reference voltage to be sampled and held when a first and a last of the predetermined plurality of input signal samples are taken;

means for causing the reference voltage samples to be stored in reference storage cells when the respective plurality of input signal samples being held are stored in the respective storage cells;

means for causing the samples of the reference voltage as stored in respective reference storage cells to be read from reference storage cells when a signal sample stored in any signal storage cell of the respective analog signal sample storage cells of the array is read out of the array;

means for providing a storage cell reference voltage by combining the reference voltages read from the reference storage cells with a relative weighting dependent upon the relative time the respective signal sample was taken and held in comparison to the times the respective reference voltage samples were taken and held, to provide a cell reference voltage; and

means for taking the difference between the signal sample read out of a storage cell of the array and the respective cell reference voltage.

~~2. The nonvolatile integrated circuit storage device of claim 1 further comprised of means for~~

~~selectively decoupling said filter from between said read means and said output amplifier means during read operations, whereby read operations may be executed at substantially accelerated clock rates for test purposes.~~

~~3. The nonvolatile integrated circuit storage device of claim 1 further comprised of means for selectively decoupling the filter from between the input amplifier means and the write means during write operations, whereby write operations may be executed at substantially accelerated clock rates.~~

~~4. A nonvolatile integrated circuit storage device having the capability of receiving, repetitively sampling, storing and reproducing an analog input signal comprising:~~

~~an array of floating gate storage cells, each for storing an analog sample of an input signal,~~

~~an input amplifier means coupled to an integrated circuit input terminal for receiving an input signal,~~

~~a filter coupled to the input amplifier means during write operations,~~

~~a plurality of sample and hold circuits, each coupled for sampling and temporarily holding a sample of the signal from said filter,~~

~~write means coupled to said plurality of sample and hold circuits and said array of storage cells for~~

~~storing in a number of said storage cells, signal samples held in the plurality of sample and hold circuits,~~

~~read means coupled to said array of storage cells for sequentially reading from a number of said storage cells the analog samples stored therein,~~

~~an output amplifier means coupled to an integrated circuit output terminal for providing an output signal thereto,~~

~~a filter coupled between said read means and said output amplifier means during read operations for providing smoothing for the output signal during read operations,~~

~~row and column address means coupled to the array for addressing said specific cells within said array of storage cells during read and write operations,~~

~~address counter means coupled to the row and column address means for addressing the array of storage cells in logical sequences during read and write operations,~~

~~an oscillator, and,~~

~~timing means coupled to the oscillator for timing the operation of the sample and hold circuits, the row and column address means, the address counter means and the read and write means.~~

2. 5. The nonvolatile integrated circuit storage device of claim 4 1 wherein said sample and hold

circuits are closed loop sample and hold circuits wherein the difference between the voltage on a holding capacitor and the signal being sampled is amplified and used to charge the holding capacitor to minimize the difference between the voltage on a said holding capacitor and the signal being sampled.

~~6. The nonvolatile integrated circuit storage device of claim 4 further comprised of means responsive to control signals to decouple the filter from between said read means and said output amplifier means during read operations to allow testing of the nonvolatile integrated circuit storage device at a substantially increased speed.~~

23. 7. The nonvolatile integrated circuit storage device of claim 4 20 further comprised of means ~~responsive to control signals~~ for selectively decoupling the filter from between the input amplifier means and the write means during write operations, whereby write operations may be executed at substantially accelerated clock rates.

~~8. The nonvolatile integrated circuit storage device of claim 4 wherein during write operations, the input signal is sequentially sampled and held in a predetermined plurality of sample and hold circuits, and~~

~~then the plurality of input signal samples being held are stored in an equal plurality of storage cells while additional samples of the input signal are sequentially taken and held, and further comprising:~~

~~reference voltage means for providing a reference voltage;~~

~~reference storage cells also forming part of the array of floating gate storage cells, each for storing an analog sample of the reference signal;~~

~~sample and hold circuits associated with said reference storage cells;~~

~~means for causing the reference voltage to be sampled and held when the first and the last of the predetermined plurality of input signal samples are taken; and,~~

~~means for causing the reference voltage samples to be stored in reference storage cells when the respective plurality of input signal samples being held are stored in the respective storage cells.~~

~~9. The nonvolatile integrated circuit storage device of claim 8 further including:~~

~~means for causing the samples of the reference voltage as stored in respective reference storage cells to be read from reference storage cells when a signal sample stored in any signal storage cell of the~~

~~respective analog signal sample storage cells of the array is read out of the array;~~

~~means for providing a storage cell reference voltage by combining the reference voltages read from the reference storage cells with a relative weighting dependent upon the relative time the respective signal sample was taken and held in comparison to the times the respective reference voltage samples were taken and held, to provide a cell reference voltage; and,~~

~~means for taking the difference between the signal sample read out of a storage cell of the array and the respective cell reference voltage.~~

3. 10- The integrated circuit storage device of claim 8 1 wherein:

the array of floating gate storage cells is arranged in columns and rows;

the reference floating gate storage cells are arranged in columns at the sides of the last named array;

and further comprised of:

~~end of message~~ floating gate storage cells used for indicating end of message arranged in columns at the sides of the reference floating gate storage cells; and,

means responsive to an end of message signal applied to the integrated circuit storage device to cause the same integrated circuit storage device to stop

a read operation or provide a signal to indicate that an end of message ~~marker~~ signal has been encountered.

4. 11. The integrated circuit storage device of claim 4 1 wherein:

the address means is also responsive to externally applied addressing signals ~~to address the start of groups of analog signal sample storage cells in the array.~~

11. 12. The integrated circuit storage device of claim 11 4 wherein:

the address range of the externally applied addressing signals ~~exceed~~ exceeds the range of addresses of the ~~start of the groups of~~ analog signal sample storage cells in the array;

and further comprising;

additional storage cells addressable by externally applied addressing signals outside the range of addresses of the ~~start of the groups of~~ analog signal sample storage cells in the array for storing digital information.

12. 13. The integrated circuit storage device of claim 12 11 further comprising:

means coupled to some of the additional storage cells for trimming the frequency of the oscillator of the integrated circuit storage device.

16. 14. The integrated circuit storage device of claim 12 11 further comprising:

means coupled to some of the additional storage cells for trimming the frequency response of a said filter of the integrated circuit storage device.

5. 15. The integrated circuit storage device of claim 11 4 further comprising:

means for setting test modes within the integrated circuit storage device.

6. 16. The integrated circuit storage device of claim 11 4 further comprising means responsive to test mode settings for mass programming of the array of signal sample storage cells in any of a plurality of test patterns.

10. 17. The integrated circuit storage device of claim 11 4 wherein:

the address range of the externally applied addressing signals exceed the range of addresses of the ~~start of the groups of~~ analog signal sample storage cells in the array;

and further comprising:

means setting configuration modes within the integrated circuit storage device.

24. 18. The integrated circuit storage device of claim 4 1 further comprising:

fast forward means to accelerate the addressing of the array of storage cells to locate the position or address of an end of message signal or to reach a position quickly without using a start address.

25. 19. The integrated circuit storage device of claim 4 1 wherein the input amplifier means includes an automatic gain control means for maintaining the input amplifier means output signal range within predetermined limits.

27. 20. The integrated circuit storage device of claim 4 1 wherein the input amplifier means includes an automatic gain control stage and a fixed gain stage, the output of the automatic gain control stage and the input to the fixed gain stage not being connected together in the integrated circuit, but each being coupled to a respective integrated circuit terminal whereby they may be connected together by connecting the last named terminals together, whereby an input signal may be

coupled to the integrated circuit through the automatic gain control stage or directly to the fixed gain stage.

28. 21. The nonvolatile integrated circuit storage device of claim 4 1 wherein said output amplifier means provides a double ended amplifier output signal.

41. 22. A plurality of nonvolatile integrated circuit storage devices, each having the capability of receiving, repetitively sampling, storing and reproducing an analog input signal;

each storage device having;

an array of floating gate storage cells, each for storing an analog sample of an input signal;

an input amplifier means coupled to an integrated circuit input terminal for receiving an input signal, said amplifier means including an automatic gain control means for maintaining the input amplifier means output signal range within predetermined limits, the input amplifier means also including a fixed gain stage, the output of the automatic gain control stage and the input to the fixed gain stage not being connected together in the integrated circuit, but each being coupled to a respective integrated

circuit terminal whereby they may be connected together by connecting the last named terminals together, whereby an input signal may be coupled to the integrated circuit through the automatic gain control stage or directly to the fixed gain stage;

a filter coupled to the input amplifier means during write operations;

a plurality of sample and hold circuits, each coupled for sampling and temporarily holding a sample of the signal from said filter;

write means coupled to said plurality of sample and hold circuits and said array of floating gate storage cells for storing in a number of said floating gate storage cells, signal samples held in the plurality of sample and hold circuits;

read means coupled to said array of floating gate storage cells for sequentially reading from a number of said floating gate storage cells the analog samples stored therein;

an output amplifier means having its input coupleable to the read means and alternatively to a terminal of the integrated circuit, and the output thereof coupleable to

an output terminal of the integrated circuit for providing an output signal thereto;

a means for coupling the filter coupled between said read means and said output amplifier means during read operations for providing smoothing for the output signal during read operations;

row and column address means coupled to the array for addressing said ~~specific~~ floating gate storage cells within said array of floating gate storage cells during read and write operations;

address counter means coupled to the row and column address means for addressing the array of floating gate storage cells in logical sequences during read and write operations;

timing means for timing the operation of the sample and hold circuits, the row and column address means, the address counter means and the read and write means;

the plurality of integrated circuit floating gate storage devices being cascaded together so that during a read operation, each device will enable the read operation of the next device when it reaches the end of its addressable input signal floating gate storage cells, and the output amplifier output of each device is

coupled to a prior device in the cascaded combination of devices, whereby the output of each device or any and all devices so cascaded is available as the output of the output amplifier of the first device of said floating gate storage devices.

7. The integrated circuit storage device of claim 6 further comprised of means for writing the test patterns in a reduced time period using multiple selection of rows and columns of the array.

8. The integrated circuit storage device of claim 7 wherein one of the plurality of test patterns is at least one alternating pattern of voltages.

9. The integrated circuit storage device of claim 8 wherein the plurality of test patterns includes horizontal stripe, vertical stripe, and checkerboard patterns.

13. The integrated circuit storage device of claim 12 wherein the additional storage cells form an extension of the array of floating gate storage cells, whereby the write means for the array of floating gate storage cells may be used also by the additional storage cells when storing digital information therein.

14. The integrated circuit storage device of claim 11 wherein at least some of the additional storage cells are used in pairs with differential logic level programming to store trim bits for the nonvolatile integrated circuit storage device, each such pair of additional storage cells being coupled to a differential sense amplifier with input weighting to force the differential sense amplifier output to a default level when the trim cells are in their native unprogrammed condition, each such pair of additional storage cells being programmable to force the differential sense amplifier output to a level opposite to the default level when the trim cells are in their native unprogrammed condition.

15. The integrated circuit storage device of claim 14 further comprising:

means coupled to some of the additional storage cells for trimming the frequency of the oscillator of the integrated circuit storage device;

means coupled to some of the additional storage cells for trimming the frequency response of the filter of the integrated circuit storage device, the oscillator and filter having a frequency and frequency response respectively which are trimmable in unison responsive to a trim current; and,

a bandgap reference means for providing a trim current to the oscillator and to the filter.

17. The integrated circuit storage device of claim 1 wherein the write means stores the signal samples held in the plurality of sample and hold circuits in said storage cells by repetitively pulsing each cell with a voltage pulse followed by reading the voltage so stored in the cell and comparing the same with the value held in the respective sample and hold circuit until the desired comparison is reached, successive voltage pulses being of increasing amplitude, the integrated circuit storage device further comprising circuit means for providing successive voltage pulse ramps of more than one pulse width to program the cells.

18. The integrated circuit storage device of claim 17 wherein a successive voltage pulse ramp is comprised of pulses of a pulse width less than the preceding voltage pulse ramp.

19. The integrated circuit storage device of claim 18 wherein the starting voltage of a successive pulse train is dependent upon the voltage of the pulse of the prior pulse train for which the desired comparison between the voltage stored in the cell and the value

held in the respective sample and hold circuit was obtained.

20. The integrated circuit storage device of claim 1 further comprising a filter coupled to the input amplifier means during write operations.

21. The integrated circuit storage device of claim 20 further comprising means for coupling the filter between said read means and said output amplifier means during read operations for providing smoothing for the output signal during read operations.

22. The integrated circuit storage device of claim 21 further comprised of means responsive to control signals to decouple the filter from between said read means and said output amplifier means during read operations to allow testing of the nonvolatile integrated circuit storage device at a substantially increased speed.

26. The integrated circuit storage device of claim 25 wherein the attack and release times for the automatic gain control means are both settable by a single external resistor and capacitor.

29. The nonvolatile integrated circuit storage device of claim 1 wherein the oscillator and filter have tracking frequency characteristics dependent on the resistance of a plurality of MOSFETs, and further comprising a high voltage supply on the integrated circuit for providing a voltage within the integrated circuit substantially above a power input voltage to the integrated circuit to control the voltage on the gates of the plurality of MOSFETs, thereby providing a wider gate control range to allow for process, temperature and power supply changes than would be provided by the lower power input voltage.

30. The nonvolatile integrated circuit storage device of claim 29 wherein the plurality of MOSFETs are low threshold MOSFETs.

31. The nonvolatile integrated circuit storage device of claim 1 further comprised of a high voltage reference on the integrated circuit coupled to a power input terminal of the integrated circuit to operate circuits thereon at voltages above the voltage on the power input terminal.

32. The nonvolatile integrated circuit storage device of claim 1 further comprised of a regulated voltage reference on the integrated circuit coupled to a

power input terminal of the integrated circuit to provide regulated array and clear gate voltages, thereby providing power supply noise rejection therefor.

33. The integrated circuit storage device of claim 1 further comprised of input logic means to power down subsections of the integrated circuit not operational during certain modes of operation of the storage device.

34. The integrated circuit storage device of claim 33 further comprised of means to pull outputs of the output amplifier means to a predetermined voltage during power down to provide a low output impedance for the outputs of the output amplifier means.

35. The integrated circuit storage device of claim 1 further comprised of means for preventing the enabling of the operation of the integrated circuit storage device for a predetermined length of time after applying power to the integrated circuit storage device or after applying a signal which causes the device to leave a power down condition to provide a settling time for circuits therein.

36. The integrated circuit storage device of claim 1 further comprised of means for detecting the presence of an externally imposed frequency and for coupling the

timing means to the external frequency in place of the oscillator.

37. The integrated circuit storage device of claim 1 wherein the write means stores the signal samples held in the plurality of sample and hold circuits in said storage cells by repetitively pulsing each cell with a voltage pulse followed by reading the voltage so stored in the cell and comparing the same with the value held in the respective sample and hold circuit until the desired comparison is reached, successive voltage pulses being of increasing amplitude, the integrated circuit storage device further comprising ramp circuit means for providing successive voltage ramps of more than one ramp rate to provide more than one pulse train of successively increasing voltage pulses to program the cells.

38. The integrated circuit storage device of claim 37 wherein the starting voltage of a successive pulse train is dependent upon the voltage of the pulse of the prior pulse train for which the desired comparison between the voltage stored in the cell and the value held in the respective sample and hold circuit was obtained. .

39. The integrated circuit storage device of claim 1 further comprising an oscillator and timing means coupled to the oscillator for timing the operation of the sample and hold circuits, the row and column address means, the address counter means and the read and write means.

40. The integrated circuit storage device of claim 1 further comprising encoding means coupled to the input amplifier means for encoding digital information into the analog input signal and decoding means coupled to the output amplifier means for recovering the digital information from the output signal.

ABSTRACT

Integrated circuit system ~~and method~~ for analog signal recording and playback having improved performance and a very high level of integration. The integrated circuit is complete with preamplifier, automatic gain control, filter, fixed references including a band gap reference, trimming, power output amplifier, memory array, multiple closed loop sample and hold circuits, column decoder, column driver, row decoder, address counters, master oscillator and chip function timing circuits including sample clock, charge pumps, high voltage regulator and waveshapers, low VCC detector, power-on reset and recording reference circuits on a single chip. ~~The chip is configurable for use of the filter as an antialiasing input filter, as an output smoothing filter or to cut out the filter, preamplifier and/or the output power filter, and for special test modes including mass programming patterns.~~ The system uses a writable analog reference scheme to put many error sources in the common mode, and provides a double ended output for maximum power output in a limited voltage range, and to allow direct connection to a speaker. Trim bits are provided for trimming the oscillator and filter so that the filter characteristics match and track the oscillator frequency and provision is made for absolute addressing and digital end of

message markers. Programming is by way of a multi level
iterative write process for high resolution, ~~with the~~
~~chips being directly cascable. Other aspects of the~~
~~integrated circuit and its operation are disclosed.~~