

SPECIFICATION

Control circuit for a positioning device using a D.C. motor

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The present invention relates to a control circuit for a positioning device using a D.C. motor.

10 A positioning device may be used for the production of semiconductor devices such as transistors and integrated circuits. In a pellet-bonding device, a semiconductor pellet is automatically brought into position on a portion for mounting the pellet in a package or a
15 lead frame, and is fastened to the pellet-mounting portion. In a wire-bonding device, a capillary for holding a connector wire made of gold or aluminium is positioned on an electrode of the semiconductor pellet or on a lead
20 portion of the lead frame, and the connector wire held by the capillary is thermally attached or welded by ultrasonic waves onto the electrode or the lead portion. In such a case, objects such as the capillary to be positioned
25 are placed on a movable table and are moved to a predetermined position.

When a D.C. motor is used as a means for driving the positioning device, a movement detector such as linear encoder or rotary encoder
30 is coupled to a controlled member, such as table or rotary member actuated by the motor in order to obtain electrical signals in accordance with movement, the D.C. motor being controlled by the comparison of output
35 signals of a counter which counts the output signals of the detector with expectation signals representing a predetermined position. When the controlled member reaches the predetermined position, the counted output signals agree with the expectation signals and
40 hence no driving signals are fed to the D.C. motor.

The D.C. motor, however, does not halt rapidly due to its moment of inertia. Hence,
45 the controlled member may often move to a position exceeding the predetermined position. In such a case, the D.C. motor is reversed in dependence upon the comparison of the counted signals of the counter with the
50 expectation signals.

In this case, if the position of the controlled member at which a count-up signal is fed to the counter, corresponding to movement in one direction, is different from the position of
55 the controlled member at which a count-down signal is produced, corresponding to movement in the opposite direction, a driving signal based upon the comparison of the counted signals with the expectation signals is
60 supplied to the D.C. motor despite the controlled member having been returned almost to the predetermined position. As a result, the controlled member develops a hunting effect.

According to the present invention there is
65 provided a control circuit for a positioning

device for moving a controlled member to a predetermined position by using a D.C. motor including;

(a) encoder means for receiving first and
70 second repeated pulse signals being produced corresponding to each movement of said controlled member by a predetermined unit distance and becoming opposite phases depending upon the direction of movement of said
75 controlled member, and for producing a first trigger signal in response to said first and second repeated signals when said first repeated pulse signal has a phase preceding the phase of the second repeated pulse signal in a
80 first direction of movement of said controlled member and a second trigger signal in response to said first and second repeated signals when said first repeated pulse signal has a phase lagging behind the phase of said
85 second repeated pulse signal in a second direction of movement of said controlled member opposite to said first direction, said first and second trigger signals having different phases from each other;

90 (b) counter means for receiving said first and second trigger signals depending upon the direction of movement of said controlled member, and for producing a binary coded signal in response to the position of said
95 controlled member;

(c) memory means for providing a predetermined binary coded signal corresponding to the predetermined position;

(d) arithmetic circuit means for producing
100 a difference binary coded signal representing the difference between the binary coded signals of said counter means and said memory means;

(e) driving circuit means for driving the
105 D.C. motor coupled to said controlled member, said driving circuit means producing a driving signal of a level corresponding to the difference binary coded signal of said arithmetic circuit means;

(f) correcting circuit means for receiving
110 said first and second repeated pulse signals and for producing a correcting pulse signal preceding occurrence of one of said first and second trigger signals in the corresponding
115 one of said first and second directions of movement of said controlled member; and

(g) connection means for providing said
120 correcting pulse signal to said arithmetic circuit means so as to cause said difference binary coded signal between the binary coded signals of said counter means and said memory means to be smaller than it would have been without the correcting pulse signal to reduce hunting, whereby the level of the
125 driving signal in said driving circuit means is decreased by said correcting signal.

Preferably, the correcting circuit means includes a flip-flop circuit which is set by the first repeated pulse signal and reset by the
130 second repeated pulse signal, and a gate

circuit receiving one of the first and second repeated pulse signals as a gate signal and transferring the output of the flip-flop circuit, and also the connection means transfers the output of the flip-flop circuit to a carry terminal of the arithmetic circuit means through the gate circuit.

The present invention will now be described in greater detail, by way of example, with reference to the accompanying drawings wherein:

Figure 1 is a block diagram of the control circuit for a positioning device using a D.C. motor in accordance with the present invention;

Figure 2 is a waveform diagram showing various signals produced by the control circuit shown in Fig. 1;

Figure 3 is a diagrammatic illustration of a rotary encoder used in the control circuit according to the present invention;

Figure 4 is a diagram showing the deviation of addresses by a half pitch in different directions of movement of the controlled member;

Figure 5 is a block diagram of a part of the control circuit, shown in Fig. 1 for explaining the effect of the present invention; and

Figure 6 is a waveform diagram showing various signals in the part of the control circuit shown in Fig. 5.

Referring first to Fig. 1, a D.C. motor 17 provides the driving force to move a controlled member 22. The D.C. motor 17 includes a movement detector 18 for producing two pulse signals ϕ_A and ϕ_B with a phase difference, in accordance with the direction of rotation of the D.C. motor 17. The movement detector 18 is, for example, composed of a rotary encoder as shown in Fig. 3. In Fig. 3, the rotary encoder includes a rotating disc 23 and a fixed plate 24. The rotating disc 23 has opaque layers 26 with a thickness of, for example, $5\mu\text{m}$ which are arranged in a regular pattern, with a constant spacing, on a transparent substrate 25. Similarly, the fixed plate 24 has a first group of opaque layers 28 and a second group of opaque layers 29 which are formed on a transparent substrate 27. The first group of opaque layers 28 and the second group of opaque layers 29 serve as a first and a second detecting portion, respectively. In order to produce two pulse signals ϕ_A and ϕ_B in accordance with the rotation of the D.C. motor 17, the rotating disc 23 and the fixed plate 24 are illuminated by a light source 30 on one side of the disc 23 and plate 24 and light which is transmitted through the rotating disc 23 and the fixed plate 24 without being obstructed by the opaque layers 26, 28 and 29 is detected by detecting elements 31 and 32 in the form of photodiodes which produce pulse signals ϕ_A and ϕ_B respectively. Since the location of the first group of opaque layers 28 has a deviation of a half pitch from the second group of opaque layers 29, the pulse

signal ϕ_A produced by the detecting element 31 is 90° out of phase with the pulse signal ϕ_B produced by the detecting element 32.

Referring again to Fig. 1, the two pulse signals ϕ_A and ϕ_B developed by the movement detector 18 are delivered through leads L_2 and L_1 . The D.C. motor 17 also includes a controller 19 which receives a control voltage through a lead L_3 and controls the speed of rotation of the D.C. motor 17. Also, the D.C. motor 17 has a generator 20 delivering a D.C. voltage corresponding to the rotating speed through a lead L_4 .

The controlled member 22, in the form of a table, is moved in the x direction by a screw 21 coupled to the D.C. motor 17. The present invention is directed to the control circuit being capable of moving this table to a predetermined position.

The two pulse signals ϕ_A and ϕ_B are produced by the movement detector 18 for each movement of the controlled member 22 by a predetermined distance (a unit distance of, for example, $5\mu\text{m}$). The phases of the two pulse signals ϕ_A and ϕ_B are reversed depending upon the direction of movement of the controlled member 22. Thus, when the controlled member 22 moves in one direction (hereinafter referred to as the forward or UP direction), the pulse signal ϕ_A is in advance of the pulse signal ϕ_B by a phase angle of 90° .

When the controlled member 22 moves in the opposite direction (hereinafter referred to as the reverse or DOWN direction), the pulse signal ϕ_B is in advance of the pulse signal ϕ_A , as shown in Fig. 2.

An up/down encoder 1 receives the pulse signals ϕ_A and ϕ_B from the movement detector 18 and produces an UP signal or a DOWN signal. When the pulse signal ϕ_B has a low level and the pulse signal ϕ_A rises from a low level to a high level, the up/down encoder 1 produces an UP signal, and when the pulse signal ϕ_B has a high level and the pulse signal ϕ_A rises from a low level to a high level, it produces a DOWN signal. Thus when the pulse signal ϕ_B has a low level and the pulse signal ϕ_A rises from a low level to a high level, the controlled member 22 is moving in the forward direction, i.e., in the UP direction, and when the pulse signal ϕ_B has a high level, and the pulse signal ϕ_A rises from a low level to a high level, the controlled member 22 is moving in the reverse direction, i.e., in the DOWN direction. A present address counter 2 consisting of an up/down counter received the Up signal or the DOWN signal which is used as a count-up signal or a count-down signal. For ease of use, addresses are set onto each of the positions of the controlled member 22. Therefore, the content of the counter 2 indicates the present position of the controlled member, i.e., the content of the counter 2 indicates an address. An object address register 3 stores an object position

(destination) of the controlled member 22, i.e., for storing an object address designated from an address designation circuit 11. An inverter group 4 consists of inverters of n bits, receives a binary signal PA of n bits from the present address counter 2 which indicates the present address of the controlled member 22, and produces a signal $\bar{P}A$ which is an inverted form of the binary signal PA. An inverter group 5 consists of n units of inverters, receives a binary signal OA of n bits which indicates the address of an object position of the object address register 3 and produces a signal $\bar{O}A$ which is an inverted form of the binary signal OA. A full adder 6 has input terminals A and B for receiving the above signals OA and PA and a carry input terminal Co. A full adder 7 adds the signals PA and $\bar{O}A$, having the same function as the full adder 6, and a positive value selector 8 transmits a positive binary output of either the output $\bar{P}A - \bar{O}A$ of the full adder 6 or the output $\bar{O}A - PA$ of the full adder 7. The positive value selector 8 includes a multiplexer which is controlled by the inverse signal $\bar{S}IGN$ of a carry overflow signal SIGN produced by the full adder 7. This selector 8 has the function of inverting input signals supplied to its input terminals A and B.

The difference between the present address stored in counter 2 and the object address stored in register 3 is processed by the control device which detects the absolute values and distinguishes positive values from negative values and, based upon the data from such values, produces a driving voltage for the D.C. motor 17 by way of a Digital-to Analog converter 12 to effect the position determining control. A large driving voltage will be produced if the distance between the present position of the controlled member 22 and the predetermined position is large; therefore, the motor 17 runs at a high speed initially and then runs at gradually decreasing speeds.

As is clear from the waveforms shown in Fig. 2, the control device produces UP and DOWN signals when the pulse signals ϕ_A changes from a low level to a high level. In this case, however, a phase difference is produced with respect to the position of the controlled member 22 depending upon whether the controlled member 22 is moving in the UP direction or the DOWN direction. This is because, if the controlled member 22 of the positioning device is stopped at a position midway between two neighbouring addresses, the member 22 will move in the UP direction by a slight vibration and in the DOWN direction at the next moment. Thus UP signals and DOWN signals are generated alternately within very short periods of time, making it difficult to utilize them. In general, systems are usually controlled by control pulses, the construction being such that it is impossible to utilize the signals generated at

times different from the times of the control pulses and, in addition, if the signals are switched on and off repeatedly within very short periods of time, the subsequent stages cannot respond making it difficult to process information. As shown in Figs. 3 and 4, therefore, the positions occupied by the addresses of the controlled member 22 deviate by a half pitch for both of the cases in which the controlled member 22 moves in the UP direction or in which the controlled member 22 moves in the DOWN direction, and a location at which a DOWN pulse will be produced is set at the middle point between the two locations at which UP pulses will be produced, thereby to prevent the UP and DOWN pulses from being generated alternately by vibration.

A correcting circuit 10 has an inverter NOT 1 for inverting the output signal ϕ_A from the movement detector 18 to produce a signal $\bar{\phi}_A$, and inverter NOT 2 for inverting the output signal ϕ_B to produce a signal $\bar{\phi}_B$, a NAND circuit NAND 1 which receives the signal ϕ_A and the output $\bar{\phi}_B$ of NOT 2 and produces an output I_S , a NAND circuit NAND 2 which receives the signals ϕ_A and ϕ_B and produces an output I_R , a flip-flop 9 which is set by the output I_S of the NAND 1 and which is reset by the output I_R of the NAND 2, and AND circuit AND 1 which receives an output Q of the flip-flop 9 and the output $\bar{\phi}_A$ of NOT 1, and an AND circuit AND 2 which receives an output $\bar{Q}$ of the flip-flop 9 and an output ϕ_A of NOT 2. The output of AND 1 is applied to a carry input terminal Co of the full adder 7, and the output of AND 2 is applied to a carry input terminal Co of the full adder 6.

The digital-to-analog converter 12 (hereinafter referred to as a D/A converter) converts the digital signal $|OA - PA|$ delivered from the selector 8 to an analog signal. An extraction circuit 13 determines the square root of the output voltage of the D/A converter 12. A polarization circuit 14 polarizes the analog signal, obtained as an absolute value through the D/A converter 12, to a positive or a negative signal depending upon whether the controlled member 22 is moving in the DOWN or the UP direction. A subtracting circuit 15 subtracts a voltage generated by the D.C. motor 17 from the output voltage of the polarization circuit 14, and an amplifier circuit 16 drives the controller 19 of the D.C. motor 17.

Referring now to Fig. 2, when the pulse signal ϕ_B has a low level and the pulse signal ϕ_A rises from a low level to a high level, the controlled member 22 is moving in the forward direction, i.e. in the UP direction, and when the pulse signal ϕ_B has a high level and the pulse signal ϕ_A rises from a low level to a high level, the controlled member 22 is moving in the reverse direction, i.e., in the DOWN direction. Therefore, when the controlled

member 22 is moving in the forward direction, the up/down encoder 1 produces an UP signal, and when the controlled member 22 is moving in the reverse direction, the up/down encoder 1 produces a DOWN signal. The UP or DOWN signal is counted by the present address counter 2, and hence, the present address is stored. While the binary signal PA of the counter 2 is fed to the inverter group 4 and the full adder 7, a binary signal CA which shows the object address stored in the object address register 3 is applied to the inverter group 5 and the full adder 6, whereby the sum of $\overline{PA}$ and OA, i.e., $\overline{PA}-OA$ is determined by the full adder 6, the sum of PA and $\overline{OA}$, i.e., $OA-PA$ is determined by the full adder 7, one of the signals $\overline{PA}-OA$ or $OA-PA$ being selected by the positive value selector 8 depending on which is of a positive value, and an absolute value $|OA-PA|$ of the difference of the binary signals corresponding to the object address and the present address is sent to the D/A converter 12.

In finding the difference of binary coded signals corresponding to the object address and the present address, a binary signal showing an address (OA or PA) on one side is inverted by the inverter 4 or 5 and is applied to the full adder 6 or 7, and then the output of the full adder 6 or 7 is inverted by the selector 8, in order to effect the subtraction in the adder 6 or 7.

The difference of binary signals corresponding to the object address and the present address takes a positive value or a negative value depending upon the present position of the controlled member 22, which will be located on either side of the object position. However, at an absolute value and a positive or a negative sign is necessary as data for driving the D.C. motor 17. Therefore, both the value consisting of the present address minus the object address and the value consisting of the object address minus the present address, are found, and whichever one of them has a positive value is produced as data for indicating the absolute value. Whether the difference is of a positive value or a negative value can be detected by the output $\overline{SIGN}$ of the overflow carry terminal C_n of either the full adder 6 or the full adder 7 (full adder 7 according to the embodiment shown in Fig. 1). When the signal PA is greater than the signal OA, in the DOWN direction, the output $\overline{SIGN}$ of the overflow carry terminal C_n of the full adder 7 is at logic level "0", and hence the positive value selector 8 selects the full adder 6 and produces a signal of positive sign to the polarization circuit 14. Conversely, when the signal PA is smaller than the signal OA, in the UP direction, the output $\overline{SIGN}$ has logic level "1", and the output $\overline{SIGN}$ of the overflow carry terminal C_n has logic level "1", and hence the positive value selector 8 selects the full adder 7 and produces a signal

of negative sign to the polarization circuit 14. The polarity of voltage applied to the D.C. motor 17 is determined by the signal $\overline{SIGN}$ which serves as a positive sign or a negative sign, and the value (absolute value) of voltage applied to the D.C. motor 17 is determined by the absolute value $|OA-PA|$.

Let it be supposed that the initial set position of the controlled member 22 lies in A_1 between x_6 and x_7 . Let it further be supposed that the present position of the controlled member is x_0 . When the controlled member 22 is located at x_0 , a binary signal produced by the present address counter 2 is smaller than a binary signal produced by the object address register 3.

A driving voltage V_{D1} is supplied to the D.C. motor 17, and the controlled member 22 moves, starting from x_0 , toward the forward direction depending upon the speed of the D.C. motor 17.

When the controlled member 22 moves to a position x_1 , the movement detector 18 produces a signal ϕ_a , and hence the up/down encoder 1 produces an UP signal to a position a in Fig. 2. In response to the UP signal, the present address counter 2 increases the binary signal by one. As a result, the difference between the binary signal of the counter 2 and the binary signal of the register 3 decreases by 1, and the driving voltage applied to the D.C. motor 17 is decreased from V_{D1} to V_{D2} .

When the controlled member 22 has moved from x_1 to x_3 , the driving voltage applied to the D.C. motor 17 is decreased from V_{D2} to V_{D3} .

When the controlled member 22 has moved from x_3 to x_6 , the binary signal of the counter 2 comes into agreement with the binary signal of the register 3 owing to the UP signal at the position c produced by the up/down encoder 1. The driving voltage V_{D4} applied to the D.C. motor 17 will be zero volts.

Thus, as the controlled member 22 approaches the set position, the driving voltage applied to the D.C. motor 17 is decreased so that the running speed of the D.C. motor 17 is decelerated. As the controlled member 22 reaches the preset position, the D.C. motor 17 halts, being controlled by a driving voltage of zero volts.

The hunting effect of such an operation is prevented by the correcting circuit 10. The hunting effect will now be described with reference to the control circuit shown in Fig. 5 from which the correcting circuit 10 shown in Fig. 1 has been removed and referring to Fig. 6 which shows waveforms of various signals of the control circuit of Fig. 5.

The D.C. motor 17 does not stop immediately due to its moment of inertia. Therefore, the controlled member 22 may move to a position in excess of the predetermined range

A₁.

As the controlled member 22 exceeds the position x_7 , in Fig. 6, the binary signal of the counter 2 becomes greater than the binary signal of the register 3 by one owing to an UP signal at the position d produced by the up/down encoder 1. Therefore, the D.C. motor 17 receives a driving voltage V_{D5} of a polarity opposite to that of the driving voltages V_{D1} to V_{D3} . Thus, the D.C. motor 17 has a driving voltage which causes it to run in the reverse direction.

If the controlled member 22 moves further forward to reach a position x_9 due to the moment of inertia, the D.C. motor 17 has a greater driving voltage V_{D6} of opposite polarity.

When the D.C. motor 17 is stopped after the controlled member 22 has moved to a position x_{10} , the D.C. motor 17 then starts to run in the reverse direction; the controlled member 22 starts to return towards the set position.

Since a phase difference has been given to the UP signal and DOWN signal, and there is no correcting circuit the DOWN signal is not produced even when the controlled member 22 is moving from the position x_9 to the position x_8 .

When the controlled member 22 has returned to the position x_8 , the up/down encoder 1 produces a DOWN signal at a position j . The driving voltage is decreased from V_{D6} to V_{D5} .

Similarly, when the controlled member 22 has returned to the position x_6 , the driving voltage is decreased from V_{D5} to zero volts due to the DOWN signal. Hence, the D.C. motor 17 has the driving voltage V_{D5} for running in the reverse direction even after the controlled member 22 has returned to near the centre of the initial preset range.

The controlled member 22 which has returned to the position x_6 may appear to stop at that position because the driving voltage is zero volts. In practice, however, there is a time deviation between the detection of movement and the control of driving voltage, and the time by which the D.C. motor 17 is changed from the accelerating state to the decelerating state lags behind the actual movement of the controlled member 22, resulting in an excess return.

Therefore, as the controlled member 22 returns in excess of the position x_4 , the D.C. motor 17 has the driving voltage V_{D3} for running in the forward direction.

The phase difference between the UP signal and the DOWN signal and the lag in time give rise to the occurrence of hysteresis characteristics with respect to the position of the controlled member. The controlled member develops hunting, i.e., repeats the movement among the positions

$x_5 \rightarrow x_7 \rightarrow x_8 \rightarrow x_4 \rightarrow x_5 \rightarrow x_7 \rightarrow x_8 \rightarrow x_4$. This is a

cause of vibration of the apparatus.

According to the present invention as shown in Fig. 1, a correcting signal for decreasing the absolute value of the driving voltage is obtained by the correcting circuit 10 prior to the UP signal or DOWN signal produced in the next cycle by utilizing an output signal of the movement detector 18. The correcting signal makes it possible to substantially remove the hysteresis characteristics in the driving voltage applied to the D.C. motor 17.

Referring again to Figs. 1 and 2, the correcting circuit 10 will be described.

In this circuit, the inverse signal I_s of the pulse signal $\phi_A \cdot \phi_B$ is produced by the NAND circuit 1 while the inverse signal I_R of the pulse signal $\phi_A \cdot \phi_B$ is produced by the NAND circuit 2. The flip-flop 9 is set by the signal I_s and is reset by the signal I_R . When the pulse signal ϕ_A has a low level, the output O_1 and O_2 of the flip-flop 9 are applied to the carry terminal Co of the full adder 6 and to the carry terminal Co of the full adder 7, respectively.

As described above, the hunting effect occurs due to the hysteresis characteristics or from the deviation of position at which the driving signal for UP movement is produced and position at which the driving signal for DOWN movement is produced, or from the deviation between the object address during the UP movement and the object address during the DOWN movement. The hunting effect can be prevented if the hysteresis characteristics are eliminated. For this purpose, the command voltages should be increased by one logic level between x_0 and x_1 , between x_2 and x_3 , and between x_4 and x_5 in Fig. 6, and the command voltages should be decreased by one logic level between x_6 and x_7 , between x_8 and x_9 , between x_{10} and x_{11} , and between x_{12} and x_{13} .

In effect, when the controlled member 22 is moving in the UP direction, a pulse I_s is generated. Then, when the pulse signal ϕ_A has a low level after the pulse I_R has been generated, the command voltage should be increased by one logic level (a voltage corresponding to a given address). When the controlled member 22 is moving in the DOWN direction, the pulse I_R is generated. Then, when the pulse signal ϕ_A has a low level after the pulse I_s has been generated, the command voltage should be decreased by one logic level.

Depending upon whether the pulses have arrived in the order of pulse I_s then pulse I_R , or in the order of pulse I_R then pulse I_s , the NAND circuits 1 and 2, and flip-flop 9 determine whether the level should be increased or decreased while the pulse signal ϕ_A has a low level. When the pulse signal ϕ_A has a low level, the AND circuits 1 and 2 send the output of the flip-flop 9 to the carry terminals

Co of the full adders 6 and 7. When a signal of logic level "1" is applied to the carry terminal Co of the full adder 6, the output of the full adder 6 is increased by one so that the level is increased by one logic level. When a signal of logic level "1" is applied to the carry terminal Co of the full adder 7, however, the logic level is decreased by one logic level even if the output of the full adder 7 is increased by one because the full adder 7 performs the calculation $0A-PA$.

Thus, when the signal I_s is produced first, and then the signal I_R is produced, the flip-flop 9 is set by the signal I_s and is reset by the signal I_R , whereby the output $\bar{Q}$ has a logic level of "0" and the output Q has a logic level of "1". Thereafter, when the pulse signal ϕ_A has a low level, the output Q is allowed to pass through the AND circuit 2 and is applied as the signal O_1 to the carry terminal Co of the full adder 7, such that the output is increased by one logic level. Conversely, when the signal I_R is produced and then the signal I_s is produced, the flip-flop is reset by the signal I_R and is set by the signal I_s , and hence the output Q has a logic level of "0" and the output $\bar{Q}$ has a logic level of "1". Thereafter, when the pulse signal ϕ_A is of the low level, the output $\bar{Q}$ is applied as the signal O_2 to the carry terminal Co of the full adder 6 via the AND circuit 2, such that the output is decreased by one logic level.

As a result, no hysteresis remains in the waveforms of command voltages as shown at V_D in Fig. 2.

Hence, the UP direction or the DOWN direction is determined by the flip-flop 9 which is set by the output I_s and which is reset by the output I_R . The output is then increased or decreased by one logic level by sending a signal to the carry terminal Cn of either one of the two full adders 6 or 7 while the pulse signal ϕ_A has a logic level of "0" (this is a timing necessary for increasing or decreasing the logic level by one). It is, therefore, made possible to obtain command signals without hysteresis, preventing vibration from being developed. The output of the AND circuit 1 of the embodiment described can be modified so that it can be added as an analog addition voltage to the D/A converter. Similarly, the output of the AND circuit 2 can be added as an analog subtraction voltage to the D/A converter.

CLAIMS

1. A control circuit for a positioning device for moving a controlled member to a predetermined position by using a D.C. motor including:

(a) encoder means for receiving first and second repeated pulse signals being produced corresponding to each movement of said controlled member by a predetermined unit distance and becoming opposite phases depend-

ing upon the direction of movement of said controlled member, and for producing a first trigger signal in response to said first and second repeated signals, when said first repeated pulse signal has a phase preceding the phase of the second repeated pulse signal in a first direction of movement of said controlled member and a second trigger signal in response to said first and second repeated signals when said first repeated pulse signal has a phase lagging behind the phase of said second repeated pulse signal in a second direction of movement of said controlled member opposite to said first direction, said first and second trigger signals having different phases from each other

(b) counter means for receiving said first and second trigger signals depending upon the direction of movement of said controlled member, and for producing a binary coded signal in response to the position of said controlled member;

(c) memory means for providing a predetermined binary coded signal corresponding to the predetermined position;

(d) arithmetic circuit means for producing a difference binary coded signal representing the difference between the binary coded signals of said counter means and said memory means;

(e) driving circuit means for driving the D.C. motor coupled to said controlled member, said driving circuit means producing a driving signal of a level corresponding to the difference binary coded signal of said arithmetic circuit means;

(f) correcting circuit means for receiving said first and second repeated pulse signals and for producing a correcting pulse signal preceding occurrence of one of said first and second trigger signals in the corresponding one of said first and second directions of movement of said controlled member; and

(g) connection means for providing said correcting pulse signal to said arithmetic circuit means so as to cause said difference binary coded signal between the binary coded signals of said counter means and said memory means to be smaller than it would have been without the correcting pulse signal to reduce hunting, whereby the level of the driving signals in said driving circuit means is decreased by said correcting signal.

2. A control circuit of a positioning device according to Claim 1, wherein said correcting circuit means includes a flip-flop circuit set by said first repeated pulse signal and reset by said second repeated pulse signal, and a gate circuit receiving one of said first and second repeated pulse signals as a gate signal and transferring the output of said flip-flop circuit.

3. A control circuit of a positioning device according to Claim 2, wherein said connection means transfers the output of said flip-flop circuit to a carry terminal of said arithmetic



Co of the full adders 6 and 7. When a signal of logic level "1" is applied to the carry terminal Co of the full adder 6, the output of the full adder 6 is increased by one so that the level is increased by one logic level. When a signal of logic level "1" is applied to the carry terminal Co of the full adder 7, however, the logic level is decreased by one logic level even if the output of the full adder 7 is increased by one because the full adder 7 performs the calculation $\bar{O}A-PA$.

Thus, when the signal I_s is produced first, and then the signal I_R is produced, the flip-flop 9 is set by the signal I_s and is reset by the signal I_R , whereby the output $\bar{Q}$ has a logic level of "0" and the output Q has a logic level of "1". Thereafter, when the pulse signal ϕ_A has a low level, the output Q is allowed to pass through the AND circuit 2 and is applied as the signal O_1 to the carry terminal Co of the full adder 7, such that the output is increased by one logic level. Conversely, when the signal I_R is produced and then the signal I_s is produced, the flip-flop is reset by the signal I_R and is set by the signal I_s , and hence the output Q has a logic level of "0" and the output $\bar{Q}$ has a logic level of "1". Thereafter, when the pulse signal ϕ_A is of the low level, the output $\bar{Q}$ is applied as the signal O_2 to the carry terminal Co of the full adder 6 via the AND circuit 2, such that the output is decreased by one logic level.

As a result, no hysteresis remains in the waveforms of command voltages as shown at V_D in Fig. 2.

Hence, the UP direction or the DOWN direction is determined by the flip-flop 9 which is set by the output I_s and which is reset by the output I_R . The output is then increased or decreased by one logic level by sending a signal to the carry terminal Cn of either one of the two full adders 6 or 7 while the pulse signal ϕ_A has a logic level of "0" (this is a timing necessary for increasing or decreasing the logic level by one). It is, therefore, made possible to obtain command signals without hysteresis, preventing vibration from being developed. The output of the AND circuit 1 of the embodiment described can be modified so that it can be added as an analog addition voltage to the D/A converter. Similarly, the output of the AND circuit 2 can be added as an analog subtraction voltage to the D/A converter.

CLAIMS

1. A control circuit for a positioning device for moving a controlled member to a predetermined position by using a D.C. motor including:

(a) encoder means for receiving first and second repeated pulse signals being produced corresponding to each movement of said controlled member by a predetermined unit distance and becoming opposite phases depend-

ing upon the direction of movement of said controlled member, and for producing a first trigger signal in response to said first and second repeated signals, when said first repeated pulse signal has a phase preceding the phase of the second repeated pulse signal in a first direction of movement of said controlled member and a second trigger signal in response to said first and second repeated signals when said first repeated pulse signal has a phase lagging behind the phase of said second repeated pulse signal in a second direction of movement of said controlled member opposite to said first direction, said first and second trigger signals having different phases from each other

(b) counter means for receiving said first and second trigger signals depending upon the direction of movement of said controlled member, and for producing a binary coded signal in response to the position of said controlled member;

(c) memory means for providing a predetermined binary coded signal corresponding to the predetermined position;

(d) arithmetic circuit means for producing a difference binary coded signal representing the difference between the binary coded signals of said counter means and said memory means;

(e) driving circuit means for driving the D.C. motor coupled to said controlled member, said driving circuit means producing a driving signal of a level corresponding to the difference binary coded signal of said arithmetic circuit means;

(f) correcting circuit means for receiving said first and second repeated pulse signals and for producing a correcting pulse signal preceding occurrence of one of said first and second trigger signals in the corresponding one of said first and second directions of movement of said controlled member; and

(g) connection means for providing said correcting pulse signal to said arithmetic circuit means so as to cause said difference binary coded signal between the binary coded signals of said counter means and said memory means to be smaller than it would have been without the correcting pulse signal to reduce hunting, whereby the level of the driving signals in said driving circuit means is decreased by said correcting signal.

2. A control circuit of a positioning device according to Claim 1, wherein said correcting circuit means includes a flip-flop circuit set by said first repeated pulse signal and reset by said second repeated pulse signal, and a gate circuit receiving one of said first and second repeated pulse signals as a gate signal and transferring the output of said flip-flop circuit.

3. A control circuit of a positioning device according to Claim 2, wherein said connection means transfers the output of said flip-flop circuit to a carry terminal of said arithmetic



circuit means through said gate circuit.

4. A control circuit for a positioning device substantially as herein described with reference to, and as illustrated in Figs. 1 and 3 of the accompanying drawings.
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