SLIP FREE VERTICAL RACK DESIGN

BACKGROUND OF THE INVENTION

The manufacture of semiconductor devices such as integrated circuits (IC's) typically requires heat treating silicon wafers in the presence of reactive gases. During this process, the temperatures and gas concentrations to which the devices are exposed must be carefully controlled, as the devices often include circuitry elements less than 1 um in size which are sensitive to minute variations in the processing environment.

The semiconductor manufacturing industry typically processes the wafers in either horizontal or vertical carriers. The horizontal carrier, typically called a "boat", has three or four horizontally disposed bars arranged in a semicircle design, with each bar having inwardly facing grooves set therein at regular intervals. Each set of grooves define a vertical space for carrying a vertically disposed wafer.

The vertical carrier, typically called a "vertical rack", has three or four vertically disposed rods arranged in a semicircle design, with each post having slots set therein at regular intervals to define a space for carrying a horizontally disposed wafer. A conventional vertical rack is shown in Figure 1. This rack typically has a top plate, a bottom plate, and three or four posts for fixing the top plate to the bottom plate. The portions of the post between each slot, termed "teeth", are identically spaced in order to support wafers at regular intervals from and parallel to the bottom plate. The entire rack is then placed within a vertical furnace for processing the wafers. Because a wafer processed on a vertical rack experiences less of a temperature gradient over its face, semiconductor manufacturers are increasingly turning to vertical furnaces. There is, however, a drawback to vertical furnacing. As shown in prior art Figure 1, the wafers disposed on a conventional vertical rack are supported at their outside edge only. As such, the areas of the wafer resting on these teeth experience higher stress than the rest of the wafer. When temperatures in the furnace exceed about 1000°C, these stresses often become significant and portions of the single crystal wafer move relative to each other along crystallographic plates in

response to that stress. This phenomenon, called "slip", effectively destroys the value of the semiconductor devices located in the area of the wafer where slip has occurred.

U.S. Patent No. 5,492,229 discloses a vertical rack design having near center support. However, the first embodiment of this design must either be made by either joining silica components (which are susceptible to high temperatures) or using a water jet to make an interior slit (which is inconvenient). The second embodiment of this design can be made solely by using a more convenient diamond saw, but requires curved vertical supports which cast large shadows upon the wafer.

Therefore, there is a need for a vertical rack design which alleviates slip, is resistant to high temperatures, can be made with a diamond saw, and does not cast a large shadow upon the wafer.

SUMMARY OF THE INVENTION

In accordance with the present invention, there is provided a vertical rack for supporting a plurality of semiconductor wafers in a spaced, substantially horizontal, parallel relation, the vertical rack comprising:

a) a vertical support means, and

b) a plurality of vertically spaced, horizontal support means extending substantially horizontally from the vertical support means to define a plurality of support levels for supporting the wafers,

wherein the horizontal support means are projections, each projection comprising an arm terminating in a wafer platform such that the innermost contact between at least one wafer platform of each support level and its supported wafer is in the region of between 20% and 80% of the wafer radius, measured from the edge of the wafer, and

wherein the arm projects at a continuous upward incline and terminates in the wafer platform.

Also in accordance with the present invention, there is provided a vertical rack for supporting a plurality of semiconductor wafers in a spaced, substantially horizontal, parallel relation, the vertical rack comprising:

a) a vertical support means, and

This Sheet Has Been Replaced

b) a plurality of vertically spaced, horizontal support means extending substantially horizontally from the vertical support means to define a plurality of support levels for supporting the wafers,

wherein the horizontal support means are projections projecting horizontally to continuously contact the wafer from the wafer edge such that the innermost contact between at least one of the arms at each support level and its supported wafer is in the region between 20% and 80% of the wafer radius, measured from the wafer radius.

In some embodiments, the vertical rack comprises:

a) a top plate,

b) a bottom plate, and

c) a plurality of vertical rods, the upper end of each rod being fixed about the periphery of the top plate and the lower end of each rod being fixed about the periphery of the bottom plate, each of the rods having a plurality of projections spaced equidistantly from the bottom plate to define a plurality of support levels for horizontally supporting the wafers,

wherein the innermost contact between at least one of the projections of each support level and its supported wafer is in the region of between 20% and 80% of the wafer radius, measured from the edge of the wafer.

In a first preferred embodiment (as in Figure 2), each projection comprises an arm terminating in a wafer platform and the wafers are supported solely by the wafer platforms. The innermost contact between each wafer platform and the supported wafer is in the region of between 20% and 80% of the wafer radius, measured from the edge of the wafer. Preferably, the arm projects at a continuous upward incline and the wafer platform is horizontal. More preferably, the projections are oriented in such a manner that the rods cast a shadow upon no more than 30% of the wafer, most preferably no more than 10% of the wafer.

In a second preferred embodiment (as in Figure 3), each projection consists of an arm projecting horizontally to continuously contact the wafer from the wafer edge such that the innermost contact between the arm and the wafer is in the region between 20% and 80% of the wafer radius, measured from the wafer

This Sheet Has Been Replaced

radius. Preferably, the projections are oriented in such a manner that the rods cast a shadow upon no more than 30% of the wafer, most preferably no more than 10% of the wafer.

DESCRIPTION OF THE FIGURES

Figure 1 is a conventional vertical rack design.

Figure 2 is a top view and a side view of a vertical rack of the present invention having projections comprising an arm terminating in a wafer platform.

Figure 3 is a top view and a side view of a vertical rack of the present invention having horizontal arms.

Figure 4 depicts the shadow produced by the rods of Figures 2 and 3 upon a typical wafer.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to Figure 2, there is provided a vertical rack 1 for processing semiconductor wafers W comprising:

a) a top plate 2,

b) a bottom plate 3 , and

c) a plurality of vertical rods 4, the upper end 5 of each rod being fixed about the periphery of the top plate 2 and the lower end 6 of each rod being fixed about the periphery of the bottom plate 3, each of the rods having a plurality of projections 7 spaced equidistantly from the bottom plate 3 to define a plurality of support levels for horizontally supporting the wafers W,

wherein each projection 7 comprises an arm 8 terminating in a wafer platform 9 such that the innermost contact between the wafer platform and the wafer is in the region of between 20% and 80% of the wafer radius, measured from the edge of the wafer.

Preliminary testing of the design shown in Figure 2 has shown that it solves the slip problem. Without wishing to be tied to a theory, it is believed that providing only peripheral edge-support to a wafer (as in Figure 1) causes significant stresses which contribute to slip. The present invention (as embodied in Figure 2) mitigates the stresses by providing support closer to the center of the wafer.

The continuous incline of the first embodiment is typically between about 0.5 and about 10 degrees from the horizontal. The wafer platform of this embodiment is typically positioned to contact the wafer such that the innermost contact between at

This Sheet Has Been Replaced



least one and preferably each of at least three of the wafer platforms and their supported wafer is in the region of between 20% and 80% of the wafer radius (measured from the edge of the wafer), and preferably between 33% and 66% of the wafer radius. The total surface area of the wafer platforms at one support level is typically between about 0.02% and about 1% of the surface area of the wafer.

Referring now to Figure 3, there is provided a vertical rack 11 for processing semiconductor wafers comprising:

a) a top plate 12,

b) a bottom plate 13 , and

c) a plurality of vertical rods 14, the upper end 15 of each rod being fixed about the periphery of the top plate 12 and the lower end 16 of each rod being fixed about the periphery of the bottom plate 13, each of the rods having a plurality of projections 17 spaced equidistantly from the bottom plate 13 to define a plurality of support levels for horizontally supporting the wafers W,

wherein each projection 17 consists of an arm projecting horizontally to continuously contact the wafer W from the wafer edge such that the innermost contact between the arm and the wafer is in the region between 20% and 80% of the wafer radius, measured from the wafer radius.

The embodiment of the present invention described by Figure 3 differs from that of Figure 2 in that its arms are horizontal. Since horizontal arms require less vertical space than inclined arms, more wafers can be processed in a rack having this design than in a rack of similar height having inclined arms. Moreover, this rack is easier to construct because it does not require a separate machining step to make the wafer platform of the inclined arm embodiment.

In the second preferred embodiment, the innermost contact between at least one and preferably each of at least three of the arms and their supported wafer is in the region of between about 20% and 80%, and preferably between 33% and 66% of the wafer radius. Moreover, the total contact area between the arms at one support level and their supported wafer is typically between about 1% and about 5% of the surface area of the wafer.

This Sheet Has Been Replaced

To minimize slip-inducing stress, the surfaces of the projections upon which the wafers rest (i.e., either the wafer platforms or horizontal arms) should be both coplanar and smooth. For example, the surfaces of the projections at a support level should be coplanar to within about 0.05 mm as defined in Section 6.5.6 of ASME National Standard Y14.5M-1994. Each should be smooth to within about 1 micron (um) R_a, as defined by Section 3.9.1 of ANSI/ASME National Standard B46.1-1985.

The distance which the projections typically extend from the rod of the vertical rack (found by measuring the shortest distance between the end of the projection and the rod and shown as "A" in Figure 3) is generally dependent upon the size of the wafer to be processed. For example, when the wafer to be processed has a 150 mm diameter, the projections typically extend at least 17 mm, usually between about 22 mm and about 42 mm, and preferably about 29 mm. When the wafer to be processed has a 200 mm diameter, the projections typically extend at least 24 mm, usually between about 32 mm and about 52 mm, and preferably about 38 mm. When the wafer to be processed has a 300 mm diameter, the projections typically extend at least 32 mm, usually between about 42 mm and about 72 mm, and preferably about 56 mm.

The vertical rack of the present invention can be made from any material commonly used in the high temperature production of vertical racks for semiconductor processing, preferably recrystallized silicon carbide. The rack material may also be CVD coated with refractory materials such as silicon carbide, silicon nitride or diamond. Preferably, the rack comprises CRYSTAR, a recrystallized silicon carbide available from the Norton Company of Worcester, MA.

It has been observed that the rods of vertical racks typically shield, or "shadow", radiant heat and/or reactive gases (which enter from the periphery of the vertical furnace) from the portions of the wafer inside of and adjacent to the posts. Accordingly, significant variations in temperature and/or gas concentration between the "shadowed" portion of the wafer and the rest of the wafer are produced. These variations contribute to slip-inducing stress. Therefore, in some embodiments, the projections are radially oriented such that the rods cast a shadow on no more than 30% of the wafer, preferably no more than

This Sheet Has Been Replaced

10% of the wafer. For the purposes of the present invention, the shadow percentage is calculated by determining the percentage of the wafer face to which reactant gases and/or heat can directly radially proceed from the rack periphery in a path unobstructed by the rods. The shaded portion of Figure 4b represents the shadow produced by the rods of Figures 2a and 3a upon the wafers.

This Sheet Has Been Replaced

Claims

1. A vertical rack for supporting a plurality of semiconductor wafers in a spaced, substantially horizontal, parallel relation, the vertical rack comprising:
a) a vertical support means, and
b) a plurality of vertically spaced, horizontal support means extending substantially horizontally from the vertical support means to define a plurality of support levels for supporting the wafers,
wherein the horizontal support means are projections, each projection comprising an arm terminating in a wafer platform such that the innermost contact between at least one wafer platform of each support level and its supported wafer is in the region of between 20% and 80% of the wafer radius, measured from the edge of the wafer, and
wherein the arm projects at a continuous upward incline and terminates in the wafer platform.

2. The rack of claim 1 wherein the innermost contact between each of at least three wafer platforms of each support level and their supported wafer is in the region of between 20% and 80% of the wafer radius, measured from the edge of the wafer.

3. The rack of claim 1 wherein the innermost contact between at least one wafer platform of each support level and its supported wafer is in the region of between 33% and 66% of the wafer radius, measured from the edge of the wafer.

4. The rack of claim 1 wherein the innermost contact between each of at least three wafer platforms of each support level and their supported wafer is in the region of between 33% and 66% of the wafer radius, measured from the edge of the wafer.

5. The rack of claim 1 wherein the wafer platform is horizontal.

6. The rack of claim 1 wherein the vertical support means are rods and the rods cast a shadow upon no more than 30% of the wafer.

7. The rack of claim 6 wherein the rods cast a shadow upon no more than 10% of the wafer.

This Sheet Has Been Replaced

8. The rack of claim 1 wherein each wafer platform has a roughness (R_a) of about 1 um.

9. The rack of claim 1 wherein the wafer platforms of each support level are coplanar within about 0.05 mm.

10. The rack of claim 1 wherein the total contact area between the wafer platforms of a support level and their support wafer is between about 0.02% and about 1% of the surface area of the wafer.

11. The rack of claim 1 comprising recrystallized silicon carbide.

12. The rack of claim 1 coated with CVD silicon carbide.

13. A vertical rack for supporting a plurality of semiconductor wafers in a spaced, substantially horizontal, parallel relation, the vertical rack comprising:

a) a vertical support means, and

b) a plurality of vertically spaced, horizontal support means extending substantially horizontally from the vertical support means to define a plurality of support levels for supporting the wafers,

wherein the horizontal support means are projections projecting horizontally to continuously contact the wafer from the wafer edge such that the innermost contact between at least one of the arms at each support level and its supported wafer is in the region between 20% and 80% of the wafer radius, measured from the wafer radius.

14. The rack of claim 13 wherein the innermost contact between each of at least three of the arms at each support level and their supported wafer is in the region between 20% and 80% of the wafer radius, measured from the wafer radius.

15. The rack of claim 13 wherein the innermost contact between at least one arm of each support level and its supported wafer is in the region between 33% and 66% of the wafer radius, measured from the wafer radius.

16. The rack of claim 13 wherein the innermost contact between each of at least three arms at each support level and their supported wafer is in the region between 33% and 66% of the wafer radius, measured from the wafer radius.

This Sheet Has Been Replaced

17. The rack of claim 13 wherein the vertical support means are rods and the rods cast a shadow upon no more than 30% of the wafer.

18. The rack of claim 17 wherein the rods cast a shadow upon no more than 10% of the wafer.

19. The rack of claim 13 wherein the portion of each arm contacting the wafer has a roughness (R_a) of 1 um.

20. The rack of claim 13 wherein the arms of each support level are coplanar within about 0.05 mm.

21. The rack of claim 13 comprising recrystallized silicon carbide.

22. The rack of claim 13 coated with CVD silicon carbide.

23. The rack of claim 13 wherein the total contact area between the arms of a support level and their supported wafer is between about 1% and about 5% of the surface area of the wafer.

24. A process comprising the steps of:
a) placing a plurality of wafers onto the projections of the vertical rack of claim 1, and
b) processing the wafers at a temperature above about 1000°C.

This Sheet Has Been Replaced

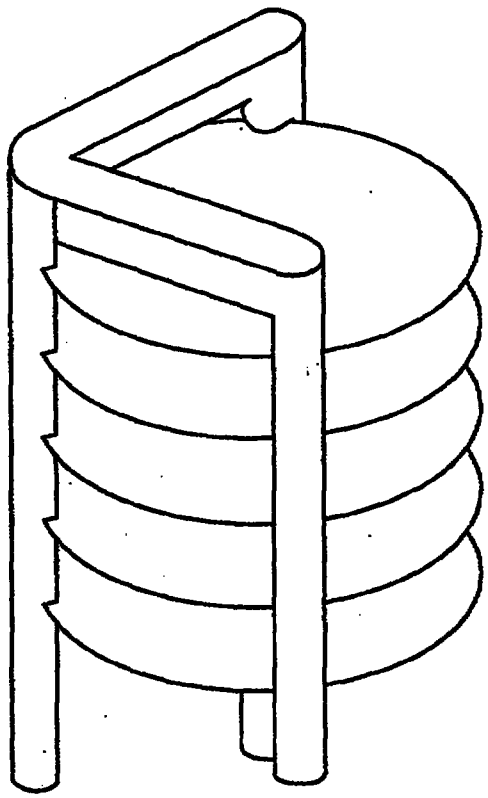


FIG. 1

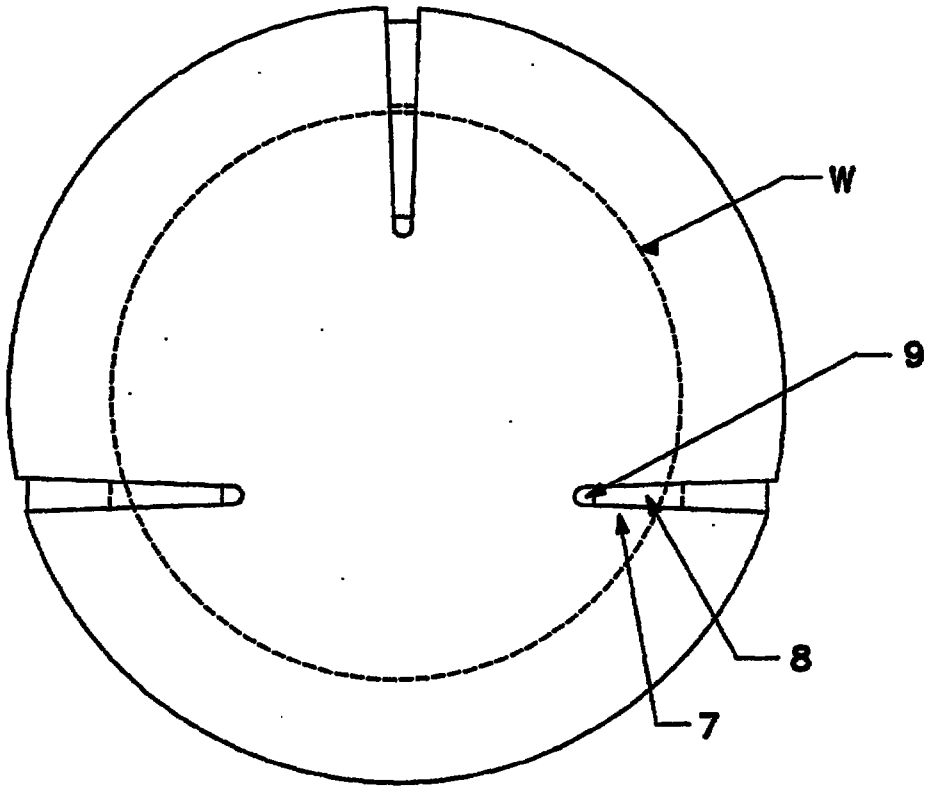


FIG. 2a

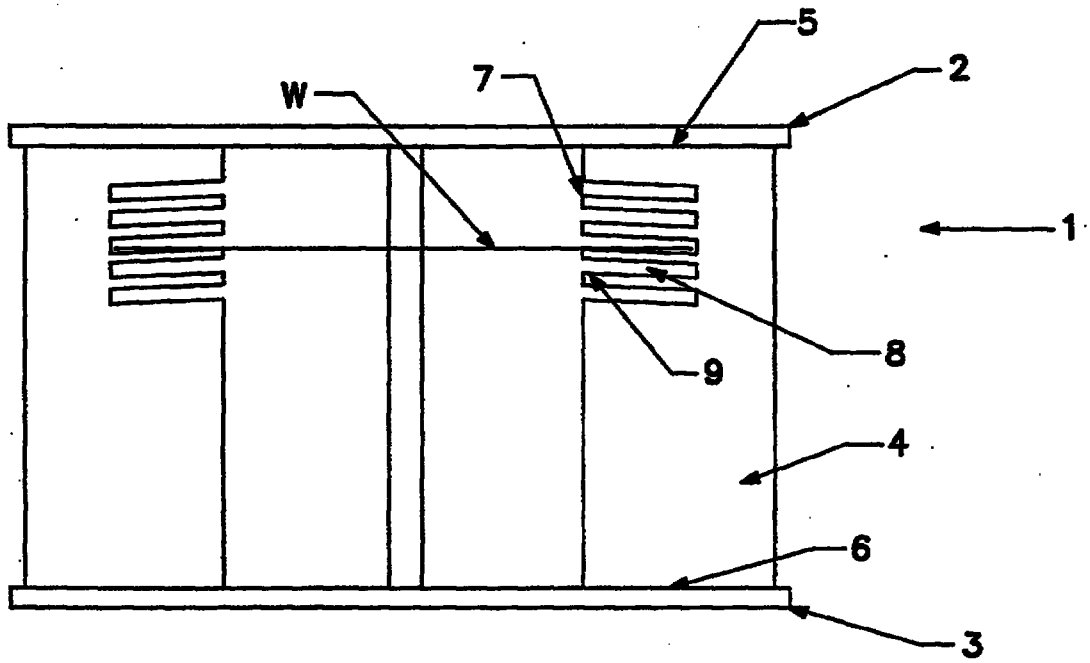


FIG. 2b

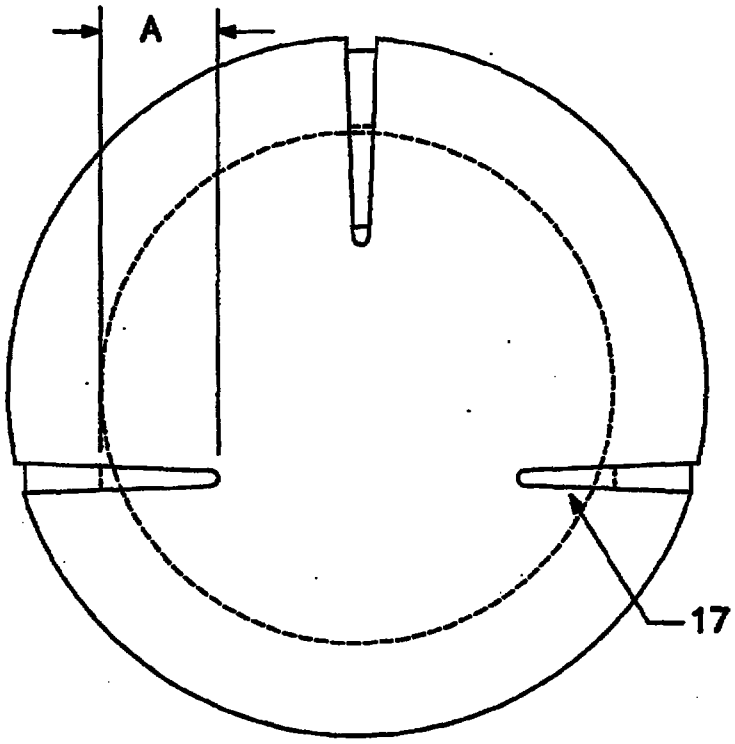


FIG. 3a

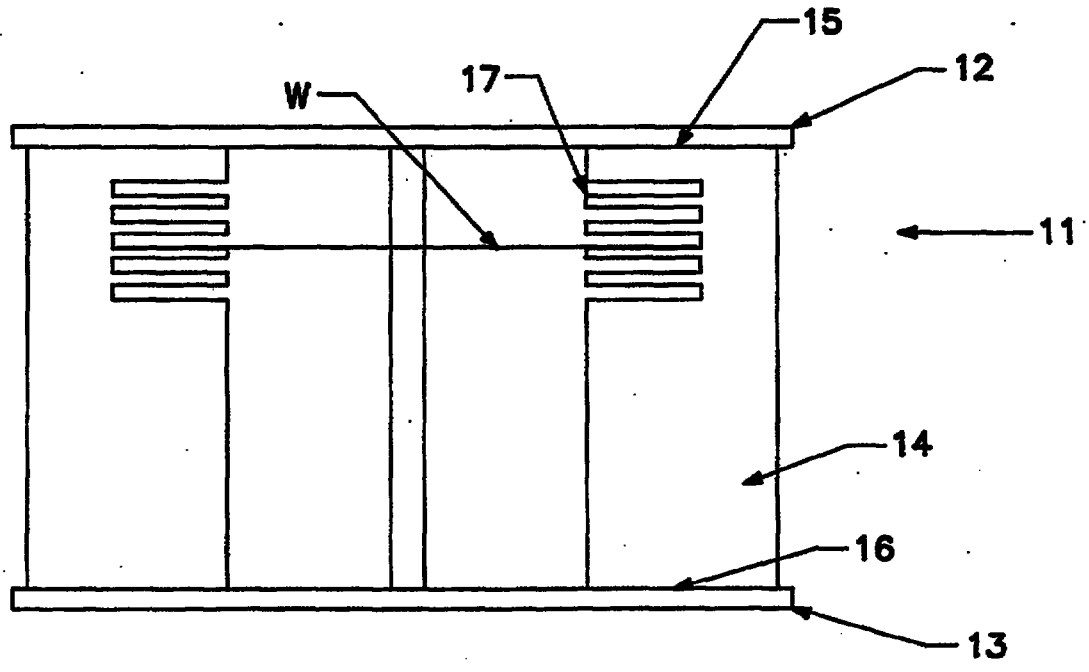


FIG. 3b

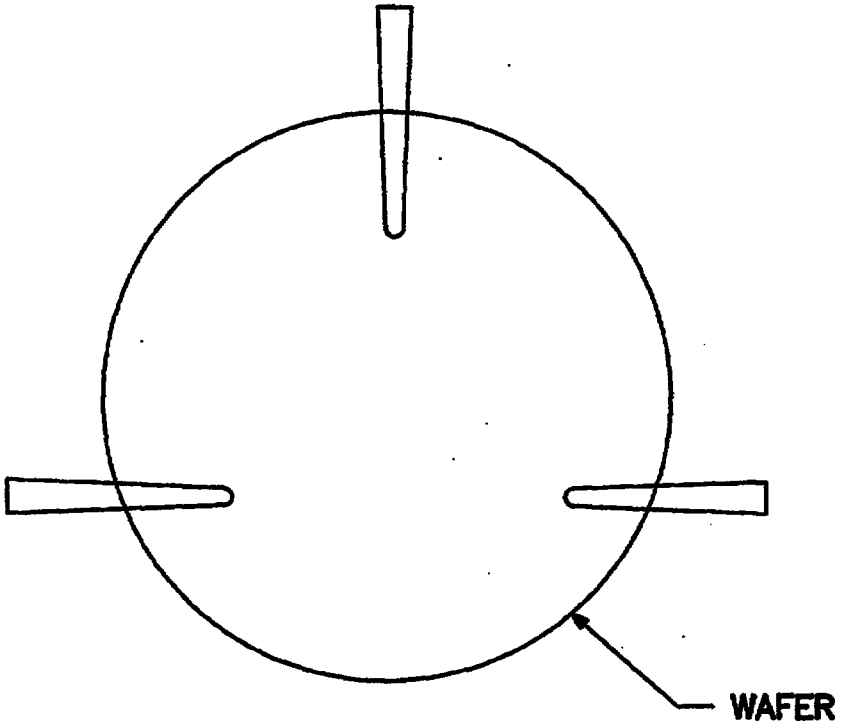


FIG. 4a

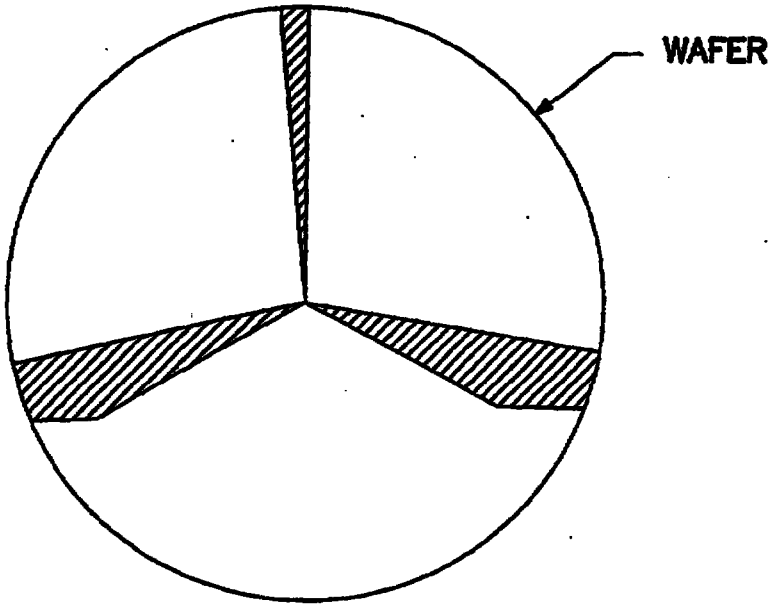


FIG. 4b

9705173-4 IPOS

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6: H01L 21/00 — A1

(11) International Publication Number: WO 96/35228

(43) International Publication Date: 7 November 1996 (07.11.96)

(21) International Application Number: PCT/US96/06294

(22) International Filing Date: 3 May 1996 (03.05.96)

(30) Priority Data:
08/435,931 — 5 May 1995 (05.05.95) — US

(71) Applicant *(for all designated States except US)*: SAINT-GOBAIN/NORTON INDUSTRIAL CERAMICS CORPORATION [US/US]; 1 New Bond Street, P.O. Box 15138, Worcester, MA 01615-0138 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: TOMANOVICH, John, A. [US/US]; 6 Briarcliff Lane, Paxton, MA 01612 (US).

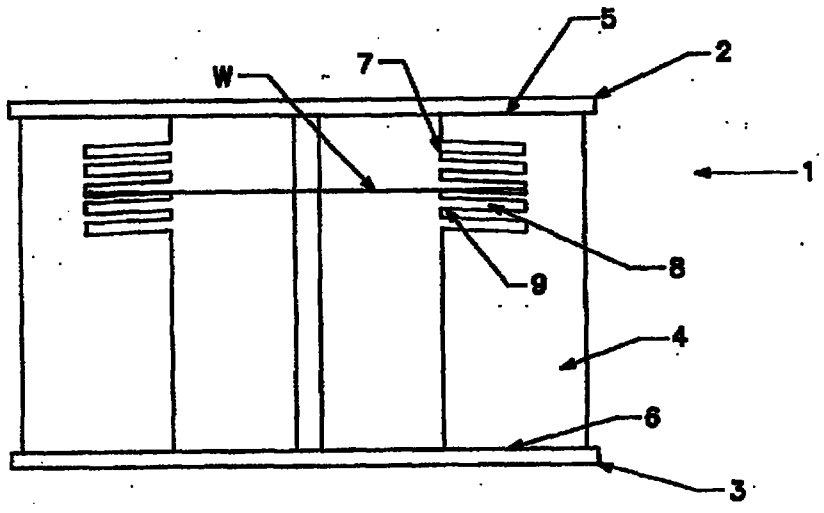
(74) Agents: DIMAURO, Thomas, M. et al.; Saint-Gobain Corporation, 1 New Bond Street, P.O. Box 15138, Worcester, MA 01615-0138 (US).

(81) Designated States: CA, CN, JP, KR, MX, SG, US, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

REPLACED SHEETS SG
Description : paged ...2... to paged ...7.....
Claim(s) : paged ...8... to paged ...10.....
Drawing(s) : paged ..... to paged .....
Abstract : paged ..... to paged .....
DATE OF RECEIPT .....

(54) Title: SLIP FREE VERTICAL RACK DESIGN



(57) Abstract

The present invention relates to a vertical rack for supporting a plurality of semiconductor wafers in a spaced, substantially horizontal, parallel relation, the vertical rack comprising: a) a vertical support means, and b) a plurality of vertically spaced, horizontal support means extending substantially horizontally from the vertical support means to define a plurality of support levels for supporting the wafers, wherein the horizontal support means are projections, each projection comprising an arm terminating in a wafer platform such that the innermost contact between at least one wafer platform of each support level and its supported wafer is in the region of between 20 % and 80 % of the wafer radius, measured from the edge of the wafer, and wherein the arm projects at a continuous upward incline and terminates in the wafer platform.