

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
8 March 2001 (08.03.2001)

PCT

(10) International Publication Number
WO 01/16960 A1

(51) International Patent Classification⁷: G11C 16/16

(74) Agent: RODDY, Richard, J.; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(21) International Application Number: PCT/US00/23785

(22) International Filing Date: 29 August 2000 (29.08.2000)

(81) Designated States (*national*): CN, JP, KR, SG.

(25) Filing Language: English

(84) Designated States (*regional*): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

(26) Publication Language: English

(30) Priority Data:
09/389,161 2 September 1999 (02.09.1999) US

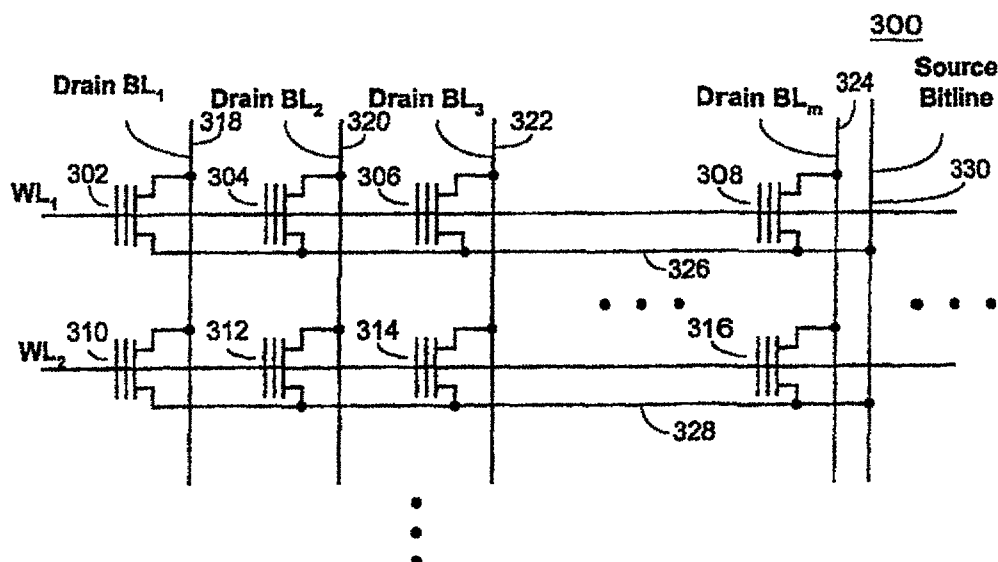
Published:
— With international search report.

(71) Applicant: ADVANCED MICRO DEVICES, INC.
[US/US]; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(72) Inventor: SUNKAVALLI, Ravi; 1901 Halford Avenue
#49, Santa Clara, CA 95051 (US).

(54) Title: 1 TRANSISTOR CELL FOR EEPROM APPLICATION



(57) Abstract: Memory devices having 1-transistor flash memory cells that in one embodiment allows bit-by-bit erase and in other embodiments allows erase of a multi-bit word. The word can be 8 bits, 16 bits, 32 bits, 64 bits or any size word. The memory devices have source bitlines that are connected to the bitline driver that controls the bitlines. The bitline driver and a wordline driver controls the voltages applied to selected bitlines, source bitlines while the wordline driver controls the voltage applied to selected wordlines to allow selected memory cells to be programmed, erased, or read.