

SHIFT REGISTER AND METHOD OF DRIVING THE SAME

ABSTRACT OF THE DISCLOSURE

A clock pulse with a smaller amplitude voltage than the power supply voltage of the shift register is inputted to the shift register. The gate width of a TFT that constitutes a second clocked inverter of the shift register is set wide so as to reduce fluctuation in output electric potential due to leak current of a first clocked inverter. Further, a TFT is added to a first clocked inverter. A signal with an amplitude voltage of the same level as the power supply voltage is inputted to a gate electrode of the added TFT to switch between ON and OFF. The leak current of the first clocked inverter is thus cut off.

(Fig. 1)