its orientation. The term "vertical" refers to a direction perpendicular to the horizontal as just defined. Terms, such as "on", "above", "below", "bottom", "top", "over", and "under", are defined with respect to the horizontal plane. A dual-type leadframe is defined as having at least two rows of lead tips.

Likewise, the drawings showing embodiments of the invention are semi-diagrammatic and not to scale and, particularly, some of the dimensions are for the clarity of presentation and are shown greatly exaggerated in the FIGs. In addition, where multiple embodiments are disclosed and described having some features in common, for clarity and ease of illustration and description thereof like features one to another will ordinarily be described with like reference numerals.

Referring now to FIG. 1, therein is shown a plan view of a half-etched, dual-type leadframe integrated circuit package system 100 in accordance with an embodiment of the present invention. The system 100 includes a leadframe 102 having lead tips 104 in first rows 106 and second rows 108. The input/output (I/O) count as determined by the number of lead tips 104 can be more closely packed than previously possible. Surrounded by the lead tips 104 is a paddle 110. The paddle 110 can use either dimple or groove designs depending on considerations such as thermal cooling, warpage reduction, and increasing the ability to mount die.

The molding compound is not shown and a dotted outline of an integrated circuit chip 112 is shown over the leadframe 102.

The system 100 is singulated from other similar systems along a sawing outline 114 and a sawing inline 116. The system 100 has the bottom of the molding encapsulant and the leadframe having the characteristics of being etched to expose the bottoms of the lead tips 104, which form the terminals for the integrated circuit chip 112. The first rows 106 and second rows 108 are completely surrounded horizontally by a perimeter around the vertical sides of the integrated circuit chip 112.

Referring now to FIG. 2, therein is shown a cross-sectional view of the leadframe 102 of FIG. 1 as initially manufactured. In FIG. 2, a leadframe 200 is a single structure combining lead tips 204 and a paddle 206.

Referring now to FIG. 3, therein is shown a cross-sectional view of the structure of FIG. 2 after further processing. The leadframe 200 has had solder paste 300 deposited on the lead tips 204, and the integrated circuit chip 112 having first and second rows of solder

bumps 302 and 304 thereon has been placed with the bumps pressed into the solder paste 300 on the respective first and second rows of lead tips 106 and 108.

What is claimed is:

1. An integrated circuit package system comprising:

an integrated circuit chip having a first row of bumps;

a dual-type leadframe having a first row of leads and a second row~~s~~ of leads with the first row of leads soldered to the first row of bumps on the integrated circuit chip; and

a molding compound encapsulating the integrated circuit chip, the bumps, the solder, and the leadframe having a bottom of the first row of leads and the second row ~~rows~~ of leads coplanar characteristic of a bottom of the leadframe planarized, and the first row of leads and the second row of leads completely surrounded horizontally by a perimeter around the vertical sides of the integrated circuit chip~~, the leadframe characterized by being planarized at the bottom thereof to separate the first and the second rows of leads~~.

2. The system as claimed in claim 1 wherein ~~the~~ bottoms of the leads ~~are characterized by being etched~~ have an etched finish on the lead tips.

3. The system as claimed in claim 1 further comprising:

a second row of bumps on the integrated circuit chip; and

the dual-type leadframe having the second row of leads soldered to the second row of bumps on the integrated circuit chip.

4. The system as claimed in claim 1 further comprising:

a second integrated circuit chip bonded to the first integrated circuit chip;

a plating layer on the second row of leads; and

wire bonds connecting pads on the second integrated circuit chip to the plating layer on the second row of leads.

5. The system as claimed in claim 4 wherein the wire bonds connect center pads on at least one of the integrated circuit chips to at least one of the rows of leads.

6. The system as claimed in claim 4 further comprising:

~~a second integrated circuit chip bonded to the first integrated circuit chip;~~

a spacer bonded to the second integrated circuit chip;

a third integrated circuit chip bonded to the spacer;

first wire bonds wirebonding the second integrated circuit chip to the second row of leads;

a third row of leads on the leadframe; and

second wire bonds wirebonding the third integrated circuit chip to the third row of leads.