

Description

The present invention relates to a tracking control method and, more particularly, to a tracking control method for use with magnetic tape having a video track and a control track in a magnetic recording and reproduction apparatus, such as a video tape recorder.

In general, household video-tape recorders (referred to as VTRs hereinafter) use rotating magnetic heads for recording and reproducing video signals. These VTRs are provided with a head servo circuit for controlling rotating speed and rotation phase of the heads and a capstan servo circuit for transporting magnetic tape at constant speed at a time of recording and in synchronization with a recorded control signal at a time of reproduction. The control signal is recorded on the tape in synchronization with video signals being recorded. However, control and video heads are different in their mechanisms. Hence the phase relationship between the control signal and the video signal varies according to mounting positions of the control head and the video heads. This variation will cause tracking error which may appear on a TV picture-tube screen at the time of reproduction of video signals.

To keep VTRs compatible, the record phase of the control signal is set up as a standard and is thus adjusted at a stage of manufacture of the VTRs. In the capstan servo circuit, on the other hand, in the case where a phase shift occurs in the recorded control signal, the phase of a reference signal for a phase comparator in the servo circuit is changed by a delay circuit, thereby compensating for the phase shift of the control signal. However, such compensation is performed by a user while watching VTR reproduced pictures on a TV picture-tube screen. That is, to obtain the most pleasant pictures, the user adjusts an externally accessible variable resistor installed to a VTR body, which is called a tracking volume control, while watching the reproduced pictures.

Recently there has been proposed a method of automatically compensating for the phase shift of a control signal described above by a tracking control apparatus using a microcomputer as shown in Fig. 1. A reference signal generator 12 generates a reference signal a for controlling a capstan motor and a head-drum motor described later. The reference signal a is applied to an input port 14₁ of a microcomputer 14 and a monostable multivibrator 16. Control head 18 is adapted to reproduce a control signal from magnetic tape. After being amplified in an amplifier 20, the reproduced control signal is applied to a Schmitt circuit 22. The reproduced control signal c wave-shaped by Schmitt circuit 22 is applied to a phase comparator 24

together with the reference signal b which has been subjected to a predetermined time delay by monostable multivibrator 16. Phase comparator 24 is adapted to make a comparison in phase between the reference signal b and the reproduced control signal c and provide to a mixing amplifier 26 an output signal d which represents the phase difference between both the signals.

An FG coil 28 generates an FG signal proportional to the rotation frequency of capstan motor 30. The FG signal is fed to an amplifier 32 for amplification. The output signal of amplifier 32 is applied to a Schmitt circuit 32 for wave-shaping and then applied to a frequency discriminator 36 as an FG signal e. Frequency discriminator 36 measures the frequency of the FG signal e and applies a speed signal f to mixing amplifier 26 accordingly. Mixing amplifier 26 mixes the phase difference signal d and the speed signal f together to produce a motor control signal g which is fed to a motor drive amplifier 38. Motor drive amplifier 38 amplifies the motor control signal g to provide a signal for rotating capstan motor 30.

A video signal reproduced by a video head 40 is applied to a peak detector 44 via a preamplifier 42, which detects a peak level of the reproduced video signal for application to an A/D conversion input port 14₂ of microcomputer 14.

Microcomputer 14 converts an output of peak detector 44 to a digital signal. A transistor 46 is connected to an output port 14₃ of the microcomputer 14 via a resistor R₁ as shown in Fig. 1.

Monostable multivibrator 16 comprises NAND gates 162, 164, a comparator 166, a transistor 168, a resistor R and a capacitor C forming together a delay circuit, a resistor R₂ and a voltage source V₁. NAND gate 162 has an input connected to reference signal generator 12 and the other input connected to the output of NAND gate 164. NAND gate 164 has an input connected to the output of NAND gate 162 and the other input connected to the output of comparator 166. NAND gate 164 provides reference signal b to phase comparator 24 and to transistor 168 via resistor R₂. Comparator 166 has its noninverting input (+) connected to ground via voltage source V₁ and its inverting input (-) to the junction of resistor R and capacitor C, which is also connected to transistor 46.

In operation, reference signal a generated by reference signal generator 12 at time t₁ as shown in Fig. 2A is applied to microcomputer 14 and monostable multivibrator 16. In monostable multivibrator 16, reference signal a is delayed by the delay circuit formed of resistor R and capacitor C, the delay time depending on a time constant defined by resistance and capacitance values. In response to the trailing edge of reference signal a, transistor 168 in monostable multivibrator 16 is

turned off and output port 14₃ of microcomputer 14 goes high, thereby causing transistor 46 to be turned on as shown in Fig. 2B. The inverting input (-) of comparator 166 thus goes low so that the output thereof becomes high. Therefore the NAND gate 164 goes low as shown in Fig. 2D.

Microcomputer 14 receives the output of peak detector 44 at input port 14₂ and causes output port 14₃ to go high when a peak level is detected with the result that transistor 46 is turned off (time t₂). The time interval between t₁ and t₂ is a delay time for the reproduced signal to attain the maximum level. As a result of transistor 46 being turned off, such a pulse as shown in Fig. 2C is applied to the inverting input (-) of comparator 166. The pulse rises in accordance with the time constant defined by resistor R and capacitor C in the monostable multivibrator 16, thereby causing the output of comparator 166 to go low. Consequently the output of NAND gate 164 goes high at time t₃ as shown in Fig. 2D. Once the output of NAND gate 164 goes high, transistor 168 is turned on, so that the high level output of NAND gate 164 is held until reference signal a next goes low at time t₄ as shown in Fig. 2D.

Thus reference signal b output from NAND gate 164 is kept in sync with the peak level of the reproduced video signal detected by microcomputer 14. Hence the rotation phase of capstan motor 30 is fixed at a time when the peak level is detected, thereby completing the tracking adjustment.

According to the tracking adjustment method described above, however, the operating point of monostable multivibrator 16 is delayed by microcomputer 14. Consequently there arises a problem that synchronizing error occurs because the amount of delay has to be internally generated by microcomputer 14.

Moreover, there is another problem that the connection of microcomputer 14 to the servo system increases the component count and manufacturing cost.

Prior art document EP-A-0 181 186 discloses a tracking control system comprising a capstan motor for moving a magnetic tape which is at least recorded with an FM signal and a control signal having a constant period, a driving circuit for generating a signal which drives the capstan motor, a control head for reproducing the control signal from the tape in a reproducing mode, and heads for reproducing the FM signal from the tape in the reproducing mode. A tracking adjuster generates a comparison signal and a phase comparator compares phases of the reproduced control signal with the comparison signal and generates a phase error signal which is supplied to the driving circuit to control the driving circuit. A sampling circuit sam-

ples a signal which is based on the reproduced FM signal with a present sampling interval, and a discriminating circuit, comprising a microprocessor, discriminates levels of sampled data obtained from the sampling circuit. A circuit generates a control signal based on a discriminated result in the discriminating circuit and supplies the control signal to the tracking adjuster to automatically and variably control a duty cycle of the comparison signal so that an envelope level of the reproduced FM signal becomes a maximum.

It is an object of the present invention to provide a tracking control apparatus which eliminates the synchronizing error for improved tracking accuracy and decreases the component count for reduction in manufacturing cost.

To solve this object the present invention provides a tracking control method as specified in the claim.

The aforementioned aspects and other features of the present invention are explained in the following description, taken in connection with the accompanying drawings in which:

Fig. 1 is a block diagram of a prior art tracking control apparatus;

Figs. 2A through 2D are timing diagrams which are useful in understanding the operation of the prior art tracking control apparatus of Fig. 1;

Fig. 3 is a block diagram of a tracking control apparatus for performing the method of the present invention;

Figs. 4A, and 4B-I and 4B-II are a pin layout and a functional block diagram, respectively, of the microcomputer of Fig. 3; and

Figs. 5 through 8 are flowcharts which are useful in understanding the operation of the tracking control apparatus of Fig. 3, more specifically, Fig. 5 illustrating steps for phase comparison, Fig. 6 illustrating steps for frequency discrimination, Fig. 7 illustrating steps for tracking control and Fig. 8 illustrating steps for capstan motor control.

An embodiment of the present invention will be described below by reference to Figs. 3 through 8 in which like reference characters designate like or corresponding parts in the prior art.

In Fig. 3, reference numeral 50 designates a microcomputer formed of the Toshiba TMP91C642 microprocessor, for example. Its pin layout and internal block diagram are shown in Fig. 4A and Figs. 4B-I and 4B-II, respectively. The microcomputer 50 comprises a central processing unit (CPU) 502 for performing required processing, a timer counter 504 for counting a signal delivered from external reference signal generator 12, latches 506, 508 and 510 which latch values counted by the timer counter 504, an analog-to-digital (A/D) converter 512 for converting an output signal of video

head 40 to a digital value, a digital-to-analog (D/A) converter 514 for converting a signal to be applied to capstan motor 30 to an analog signal, a ROM (read-only memory) 516 and a RAM (random access memory) 518. Various pieces of data can be transferred among these components via a bus line as shown in Fig. 3.

Microcomputer 50 has the construction shown in Figs. 4B-I and 4B-II. As is shown in Figs. 4B-I and 4B-II, CPU (TLCS-90) 502, A/D converter 512, ROM (16K) 516, and RAM (320B) 518 are coupled to one another through a bus line. To this bus line, the following structural elements are also coupled: serial I/O (2ch) 520 through which data is supplied from or to an external device; timer counter (8 Bit, 4 CH/PWM8) 522 having a timer function of counting internal clocks and an event function of counting the number of pulses externally input; V-synchronous controller 524 having a V-separation function of separating a C-synchronous input (from 12P) to a V-Sync. and also a function of determining whether the C-Sync. input is an even-numbered field or an odd-numbered field and whether it is a NTSC or PAL/SECAM (60/50 field); and servo input controller 526 including a D-FG frequency dividing circuit for varying the D-APC sampling, a C-FG frequently dividing circuit for performing the picture search frequency division in accordance with the number which is double the search speed, a C-FG mask counter, and a P-CTL frequency dividing circuit. Further, the following structural elements are coupled to the bus line: PWM output controller (2ch) 528 for controlling the motor by modulating a digital amount into a pulse width (resolution: 12 bits) and deriving an analog voltage by causing the pulse width to pass through a low-pass filter; interrupt controller 530 for controlling the interrupting signal supplied through an external I/O; Index/Address detector 532 for detecting the duty of a reproduced control signal, an index (VHS type), and an address (VHS type); and watchdog timer 534 which includes a timer for detecting an erroneous operation of CPU 502 and which resets CPU 502 after the elapse of a predetermined time.

A 18-bit time base counter 536 is a 18-bit up counter which counts the internal clocks (200 msec at the time of 10 MHz oscillation). This watchdog timer 534 is coupled to both time base counter 538 and programmable timing pulse generator 540 through a bus line, and is further coupled to the above-mentioned bus line. Time base counter 538 is a 24-bit, 8-step element with FIFO. It has a function of latching a counted value at the edge of an externally supplied signal and can measure the period of each input signal on the basis of the latched data. Programmable timing pulse generator 540 is an element of $(16 \text{ bit} + 16 \text{ bit}) \times 2$ and is provided with FIFO. Generator 540 can output

pulses (20 pulses at the maximum) at timings which are synchronous with 18-bit time base counter 536, so that it produces highly accurate timing pulses in synchronism with capture inputs.

Programmable timing pulse generator 540 constitutes reference signal generator 12 shown in Fig. 3, in conjunction with V-Sync. controller 524. Servo input controller 526 is a section where P-CTL signal c' and C-FG signal e' are input. Further, 18-bit time base counter 536 is a section corresponding to timer counter 504, and time base counter 538 is a section corresponding to latches 506, 508 and 510.

Reference numerals 542, 544, 546, 548, 550 and 554 denote input/output ports, reference numeral 552 denotes an input port, reference numeral 556 denotes an output port. Reference numeral 558 denotes an oscillator for generating signals used for the interface of input/output communication.

Reference signal a generated by reference signal generator 12 is applied to CPU 502 and latch 506. A signal reproduced by control head 18 and amplified by amplifier 20 is applied to CPU 502 and latch 508 as a P-CTL signal c' after being subjected to wave-shaping in Schmitt circuit 60. Similarly, an FG signal generated by FG coil 28, which is proportional to the rotating speed of capstan motor 30, is applied to CPU 502 and latch 510 as a C-FG signal e' after amplification in amplifier 32 and subsequent wave-shaping in Schmitt circuit 62.

A video signal reproduced by video head 40 is amplified by preamplifier 42 and then applied to A/D converter 512 via peak detector 44. An output signal of D/A converter 514 is amplified by motor drive amplifier 38 and then applied to capstan motor 30.

The operation of the embodiment will now be described with reference to flowcharts of Figs. 5 through 8.

The control signal reproduced by control head 18 is amplified by amplifier 20 up to a predetermined level and then applied to Schmitt circuit 60. The amplified control signal is wave-shaped by Schmitt circuit 60 to P-CTL signal c' . Here the function of phase comparison will be described. As shown in Fig. 5, P-CTL signal c' and reference signal a generated by reference signal generator 12 arrive at microcomputer 50 (step ST1). Reference signal a is applied to CPU 502 and latch 506 and P-CTL signal c' is applied to CPU 502 and latch 508. Every time reference signal a arrives at microcomputer 50, CPU 502 causes latch 506 to hold the count of timer counter 504 as data representing reference signal's time of arrival at the microcomputer. Similarly, every time P-CTL signal c' arrives at microcomputer 50, CPU 502 causes

latch 508 to hold the count value (data representing P-CTL signal's time of arrival) of timer counter 504 (step ST2). CPU 502 thus reads arrival-time data (counts of the timer counter) from latches 506 and 508 and then writes the arrival-time data (NVP) read from latch 506 into RAM 518 (step ST4). Subsequently CPU 502 calculates the difference between the arrival-time data (NVP) of reference signal a, which has been written into RAM 518, and the arrival-time data (NPCTL) of P-CTL signal c' read from latch 508 (step ST5). This difference corresponds to the phase difference between reference signal a and P-CTL signal c'. The operation of phase comparison is thus achieved.

The FG signal generated by FG coil 28 is amplified by amplifier 32 and then wave-shaped by Schmitt circuit 62. As a result, C-FG signal e' proportional to the rotation frequency of capstan motor 30 is formed. In operation of frequency discrimination, as shown in Fig. 6, upon arrival at microcomputer 50 (step ST6), C-FG signal e' is entered to CPU 502 and latch 510. Every time C-FG signal e' arrives at microcomputer 50, CPU 502 causes latch 510 to hold the count of timer counter 504 (step ST9). Upon arrival of C-FG signal e', CPU 502 reads the arrival-time data of signal e' from latch 510 (step ST8). Subsequently CPU 502 writes the time data read from latch 510 into RAM 518 (step ST9). CPU 502 then calculates the difference between two successive pieces of arrival-time data of C-FG signal e', one of which being now written into RAM 518 and the other of which having been written therein previously (step ST10). In step ST11, CPU 502 calculates the controlled variable in phase of capstan motor 30 from the difference in time data calculated in step ST10. An interval between successive times of arrival of signal C-FG signal e' can be found in this way. CPU 502 detects the frequency of C-FG signal e', thereby achieving the operation of frequency discrimination.

CPU 502 mixes the speed error and the phase error together, which are obtained by the above described operations, in accordance with a predetermined arithmetic operation to produce motor control signal g' which is adapted to rotate capstan motor 30 in predetermined phase and at predetermined speed. Motor control signal g' is converted to an analog signal by D/A converter 514 and then applied to motor drive amplifier 38 for amplification. The amplified motor control signal from motor drive amplifier 38 drives capstan motor 30.

The video signal reproduced by video head 40 is amplified by preamplifier 42 and then applied to peak detector 44. Peak detector 44 detects a peak value of the input video signal, which is entered to microcomputer 50.

The tracking control operation will now be described with reference to Fig. 7. When the peak level of a video signal being reproduced is detected by peak detector 44, the detected peak level is entered to A/D converter 512 (step ST12). CPU 502 reads the peak level of the video signal being reproduced via A/D converter 512 (step ST13). Subsequently CPU 502 calculates the phase controlled variable of motor 30 so that the peak level may become maximum (step ST14).

At the same time, CPU 502 varies the controlled variable of the motor control signal by a predetermined amount in accordance with the amount of phase error obtained by the phase comparison operation in steps ST1 - ST5 (step ST15). CPU 502 then reads, as described above, the peak level of the reproduced video signal after the controlled variable is varied and searches for a point at which the peak level becomes maximum (step ST16). If the point at which the peak level becomes maximum has thus been found, CPU 502 sets the maximum peak level at a desired value (step ST17). CPU 502 varies the controlled variable of the motor control signal so that the desired value may be attained (step ST18). The tracking control is achieved in this way.

Referring to Fig. 8, the control operation of capstan motor 30 is as follows. The speed controlled variable of capstan motor 30 calculated in step ST11 and the phase controlled variable of motor 30 calculated in step ST14 are added together to produce a motor controlled variable (step ST19). The motor controlled variable is subsequently converted to an analog signal by D/A converter 514 for application to motor drive amplifier 38 as motor control signal g, (step ST20). Capstan motor 30 is responsive to the output of motor drive amplifier 38 to rotate at the predetermined phase and the predetermined speed.

According to the tracking control apparatus arranged as above, CPU 502 in microcomputer 50 controls the speed and phase of capstan motor 30 by means of its phase comparison and frequency discrimination functions and moreover controls the rotation phase of capstan motor 30 to perform proper tracking control.

Claims

1. A method of operation of a tracking control apparatus for use with a magnetic tape having a video track and a control track, said tracking control apparatus comprising:
 - a capstan motor (30) adapted to be rotated at a predetermined speed to transport the magnetic tape at a constant speed;
 - rotation frequency signal generating means (28, 32, 62) for generating a pulse



latch 508 to hold the count value (data representing P-CTL signal's time of arrival) of timer counter 504 (step ST2). CPU 502 thus reads arrival-time data (counts of the timer counter) from latches 506 and 508 and then writes the arrival-time data (NVP) read from latch 506 into RAM 518 (step ST4). Subsequently CPU 502 calculates the difference between the arrival-time data (NVP) of reference signal a, which has been written into RAM 518, and the arrival-time data (NPCTL) of P-CTL signal c' read from latch 508 (step ST5). This difference corresponds to the phase difference between reference signal a and P-CTL signal c'. The operation of phase comparison is thus achieved.

The FG signal generated by FG coil 28 is amplified by amplifier 32 and then wave-shaped by Schmitt circuit 62. As a result, C-FG signal e' proportional to the rotation frequency of capstan motor 30 is formed. In operation of frequency discrimination, as shown in Fig. 6, upon arrival at microcomputer 50 (step ST6), C-FG signal e' is entered to CPU 502 and latch 510. Every time C-FG signal e' arrives at microcomputer 50, CPU 502 causes latch 510 to hold the count of timer counter 504 (step ST9). Upon arrival of C-FG signal e', CPU 502 reads the arrival-time data of signal e' from latch 510 (step ST8). Subsequently CPU 502 writes the time data read from latch 510 into RAM 518 (step ST9). CPU 502 then calculates the difference between two successive pieces of arrival-time data of C-FG signal e', one of which being now written into RAM 518 and the other of which having been written therein previously (step ST10). In step ST11, CPU 502 calculates the controlled variable in phase of capstan motor 30 from the difference in time data calculated in step ST10. An interval between successive times of arrival of signal C-FG signal e' can be found in this way. CPU 502 detects the frequency of C-FG signal e', thereby achieving the operation of frequency discrimination.

CPU 502 mixes the speed error and the phase error together, which are obtained by the above described operations, in accordance with a predetermined arithmetic operation to produce motor control signal g' which is adapted to rotate capstan motor 30 in predetermined phase and at predetermined speed. Motor control signal g' is converted to an analog signal by D/A converter 514 and then applied to motor drive amplifier 38 for amplification. The amplified motor control signal from motor drive amplifier 38 drives capstan motor 30.

The video signal reproduced by video head 40 is amplified by preamplifier 42 and then applied to peak detector 44. Peak detector 44 detects a peak value of the input video signal, which is entered to microcomputer 50.

The tracking control operation will now be described with reference to Fig. 7. When the peak level of a video signal being reproduced is detected by peak detector 44, the detected peak level is entered to A/D converter 512 (step ST12). CPU 502 reads the peak level of the video signal being reproduced via A/D converter 512 (step ST13). Subsequently CPU 502 calculates the phase controlled variable of motor 30 so that the peak level may become maximum (step ST14).

At the same time, CPU 502 varies the controlled variable of the motor control signal by a predetermined amount in accordance with the amount of phase error obtained by the phase comparison operation in steps ST1 - ST5 (step ST15). CPU 502 then reads, as described above, the peak level of the reproduced video signal after the controlled variable is varied and searches for a point at which the peak level becomes maximum (step ST16). If the point at which the peak level becomes maximum has thus been found, CPU 502 sets the maximum peak level at a desired value (step ST17). CPU 502 varies the controlled variable of the motor control signal so that the desired value may be attained (step ST18). The tracking control is achieved in this way.

Referring to Fig. 8, the control operation of capstan motor 30 is as follows. The speed controlled variable of capstan motor 30 calculated in step ST11 and the phase controlled variable of motor 30 calculated in step ST14 are added together to produce a motor controlled variable (step ST19). The motor controlled variable is subsequently converted to an analog signal by D/A converter 514 for application to motor drive amplifier 38 as motor control signal g, (step ST20). Capstan motor 30 is responsive to the output of motor drive amplifier 38 to rotate at the predetermined phase and the predetermined speed.

According to the tracking control apparatus arranged as above, CPU 502 in microcomputer 50 controls the speed and phase of capstan motor 30 by means of its phase comparison and frequency discrimination functions and moreover controls the rotation phase of capstan motor 30 to perform proper tracking control.

Claims

1. A method of operation of a tracking control apparatus for use with a magnetic tape having a video track and a control track, said tracking control apparatus comprising:
 - a capstan motor (30) adapted to be rotated at a predetermined speed to transport the magnetic tape at a constant speed;
 - rotation frequency signal generating means (28, 32, 62) for generating a pulse



signal (e') with a frequency dependent on the rotation frequency of said capstan motor (30);

- reference signal generating means (12) for generating a predetermined reference signal (a);
- control signal reproducing means (18) for reproducing a control signal (c) from the control track of the magnetic tape;
- video-signal reproducing means (40) for reproducing a video signal from the video track of the magnetic tape;
- level detecting means (44) for detecting a predetermined level of the video signal reproduced by said video-signal reproducing means (40);
- a microprocessor (50) including a timer (504) for calculating (α) the rotation frequency of said capstan motor (30) in accordance with the pulse signal (e') from said rotation frequency signal generating means (28, 32, 62), (β) the rotation phase error of said capstan motor (30) by making a phase comparison between the reference signal (a) and an amplified and wave-shaped control signal (c') obtained by amplifying and wave-shaping said control signal (c); and (γ) control data for said capstan motor (30) from the rotation frequency and the rotation phase error of said capstan motor (30) and for providing the control data to said capstan motor (30).

characterized in that the method includes the steps of

- generating time data by said timer (504) every time the predetermined reference signal (a) arrives at said microprocessor (50), every time said amplified and wave-shaped control signal (c') arrives at said microprocessor (50) and every time the said pulse signal arrives at said microprocessor;
- calculating the rotation frequency on the basis of the difference between time data generated by said timer (504) when said pulse signal (e') arrives at said microprocessor (50), and
- calculating the rotation phase error of said capstan motor (30) on the basis of the difference between time data, which is generated by said timer (504) when the reference signal (a) is generated by said reference signal generating means (12), and time data which is generated by said timer means (504) when said amplified and wave-shaped control signal (c') is input to said microprocessor (50).

Patentansprüche

1. Verfahren zum Betrieb eines Spurhaltungsregelungsgeräts zum Einsatz bei einem Magnetband mit einer Videospur und einer Steuer-
spur, wobei das Spurhaltungsregelungsgerät aufweist:

einen Antriebsmotor (30), der so angepaßt ist, daß er mit einer vorbestimmten Geschwindigkeit gedreht wird, um das Magnetband mit einer konstanten Geschwindigkeit zu transportieren;

eine umdrehungsfrequenzsignalerzeugende Einrichtung (28, 32, 62) zum Erzeugen eines Impulssignals (e') mit einer Frequenz, die von der Umdrehungsfrequenz des Antriebsmotors (30) abhängt;

eine bezugssignalerzeugende Einrichtung (12) zum Erzeugen eines vorbestimmten Bezugssignals (a);

eine steuersignalreproduzierende Einrichtung (18) zum Reproduzieren eines Steuersignals (c) von der Steuerspur des Magnetbands;

eine videosignalreproduzierende Einrichtung (40) zum Reproduzieren eines Videosignals von der Videospur des Magnetbands;

eine Pegelerkennungseinrichtung (44) zum Erkennen eines vorbestimmten Pegels des von der videosignalreproduzierenden Einrichtung (40) reproduzierten Videosignals;

einen Mikroprozessor (50), der einen Zeit- bzw. Taktgeber (504) beinhaltet zum Berechnen (α) der Umdrehungsfrequenz des Antriebsmotors (30) in Übereinstimmung mit dem Impulssignal (e') von der umdrehungsfrequenzsignalerzeugenden Einrichtung (28, 32, 62), (β) des Umdrehungsphasenfehlers des Antriebsmotors (30) durch Durchführung eines Phasenvergleichs zwischen dem Bezugssignal (a) und einem verstärkten und wellengeformten Steuersignal (c'), das durch Verstärken und Wellenformen des Steuersignals (c) erhalten wird; und (γ) der Steuerdaten für den Antriebsmotor (30) von der Umdrehungsfrequenz und dem Umdrehungsphasenfehler des Antriebsmotors (30) und zum Liefern der Steuerdaten an den Antriebsmotor (30),

dadurch gekennzeichnet, daß das Verfahren die Schritte beinhaltet zum

Erzeugen von Zeit- bzw. Taktdaten durch einen Taktgeber (504) jedesmal, wenn das vorbestimmte Bezugssignal (a) bei dem Mikroprozessor (50) ankommt, und jedesmal, wenn das verstärkte und wellengeformte Steuersignal (c') beim Mikroprozessor (50) ankommt, und jedesmal, wenn das Impulssignal beim Mikroprozessor ankommt,



Berechnen der Umdrehungsfrequenz auf der Grundlage des Unterschieds zwischen den vom Taktgeber (504) erzeugten Taktdaten, wenn das Impulssignal (e') beim Mikroprozessor (50) ankommt, und

Berechnen des Umdrehungsphasenfehlers des Antriebsmotors (30) auf der Grundlage des Unterschieds zwischen den Taktdaten, die von dem Taktgeber (504) erzeugt werden, wenn das Bezugssignal (a) von der bezugssignalerzeugenden Einrichtung (12) erzeugt wird, und den Taktdaten, die von der Taktgebereinrichtung (504) erzeugt werden, wenn das verstärkte und wellengeformte Steuersignal (c') in den Mikroprozessor (50) eingegeben wird.

Revendications

1. Un procédé de fonctionnement d'un dispositif de commande de suivi de piste prévu pour l'utilisation avec une bande magnétique ayant une piste vidéo et une piste de commande, ce dispositif de commande de suivi de piste comprenant :

- un moteur de cabestan (30) conçu pour être mis en rotation à une vitesse prédéterminée de façon à transporter la bande magnétique à une vitesse constante;
- des moyens de génération de signal de fréquence de rotation (28, 32, 62) destinés à générer un signal sous forme d'impulsions (e') ayant une fréquence qui dépend de la fréquence de rotation du moteur de cabestan (30);
- des moyens de génération de signal de référence (12) destinés à générer un signal de référence prédéterminé (a);
- des moyens de reproduction de signal de commande (18) destinés à reproduire un signal de commande (c) à partir de la piste de commande de la bande magnétique;
- des moyens de reproduction de signal vidéo (40) destinés à reproduire un signal vidéo à partir de la piste vidéo de la bande magnétique;
- des moyens de détection de niveau (44) destinés à détecter un niveau prédéterminé du signal vidéo qui est reproduit par les moyens de reproduction de signal vidéo (40);
- un microprocesseur (50) comprenant un dispositif de mesure de temps (504) pour calculer (α) la fréquence de rotation du moteur de cabestan (30) conformément au signal sous forme d'impulsions (e') qui provient des moyens de génération de signal de fréquence de rotation (28,

32, 62), (β) l'erreur de phase de rotation du moteur de cabestan (30), en effectuant une comparaison de phase entre le signal de référence (a) et un signal de commande amplifié et mis en forme (c') qui est obtenu par amplification et mise en forme du signal de commande (c); et (γ) des données de commande pour le moteur de cabestan (30), à partir de la fréquence de rotation et de l'erreur de phase de rotation du moteur de cabestan (30), et destiné à appliquer les données de commande au moteur de cabestan (30).

caractérisé en ce que ce procédé comprend les étapes suivantes :

- on génère des données de temps au moyen du dispositif de mesure de temps (504), chaque fois que le signal de référence prédéterminé (a) arrive au microprocesseur (50), chaque fois que le signal de commande amplifié et mis en forme (c') arrive au microprocesseur (50), et chaque fois que le signal sous forme d'impulsions arrive au microprocesseur;
- on calcule la fréquence de rotation sur la base de la différence entre les données de temps qui sont générées par le dispositif de mesure de temps (504) lorsque le signal sous forme d'impulsions (e') arrive au microprocesseur (50), et
- on calcule l'erreur de phase de rotation du moteur de cabestan (30) sur la base de la différence entre des données de temps qui sont générées par le dispositif de mesure de temps (504) lorsque les moyens de génération de signal de référence (12) génèrent le signal de référence (a), et des données de temps qui sont générées par les moyens de mesure de temps (504) lorsque le signal de commande amplifié et mis en forme (c') est appliqué au microprocesseur (50).