COOPERATIVE WRITES OVER THE ADDRESS CHANNEL OF A BUS

RELATED APPLICATIONS

[0001] The present Application for Patent claims priority to Provisional Application No. 60/776,529 entitled "Cooperative Writes Over Address Channel" filed February 24, 2006, and assigned to the assignee hereof and hereby expressly incorporated by reference herein.

[0002] The present Application for Patent is related to the following co-pending U.S. Patent Applications:

"Auxiliary Writes Over Address Channel" having Attorney Docket No. 060485, filed concurrently herewith, assigned to the assignee hereof, and expressly incorporated by reference herein.

BACKGROUND

Field

[0003] The present disclosure relates generally to processing systems, and more specifically, to systems and techniques for performing cooperative writes over the address channel of a bus.

Background

[0004] At the heart of most modern processing systems is an interconnect referred to as a bus. The bus moves information between various processing entities in the system. Today, most bus architectures are fairly standardized. These standardized bus architectures typically have independent and separate read, write and address channels.

[0005] This type of bus architecture is often found in processing systems with one or more general purpose processors supported by memory. In these systems, the memory provides a storage medium that holds the programs and data needed by the processors to perform their functions. A processor may read or write to the memory by placing an address on the address channel and sending the appropriate read/write control signal.

Depending on the state of the read/write control, the processor either writes to the memory over the write channel or reads from the memory over the read channel. In these types of processing systems, as well as many others, it is desirable to reduce the write latency and increase the write bandwidth.

SUMMARY

[0006] An aspect of a processing system is disclosed. The processing system includes a receiving device, a bus having first, second and third channels, and a sending device configured to address the receiving device on the first channel, and read a payload from the receiving device on the second channel, the sending device being further configured to write a first portion of a payload to the receiving device on the first channel and a second portion of the payload to the receiving device on the third channel.

[0007] Another aspect of a processing system is disclosed. The processing system includes a receiving device, a bus having first, second and third channels, means for addressing the receiving device on the first channel, means for reading a payload from the receiving device on the second channel, and means for writing a first portion of a payload to the receiving device on the first channel and a second portion of the payload to the receiving device on the third channel.

[0008] An aspect of a method of communicating between a sending device and a receiving device over a bus is disclosed. The bus includes first, second and third channels. The method includes addressing a receiving device on the first channel, reading a payload from the receiving device on the second channel, and writing a first portion of a payload to the receiving device on the first channel and a second portion of the payload to the receiving device on the third channel.

[0009] An aspect of a bus mastering device is disclosed. The bus mastering device includes a processor, and a bus interface configured to interface the processor to a bus having first, second and third channels, the bus interface being further configured to address a slave on the first channel, receive a payload from the slave on the second channel, and write a first portion of a payload to the slave on the first channel and a second portion of the payload to the slave on the third channel.

[0010] Another aspect of a bus mastering device is disclosed. The bus mastering device includes a processor, and means for interfacing the processor to a bus having first, second and third channels, the means for interfacing the processor to the bus comprising means for addressing a slave on the first channel, means for receiving a payload from the slave on the second channel, and means for writing a first portion of a payload to the slave on the first channel and a second portion of the payload to the slave on the third channel.

[0011] An aspect of a slave device is disclosed. The slave device includes memory, and a bus interface configured to interface the memory to a bus having first, second and third channels, the bus interface being configured to receive an address and a first portion of a payload from a bus mastering device on the first channel, send a payload to the bus mastering device on the second channel, and receive a second portion of the payload from the bus mastering device on the third channel.

[0012] Another aspect of a slave device is disclosed. The slave device includes memory, and means for interfacing the memory to a bus having first, second and third channels, the means for interfacing the memory to the bus comprising means for receiving an address and a first portion of a payload from a bus mastering device on the first channel, means for sending a payload to the bus mastering device on the second channel, and means for receiving a second portion of the payload from the bus mastering device on the third channel.

[0013] It is understood that other embodiments of the present invention will become readily apparent to those skilled in the art from the following detailed description, wherein various embodiments of the invention are shown and described by way of illustration. As will be realized, the invention is capable of other and different embodiments and its several details are capable of modification in various other respects, all without departing from the present invention. Accordingly, the drawings and detailed description are to be regarded as illustrative in nature and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Aspects of the present invention are illustrated by way of example, and not by way of limitation, in the accompanying drawings, wherein:

[0015] FIG. 1 is a simplified block diagram illustrating an example of two devices in a processing system communicating over a bus;

[0016] FIG. 2 is an illustration showing information flowing on the address and write channels of a bus in the processing system of FIG. 1 with the address channel providing a generic medium for addresses and data;

[0017] FIG. 3 is a timing diagram showing two write operations over a bus in the processing system of FIG. 1;

[0018] FIG. 4 is a simplified block diagram illustrating a cache coherent processing system with two processing devices in communication with a shared resource through a bus interconnect;

[0019] FIG. 5 is an illustration showing the information flowing on the address and write channels between one processing device and the bus interconnect in the cache coherent processing system of FIG. 4;

[0020] FIG. 6 is a simplified block diagram illustrating an example of two devices in a processing system communicating over a 4-channel bus; and

[0021] FIG. 7 is an illustration showing information flowing on the address and write channels of a 4-channel bus in the processing system of FIG. 6 with the read and write address channels providing a generic media for addresses and data.

DETAILED DESCRIPTION

[0022] The detailed description set forth below in connection with the appended drawings is intended as a description of various embodiments of the present invention and is not intended to represent the only embodiments in which the present invention may be practiced. The detailed description includes specific details for the purpose of providing a thorough understanding of the present invention. However, it will be apparent to those skilled in the art that the present invention may be practiced without these specific details. In some instances, well-known structures and components are shown in block diagram form in order to avoid obscuring the concepts of the present invention.

[0023] FIG. 1 is a simplified block diagram illustrating an example of two devices in a processing system communicating over a bus. The processing system 100 may be a collection of hardware devices that cooperate to perform one or more processing functions. Typical applications of the processing system 100 include, but are not limited to, desktop computers, laptop computers, servers, cellular phones, personal digital assistants (PDA), game consoles, pagers, modems, audio equipment, medical devices, automotive, video equipment, industrial equipment, or any other machine or device capable of processing, retrieving and storing information.

[0024] The processing system 100 is shown with a sending device 102 in communication with a receiving device 104 over a bus 106. The bus 106 includes three channels: an address channel 106a, a write channel 106b, and a read channel 106c. A "channel" is defined as a set of electrical conductors used to carry information between two devices and which has a set of common control signals. In this example, each channel is 32-bits wide. Typically, a bus interconnect (not shown) will be used to establish a point-to-point communications path between the sending device 102 and the receiving device 104 over the bus 106. Alternatively, the bus 106 may be a dedicated bus, a shared bus, or any other type of suitable bus architecture.

[0025] The sending device 102 may be any type of bus mastering device. In this example, the sending device 102 includes a processor 108 and a bus interface 110. The processor 108 may be a general purpose processor, such as a microprocessor, a special purpose processor, such as a digital signal processor (DSP), an application specific integrated circuit (ASIC), a direct memory access (DMA) controller, a bridge, a programmable logic component, or any other entity that requires access to the bus 106. The bus interface 110 is used to drive the address and write channels 106a, 106b, as well as provide the appropriate control signals. The bus interface 110 also serves as a receiver for the read channel 106c.

[0026] The receiving device 104 may be any type of slave device. The receiving device 104 may be temporary memory, such as SDRAM, DRAM, or RAM, or a longer term storage device such as flash memory, ROM memory, EPROM memory, EEPROM memory, CD-ROM, DVD, magnetic disk, rewritable optic disk, etc.. Alternatively, the receiving device 104 may be a bridge or any other device capable of retrieving and

storing information. In this example, the receiving device 104 includes a bus interface 112 and memory 114. The bus interface 112 is used to drive the read channel 106c and the appropriate control signals. The bus interface 112 also serves as a receiver for the address and write channels 106a, 106b. The memory 114 may be any device whose contents can be accessed (i.e., read and written to) randomly.

[0027] In this bus architecture, the sending device 102 may read from or write to the receiving device 104. When the sending device 102 performs a write operation, it sends the address to the receiving device 104 on the address channel 106a with the appropriate control signals. The payload may be sent either on the address channel 106a, the write channel 106b, or both. The "payload" refers to the data associated with a particular read or write operation, and in this case, a write operation. When the sending device performs a read operation, it sends the address to the receiving device 104 on the address channel 106a with the appropriate control signals. In response, the receiving device 104 sends the payload to the sending device 102 on the read channel 106c.

[0028] An example of two write operations will now be described with reference to FIG. 2. FIG. 2 is an illustration showing the information flowing on the address and write channels. In this example, the sending device initiates two 16-byte write operations.

[0029] Referring to FIG. 2, on the first clock cycle 202, the sending device initiates the first 16-byte write operation by sending a 4-byte address A1 to the receiving device on the address channel 106a with the appropriate control signals. During the same clock cycle 202, the sending device also sends the first 4-bytes of the first payload W1(1) to the receiving device on the write channel 106b.

[0030] On the second clock cycle 204, the sending device uses both the address channel 106a and the write channel 106b to send data. The sending device sends the second 4-bytes of the first payload W1(2) on the write channel 106b and third 4-bytes of the first payload W1(3) on the address channel 106a

[0031] The sending device initiates the next 16-byte write operation during the third clock cycle 206 by sending a 4-byte address A2 to the receiving device on the address channel 106a with the appropriate control signals. The sending device completes the

transmission of the first payload during the same clock cycle of the next write operation by sending the final 4-bytes W1(4) to the receiving device on the write channel 106b.

[0032] The sending device then uses the next two clock cycles to send the second payload to the receiving device. On the fourth clock cycle 208, the sending device sends to the receiving device the first 4-bytes of the second payload W2(1) on the write channel 106b and the second 4-bytes of the second payload W2(2) on the address channel 106a. On the next clock cycle 210, the sending device sends to the receiving device the third 4-bytes of the second payload W2(3) on the write channel 106b and the final 4-bytes of the second payload W2(4) on the address channel 106a.

[0033] Two types of control signals may be used to support a medium for the transmission of addresses and data. The first control signal, referred to as an "Address/Data" signal, is used on the address channel 106a to indicate whether the information being transmitted is an address or data. In this example, when the Address/Data signal is asserted, an address is being transmitted on the address channel 106a. Conversely, when the Address/Data signal is deasserted, data is being transmitted on the address channel 106a.

[0034] The second control signal, referred to as a "Beat ID," is used on both the address and write channels 106a, 106b to indicate the beat of the current payload being transmitted. It should be noted that the "Beat ID" is a zero-based indicator such that a value of "0" indicates the first beat of the payload being transmitted. In this example, each payload is transmitted in its entirety before the next payload is transmitted, and therefore, there is no need for signaling to identify each payload. In alternative embodiments of the processing system, where the payloads are transmitted out of order, or the beats of different payloads are interleaved, the signaling may include payload sequence numbers.

[0035] An example illustrating how the two control signals may be used will now be described with reference to FIG. 3. The bus protocol for the address and write channels 106a, 106b is shown below in Table 1. This bus protocol is being used to illustrate the inventive aspects of a processing system, with the understanding that such inventive aspects may be used with other bus protocols. Those skilled in the art will

readily be able to vary and/or add signals to this protocol in the actual implementation of the bus architectures described herein.

TABLE 1

Address Channel		
Signal	**Definition**	**Driven By**
Address	32-bit medium to transmit addresses and data.	Sending Device
Address/Data	Indicates whether the information being transmitted on the address channel is an address or data.	Sending Device
AValid	Indicates whether valid information is being transmitted on the address channel.	
Address Beat ID	Indicates which beat of the payload is being transmitted on the address channel during a data tenure.	Sending Device
Read/Write	Indicates whether a read or write operation is being requested during an address tenure.	Sending Device
Payload Size	Indicates the size of the payload for the current address.	Sending Device
Address Transfer Ack	Indicates whether the receiving device has successfully received information transmitted on the address channel.	Receiving Device

Write Channel		
Signal	**Definition**	**Driven By**
Write	32-bit medium to transmit data.	Sending Device
WValid	Indicates whether valid information is being transmitted on the write channel.	Sending Device
Write Beat ID	Indicates which beat of the payload is being transmitted on the write channel.	
Write Transfer Ack	Indicates whether the receiving device has successfully received information transmitted on the write channel.	Receiving Device

TABLE 2

Beat ID	Definition
00	Indicates that the first beat of the payload is being transmitted on the channel.
01	Indicates that the second beat of the payload is being transmitted on the channel.
10	Indicates that the third beat of the payload is being transmitted on the channel.
11	Indicates that the fourth beat of the payload is being transmitted on the channel.

[0036] FIG. 3 is a timing diagram showing the control signaling for the same two 16-byte write operations described above in connection with FIG. 2. A System Clock 306 may be used to synchronize communications between the sending and receiving devices. The System Clock 306 is shown with five clock cycles, with each clock cycle numbered sequentially.

[0037] A write operation may be initiated on the address channel 106a by the sending device during the first clock cycle 301. This write operation is achieved by transmitting the address A1 for the first write operation on the 32-bit Address medium 308. The sending device asserts the AValid 312 signal to indicate that valid information is being transmitted on the address channel 106a. The sending device 102 also asserts the Address/Data signal 313 to indicate that the information being transmitted on the address channel 106a is an address. The sending device 102 deasserts the Read/Write signal 316 to request a write operation. The Payload Size 318 signal may be used to indicate the size of the payload, which in this case is 16-bytes. The state of the Address Beat ID 314 can be ignored during an address tenure on the address channel 106a.

[0038] During the same first clock cycle 301, the sending device uses the Write medium 320 to transmit the first 4-bytes of the first payload W1(1) and sets the Write Beat ID 326 to "00". The sending device also asserts the WValid signal 324 to indicate that valid information is being transmitted on the write channel 106b.

[0039] At the end of the first clock cycle 301, the sending device checks for an asserted Address Transfer Ack signal 310 to confirm the successful delivery of the address A1 over the address channel 106a to the receiving device. The sending device also checks for an asserted Write Transfer Ack signal 322 to confirm the successful delivery of the first 4-bytes of the first payload W1(1) over the write channel 106b to the receiving device.

[0040] On the second clock cycle 302, the sending device uses the Write medium 320 to send the second 4-bytes of the first payload W1(2) and sets the Write Beat ID 326 to "01". The sending device also asserts the WValid signal 324 to indicate that valid information is being transmitted on the write channel 106b.

[0041] During the same second clock cycle 302, the sending device transmits the third 4-bytes of the first payload W1(3) to the receiving device on the Address medium 308 and sets the Address Beat ID 314 to "10". The sending device also asserts the AValid 312 signal to indicate that valid information is being transmitted on the address channel 106a and deasserts the Address/Data signal 313 to indicate that the information being transmitted on the address channel 106a is data. The state of the Read/Write signal 316 and Payload Size 318 may be ignored during a data tenure on the address

channel 106a. In FIG. 3, the Read/Write signal 316 and the Payload Size 318 remain unchanged, but could be set to any state.

[0042] At the end of the second clock cycle 302, the sending device checks for an asserted Write Transfer Ack signal 322 to confirm the successful delivery of the second 4-bytes of the first payload W1(2) over the write channel 106b to the receiving device. The sending device also checks for an asserted Address Transfer Ack signal 310 to confirm the successful delivery of the third 4-bytes of the first payload W1(3) over the address channel 106a to the receiving device.

[0043] On the third clock cycle 303, the sending device uses the Write medium 320 to send the final 4-bytes of the first payload W1(4) and sets the Write Beat ID 326 to "11". The sending device also asserts the WValid signal 324 to indicate that valid information is being transmitted on the write channel 106b.

[0044] During the same third clock cycle 303 as completing the first write operation, the sending device transmits the address A2 for the second 16-byte write operation on the Address medium 308. The sending device asserts the AValid 312 signal to indicate that valid information is being transmitted on the address channel 106a. The sending device 102 also asserts the Address/Data signal 313 to indicate that the information being transmitted on the address channel 106a is an address A2. The sending device 102 deasserts the Read/Write signal 316 to request a write operation. The Payload Size 318 signal may be used to indicate the size of the payload, which in this case is 16-bytes. The state of the Address Beat ID 314 can be ignored during an address tenure on the address channel 106a.

[0045] At the end of the third clock cycle 303, the sending device checks for an asserted Address Transfer Ack signal 310 to confirm the successful delivery of the address A2 over the address channel 106a to the receiving device. The sending device also checks for an asserted Write Transfer Ack signal 322 to confirm the successful delivery of the final 4-bytes of the first payload W1(4) over the write channel 106b to the receiving device.

[0046] The sending device uses the next two clock cycles to send the second payload to the receiving device. On the fourth clock cycle 304, the sending device sends the first 4-bytes of the second payload W2(1) to the receiving device using the

Write medium 320 and sets the Write Beat ID 326 to "00". The sending device continues to assert the WValid signal 324 to indicate that valid information is being transmitted on the write channel 106b.

[0047] During the same fourth clock cycle 304, the sending device transmits the second 4-bytes of the second payload W2(2) on the Address medium 308 and sets the Address Beat ID 314 to "01". The sending device also asserts the AValid 312 signal to indicate that valid information is being transmitted on the address channel 106a and deasserts the Address/Data signal 313 to indicate that the information being transmitted on the address channel 106a is data. The state of the Read/Write signal 316 and Payload Size 318 may be ignored during a data tenure on the address channel 106a.

[0048] At the end of the fourth clock cycle 304, the sending device checks for an asserted Write Transfer Ack signal 322 to confirm the successful delivery of the first 4-bytes of the second payload W2(1) over the write channel 106b to the receiving device. The sending device also checks for an asserted Address Transfer Ack signal 310 to confirm the successful delivery of the second 4-bytes of the second payload W2(2) over the address channel 106a to the receiving device.

[0049] On the fifth clock cycle 305, the sending device sends the third 4-bytes of the second payload W2(3) to the receiving device using the Write medium 320 and sets the Write Beat ID 326 to "10". The sending device assert the WValid signal 324 to indicate that valid information is being transmitted on the write channel 106b.

[0050] During the same fifth clock cycle 305, the sending device transmits the final 4-bytes of the second payload W2(4) on the Address medium 308 and sets the Address Beat ID 314 to "11". The sending device also asserts the AValid 312 signal to indicate that valid information is being transmitted on the address channel 106a and deasserts the Address/Data signal 313 to indicate that the information being transmitted on the address channel 106a is data. The state of the Read/Write signal 316 and Payload Size 318 may be ignored during a data tenure on the address channel 106a.

[0051] At the end of the fifth clock cycle 305, the sending device checks for an asserted Write Transfer Ack signal 322 to confirm the successful delivery of the third 4-bytes of the second payload W2(3) over the write channel 106b to the receiving device. The sending device also checks for an asserted Address Transfer Ack signal 310 to

confirm the successful delivery of the final 4-bytes of the second payload W2(4) over the address channel 106a to the receiving device.

[0052] A reduction in signaling may be achieved by replacing the Beat ID with an implicit addressing scheme. An example of such an implicit addressing scheme is shown in FIG. 2. In this example, the implicit addressing scheme requires that the next 4-byte sequence of the current payload be transmitted on the earliest clock cycle available, with preference given to the write channel 106b over the address channel 106a.

[0053] Referring to FIG. 2, the earliest clock cycle available to send the first 4-bytes of the first payload W1(1) is the first clock cycle 202 and the write channel 106b is available during that clock cycle 202. The earliest clock cycle available to send the second 4-bytes of the first payload W1(2) is the second clock cycle 204, and again the write channel 106b is available. The second clock cycle 204 is also available to transmit the third 4-bytes of the first payload W1(3), but the write channel 106b is not available. Thus, the third 4-bytes of the first payload W1(3) are transmitted on the address channel 106a. The earliest clock cycle available to send the final 4-bytes of the first payload W1(4) is the third clock cycle 206, and again the write channel 106b is available.

[0054] During the third clock cycle 206, the address A2 for the second write operation is transmitted to the receiving device. However, the write channel 106a is not available to send the first 4-bytes of the second payload W2(1) because it is needed during the third clock cycle 206 to send the final 4-bytes of the first payload W1(4). The earliest clock cycle available to send the first 4-bytes of the second payload W2(1) is the fourth clock cycle 208 and the write channel 106b is available during that clock cycle 208. The fourth clock cycle 208 is also available to transmit the second 4-bytes of the second payload W2(2), but the write channel 106b is not available. Thus, the second 4-bytes of the second payload W2(2) are transmitted on the address channel 106a. The earliest clock cycle available to send the final 8-bytes of the second payload W2(3), W2(4) is the fifth clock cycle 210. The third 4-bytes of the second payload W2(3) are transmitted on the write channel 106b, i.e., the preferred channel, and the final 4-bytes of the second payload W2(4) are transmitted on the address channel 106a.

[0055] The use of the address channel as a medium for transmitting addresses and data can be employed in various processing environments. By way of example, this technique may be used to reduce the amount of time it takes for a processor to acquire a cache line from another processor in a hardware enforced cache coherent system. This example will be described further with reference to FIG. 4. A cache coherent processing system 400 is shown in FIG. 4 with two processing devices 402a, 402b in communication with a shared resource, such as a memory device 404, through a bus interconnect 406. In this example, the first processing device 402a reads from the memory device 404 by placing an address on its address channel $406a_1$ with the appropriate control signals. The address is forwarded to the memory device 404 by the bus interconnect 406 on the memory's address channel $406a_3$. In response, the bus interface 408 retrieves a block of data from the memory 410 and places it on the memory's read channel $406c_3$. The bus interconnect 406 forwards the data from the memory device 404a to the first processing device 402a over the first processor device's read channel $406c_1$. Once received by the first processing device 402a, the data may be placed in cache 412, modified by a processor 414 and written back to the memory device 404 by the bus interface 416. The write operation may be performed in the same manner as described above in connection with FIGS. 2 and 3.

[0056] Cache coherency deals with the situation where the second processing device 402b subsequently attempts to read from the same address. Without a mechanism to ensure cache coherency, the second processing device 402b might receive stale data from the memory device 404 if the data in the cache 412 of the first processing device 402a has been modified but not yet written back to the memory device 404.

[0057] A process referred to as "snooping" is commonly used to maintain coherency between cache and memory. Snooping is the process where a processing device, such as the second processing device 402b in this example, issues a read request to a cacheable address in the memory device 404 not present in its own cache 418, which causes the bus interconnect 406 to broadcast the snoop address to the other processing devices in the system prior to forwarding the read request to the memory device 404 for the data. If another processing device, such as the first processing device 402a, has the requested data stored in its cache 412 in a modified state, it will write the

modified data back to the memory device 404. Simultaneously, the bus interconnect 406 will send the modified data to the second processing device 402b over the read channel $406c_2$ between. The second processing device 402 will place the modified data in the cache 418 for use by the processor 422.

[0058] FIG. 5 is an illustration showing the information flowing on the address and write channels $406a_1$, $406b_1$ between the first processing device 402a and the bus interconnect 406. Referring to FIGS. 4 and 5, the first processing device 402a writes a 32-byte payload from its cache 412 to the memory device 404 in response to a snoop address broadcast by the bus interconnect 406. The write operation is performed by sending the 32-byte payload to the bus interconnect 406 using both the address and write channels $406a_1$, $406b_1$. On the first clock cycle 502, the first processing device 402a sends the snooped address A to the bus interconnect 406 on its address channel $406a_1$ with the appropriate control signals. During the same clock cycle 502, the first 4-bytes of the payload W(1) are sent by the first processing device 402a to the bus interconnect 406 on the write channel $406b_1$.

[0059] The remainder of the payload is sent from the first processing device 402a to the bus interconnect 406 over the next four clock cycles. On the second clock cycle 504, the first processing device 402a sends the second 4-bytes of the payload W(2) on the write channel $406b_1$ and third 4-bytes of the payload W(3) on the address channel $406a_1$. The fourth 4-bytes of the payload W(4), the sixth 4-bytes of the payload W(6), and the final 4-bytes of the payload W(8) are sent by the first processing device 402a to the bus interconnect 406 on the write channel $406b_1$ over the next three clock cycles 506, 508 510. The fifth 4-bytes of the payload W(5) and the seventh 4-bytes of the payload W(7) are sent by the first processing device 402a to the bus interconnect 406 on the address channel $406a_1$ over the next two clock cycles 506, 508.

[0060] The bus interconnect 406 may send the 32-byte payload to the memory device 404 in a similar manner using both the address and write channels $406a_3$, $406b_3$ to send the payload in 5-clock cycles. The bus interconnect 406 also sends the 32-byte payload to the second processing device 402b on the read channel $406c_2$ in 8-clock cycles in response to the original read request of processing device 402b. The transmission of the 32-byte payload to the memory device 404 and the second

processing device 402 can overlap or follow the transmission of the payload between the first processing device 402a and the bus interconnect 406.

[0061] An explanation of the control signaling, which was described in detail in connection with FIG. 3, will not be repeated here other than to say that the Beat ID for both the address and write channels $406a_1$, $406b_1$ will need to be expanded to a 3-bit code to handle an 8-beat payload.

[0062] FIG. 6 is a simplified block diagram illustrating an example of two devices in a processing system 600 communicating over a 4-channel bus. A separate and independent address channel is provided for each read and write channel. In this example, each channel is 32-bits wide, but may be any width in practice depending upon the particular application and overall design constraints. A write operation over the 4-channel bus may be performed by sending to the receiving device 604 an address on the write address channel 606a and data on the write address channel 606a, the write channel 606b, and/or the read address channel 606d. A read operation over the 4-channel bus is performed by sending to the receiving device 604 an address on a read address channel 606d. In response, the receiving device 604 sends the payload to the sending device 602 on the read channel 606c.

[0063] FIG. 7 is an illustration showing the information flowing on the write address, read address, and write channels between the sending device and receiving device over a 4-channel bus. On the first clock cycle 702, the sending device initiates the first 16-byte write operation by sending a 4-byte address A1 to the receiving device on the write address channel 606a with the appropriate control signals. During the same clock cycle 702, the sending device also transmits the first 4-bytes of the first payload W1(1) on the write channel 606b and the second 4-bytes of the same payload W1(2) on the read address channel 606d.

[0064] On the second clock cycle 704, the remainder of the first payload is sent by the sending device to the receiving device. More specifically, on the second clock cycle 704 as completing the first write operation, the sending device transmits the third 4-bytes of the first payload W1(3) on the write channel 606b and final 4-bytes of the first payload W1(4) on the read address channel 606d. During the same clock cycle 704, the

sending device sends the address A2 for the second 16-byte write operation to the receiving device on the write address channel 606a.

[0065] The sending device then uses the next two clock cycles to send the second payload to the receiving device. On the third clock cycle 706, the sending device sends to the receiving device the first 4-bytes of the second payload W2(1) on the write channel 606b, the second 4-bytes of the second payload W2(2) on the read address channel 606d, and the third 4-bytes of the second payload W2(3) on the write address channel 606a. On the next clock cycle 708, the sending device sends the final 4-bytes of the second payload W2(4) on the write channel 606b to the receiving device.

[0066] The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic component, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing components, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0067] The methods or algorithms described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. A storage medium may be coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in the sending and/or receiving component, or elsewhere. In the alternative, the processor and the storage

medium may reside as discrete components in the sending and/or receiving component, or elsewhere.

[0068] The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the invention. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

WHAT IS CLAIMED IS:

CLAIMS

1. A processing system, comprising:

a receiving device;

a bus having first, second and third channels; and

a sending device configured to address the receiving device on the first channel, and read a payload from the receiving device on the second channel, the sending device being further configured to write a first portion of a payload to the receiving device on the first channel and a second portion of the payload to the receiving device on the third channel.

2. The processing system of claim 1 wherein the sending device is further configured to concurrently write the first and second portions of the payload to the receiving device.

3. The processing system of claim 1 wherein the sending device is further configured to concurrently address the receiving device and write the second portion of the payload to the receiving device.

4. The processing system of claim 1 wherein the sending device is further configured write the first and second portions of the payload to a first address of the receiving device, the sending device being further configured to send a second address to the receiving device on the first channel concurrently with the writing of the second portion of the payload to the receiving device.

5. The processing system of claim 1 wherein the sending device comprises a first processing device and the receiving device comprises a bus interconnect, the processing system further comprising a second processing device, the bus interconnect being configured to connect the first and second processing devices to a shared resource, and wherein the first processing device is further configured to write the first and second portions of a payload to the bus interconnect in response to a snoop address from the second processing device.

6. The processing system of claim 1 wherein the bus further comprises a fourth channel, the sending device being further configured to address the receiving device on the first channel for write operations and address the receiving device on the fourth channel for read operations, and wherein the sending device is further configured to write a third portion of the payload to the receiving device on the fourth channel.

7. The processing system of claim 6 wherein the sending device is further configured to concurrently write the first, second and third portions of the payload to the receiving device.

8. The processing system of claim 6 wherein the sending device is further configured write the first, second and third portions of the payload to a first address of the receiving device, the sending device being further configured to send a second address to the receiving device on the first channel concurrently with the writing of the second or third portion of the payload to the receiving device.

9. The processing system of claim 1 wherein the sending device is further configured to provide a control signal to the receiving device indicating whether the first channel is currently being used to address the receiving device or write the first portion of the payload to the receiving device.

10. The processing system of claim 1 wherein the sending device is further configured to provide a control signal on each of the first and third channels to the receiving device, each of the control signals identifying the portion of the payload being sent on its corresponding channel.

11. A processing system, comprising:

a receiving device;

a bus having first, second and third channels;

means for addressing the receiving device on the first channel;

means for reading a payload from the receiving device on the second channel; and

means for writing a first portion of a payload to the receiving device on the first channel and a second portion of the payload to the receiving device on the third channel.

12. A method of communicating between a sending device and a receiving device over a bus, the bus comprising first, second and third channels, the method comprising:

addressing a receiving device on the first channel,

reading a payload from the receiving device on the second channel; and

writing a first portion of a payload to the receiving device on the first channel and a second portion of the payload to the receiving device on the third channel.

13. The method of claim 12 wherein the first and second portions of the payload are concurrently written to the receiving device.

14. The method of claim 12 wherein the receiving device is addressed concurrently with the writing of the second portion of the payload to the receiving device.

15. The method of claim 12 wherein the first and second portions of the payload a written to a first address of the receiving device, the addressing of the receiving device further comprising sending a second address to the receiving device on the first channel concurrently with the writing of the second portion of the payload to the receiving device.

16. The method of claim 12 wherein the sending device comprises a first processing device and the receiving device comprises a bus interconnect, the processing system further comprising a second processing device, the bus interconnect being configured to connect the first and second processing devices to a shared resource, and wherein the first and second portions of a payload are written to the bus interconnect in response to a snoop address from the second processing device.

17. The method of claim 12 wherein the bus further comprises a fourth channel, the addressing of the receiving device on the first channel being for write operations, the method further comprising addressing the receiving device on the fourth channel for read operations, and writing a third portion of the payload to the receiving device on the fourth channel.

18. The method of claim 17 wherein the sending device is further configured to concurrently write the first, second and third portions of the payload to the receiving device.

19. The method of claim 18 wherein the first, second and third portions of the payload are written to a first address of the receiving device, the method further comprising sending a second address to the receiving device on the first channel concurrently with the writing of the second or third portion of the payload to the receiving device.

20. The method of claim 12 further comprising providing a control signal to the receiving device indicating whether the first channel is currently being used to address the receiving device or write the first portion of the payload to the receiving device.

21. The method of claim 12 further comprising a control signal on each of the first and third channels to the receiving device, each of the control signals identifying the portion of the payload being sent on its corresponding channel.

22. A bus mastering device, comprising:

a processor; and

a bus interface configured to interface the processor to a bus having first, second and third channels, the bus interface being further configured to address a slave on the first channel, receive a payload from the slave on the second channel, and write a first portion of a payload to the slave on the first channel and a second portion of the payload to the slave on the third channel.

23. The bus mastering device of claim 22 wherein the bus interface is further configured to concurrently write the first and second portions of the payload to the slave.

24. The bus mastering device of claim 22 wherein the bus interface is further configured to concurrently address the slave and write the second portion of the payload to the slave.

25. The bus mastering device of claim 22 wherein the bus interface is further configured write the first and second portions of the payload to a first address of the slave, the bus interface being further configured to send a second address to the slave on the first channel concurrently with the writing of the second portion of the payload to the slave.

26. The bus mastering device of claim 22 wherein the slave comprises a bus interconnect configured to connect the bus mastering device and a second bus mastering device to a shared resource, and wherein the bus mastering device is further configured to write the first and second portions of a payload to the bus interconnect in response to a snoop address from the second bus mastering device.

27. The bus mastering device of claim 22 wherein the bus further comprises a fourth channel, the bus interface being further configured to address the slave on the first channel for write operations and address the slave on the fourth channel for read operations, and wherein the bus interface is further configured to write a third portion of the payload to the slave on the fourth channel.

28. The bus mastering device of claim 27 wherein the bus interface is further configured to concurrently write the first, second and third portions of the payload to the slave.

29. The bus mastering device of claim 27 wherein the bus interface is further configured write the first, second and third portions of the payload to a first address of the slave, the bus interface being further configured to send a second address to the

slave on the first channel concurrently with the writing of the second or third portion of the payload to the slave.

30. The bus mastering device of claim 22 wherein the bus interface is further configured to provide a control signal to the slave indicating whether the first channel is currently being used to address the slave or write the first portion of the payload to the slave.

31. The bus mastering device of claim 22 wherein the bus interface is further configured to provide a control signal on each of the first and third channels to the slave, each of the control signals identifying the portion of the payload being sent on its corresponding channel.

32. A bus mastering device, comprising:

a processor; and

means for interfacing the processor to a bus having first, second and third channels, the means for interfacing the processor to the bus comprising means for addressing a slave on the first channel, means for receiving a payload from the slave on the second channel, and means for writing a first portion of a payload to the slave on the first channel and a second portion of the payload to the slave on the third channel..

33. A slave device, comprising:

memory; and

a bus interface configured to interface the memory to a bus having first, second and third channels, the bus interface being configured to receive an address and a first portion of a payload from a bus mastering device on the first channel, send a payload to the bus mastering device on the second channel, and receive a second portion of the payload from the bus mastering device on the third.

34. The slave device of claim 33 wherein the bus interface is further configured to concurrently receive the first and second portions of the payload.

35. The slave device of claim 33 wherein the bus interface is further configured to concurrently receive the address and the second portion of the payload.

36. The slave device of claim 33 wherein the bus interface is further configured write the first and second portions of the payload to a first address in the memory, the bus interface being further configured to receive a second address on the first channel concurrently with the second portion of the payload.

37. The slave device of claim 33 wherein the bus further comprises a fourth channel, the bus interface being further configured to receive the address on the first channel for write operations and receive an address on the fourth channel for a read operation, and wherein the bus interface is further configured to receive a third portion of the payload from the bus mastering device on the fourth channel.

38. The slave device of claim 37 wherein the bus interface is further configured to concurrently receive the first, second and third portions of the payload.

39. The slave device of claim 37 wherein the bus interface is further configured write the first, second and third portions of the payload to a first address in the memory, the bus interface being further configured to receive a second address from the bus mastering device on the first channel concurrently with the receipt of the second or third portion of the payload.

40. The slave device of claim 33 wherein the bus interface is further configured to receive a control signal from the bus mastering device indicating whether the first channel is currently being used to send the address or the first portion of the payload.

41. The slave device of claim 33 wherein the bus interface is further configured to receive a control signal on each of the first and third channels from the bus mastering device, each of the control signals identifying the portion of the payload being sent on its corresponding channel.

42. A slave device, comprising:

memory; and

means for interfacing the memory to a bus having first, second and third channels, the means for interfacing the memory to the bus comprising means for receiving an address and a first portion of a payload from a bus mastering device on the first channel, means for sending a payload to the bus mastering device on the second channel, and means for receiving a second portion of the payload from the bus mastering device on the third channel.