

ULTRA-SMALL CAPACITOR ARRAY

Background of the Invention

The present invention relates generally to small electronic components adapted to be mounted on a larger circuit board. More particularly, the invention relates to an ultra-small capacitor array for use in a variety of applications.

For some time, the design of various electronic components has been driven by a general industry trend toward miniaturization. In this regard, a need exists for ever smaller electronic components having exceptional operating characteristics. For example, some applications may require a very small capacitor array wherein each of the individual capacitors has a relatively large capacitance value.

Consider a device specifying an exterior size of no greater than 0.50 mils and 0.55 mils in respective width and length dimensions, while providing an array of three capacitors each having a capacitance of at least 560 picofarads. It is very difficult in such a small component to provide multiple capacitors having the desired capacitance value. Adequate termination structures for connection of the device to external circuitry must also be provided.

Summary of the Invention

The present invention recognizes various disadvantages of prior art constructions and

present invention to provide a novel electronic component.

It is a further object of the present invention to provide a novel capacitor array of
5 ultra-small dimensions.

It is a further object of the present invention to provide a novel capacitor array wherein each of the individual capacitors has a relatively large capacitance value.

10 It is a still further object of the present invention to provide a novel thin-film capacitor device.

It is an additional object of the present invention to provide a method of manufacturing a
15 thin film capacitor array.

Some of these objects are achieved by a miniature capacitor device for inverted mounting to a predetermined surface. The device comprises a substrate, such as silicon, glass or Al_2O_3 . A first
20 conductive layer is disposed on the substrate. The first conductive layer defines at least one first capacitor plate and a first terminal structure adjacent thereto. In addition, a dielectric layer is disposed on the first capacitor plate. A second
25 conductive layer defines at least one second capacitor plate and a second terminal structure adjacent thereto. The second capacitor plate is disposed on the dielectric layer in opposition to the first capacitor plate. It will often be
30 desirable to also provide an encapsulate material disposed over layers on the substrate. The

encapsulate material is defined to expose the first and second terminal structures.

The dielectric material may preferably have a dielectric constant of at least about 100. Often, the dielectric constant may exceed 500, with a dielectric constant of 1100 being utilized in some exemplary embodiments. The dielectric material may comprises a lead-based dielectric material such as a PZT material. Such a dielectric layer may have a thickness of no greater than approximately 1.0 μm .

The first conductive layer may comprise at least three first capacitor plates. In this case, the second conductive layer comprises at least three second capacitor plates respectively opposed thereto. The second conductive layer may further define a respective second terminal structure disposed adjacent to each of the second capacitor plates.

Other objects of the invention are achieved by a miniature capacitor array having a plurality of capacitor devices in a single package. The device comprises a substrate having a first conductive layer disposed thereon. The first conductive layer defines a plurality of first capacitor plates. A dielectric layer is disposed on the plurality of first capacitor plates. A second conductive layer defines a plurality of second capacitor plates disposed on the dielectric layer in opposition to respective of the first capacitor plates. The second conductive layer further defines respective terminal structures adjacent to each of the second

capacitor plates. It will often be desirable to provide an encapsulate material disposed over layers on the substrate. The encapsulate material is defined to expose the terminal structures.

5 The first conductive layer may comprise at least three first capacitor plates. The second conductive layer may comprise at least three second capacitor plates respectively opposed thereto.

10 In some exemplary embodiments, the top surface of the substrate has an area of no greater than approximately 2750 square mils. Each of the capacitor devices may be advantageously located between a respective pair of terminal structures. The capacitor devices may have a relatively large
15 capacitance value.

 The first conductive layer may be a continuous conductive layer in which the plurality of capacitor plates comprise integral portions thereof. The first conductive layer may define a
20 common terminal structure as a further integral portion thereof.

 Further objects of the present invention are achieved by an electronic device comprising at least one thin film capacitor arranged on a
25 substrate. The capacitor of the electronic device has a capacitance of approximately equal to or greater than 14 nanofarad/mil².

 In some exemplary embodiments, the thin film capacitor is located between terminals configured
30 for connection of the electronic device to external circuitry. The capacitor may have a dielectric

layer with a thickness of no greater than approximately 1.0 μm . For example, the dielectric layer may have a thickness of approximately 0.8 to 1.0 μm . A PZT dielectric material applied by a sol-gel process may be utilized.

Other objects of the invention are achieved by a method of manufacturing a thin film capacitor array. As an initial step, the method involves providing a generally planar substrate. A first conductive layer is applied to the substrate and formed so as to define a plurality of first capacitor plates. A dielectric layer is then applied to cover the first capacitor plates of the first conductive layer. Next, a second conductive layer is applied to define a plurality of second capacitor plates opposed to respective of the first capacitor plates. An encapsulate material may also be applied over the layers on the substrate.

Other objects, features and aspects of the present invention are provided by various combinations and subcombinations of the disclosed elements, as well as methods of practicing same, which are discussed in greater detail below.

Brief Description of the Drawings

A full and enabling disclosure of the present invention, including the best mode thereof, to one of ordinary skill in the art, is set forth more particularly in the remainder of the specification, including reference to the accompanying drawings, in which:

Figure 1 is a side elevation of an ultra-small

capacitor array of the present invention as mounted to a printed circuit board;

Figure 2 is a plan view of the ultra-small capacitor array of Figure 1 as taken along line 2-2;

Figure 3 is a schematic diagram of the circuit provided by the capacitor array of Figure 2;

Figure 4 is a cross-sectional view as taken along line 4-4 of Figure 2;

Figure 5 is a cross-sectional view as taken along line 5-5 of Figure 2;

Figure 6 is a cross-sectional view as taken along line 6-6 of Figure 2;

Figures 7A through 7E illustrate successive steps in the manufacture of a capacitor array as in Figure 2;

Figures 8A through 8D illustrate successive steps in the manufacture of a first alternative capacitor array;

Figures 9A through 9D illustrate successive steps in the manufacture of a second alternative capacitor array; and

Figure 10 is a schematic diagram of the circuit provided by the capacitor array produced as shown in Figures 9A through 9D.

Repeat use of reference characters in the present specification and drawings is intended to represent same or analogous features or elements of the invention.

Detailed Description of Preferred Embodiments

It is to be understood by one of skill in the

art that the present discussion is a description of exemplary embodiments only, and is not intended as limiting the broader aspects of the present invention, which broader aspects are embodied in the exemplary constructions.

Figure 1 illustrates a miniature capacitor device 10 of the present invention surface mounted to a printed circuit board 12. As can be seen, device 10 is inverted so that terminal structures on its "top" are electrically connected to circuit traces of the circuit board 12. This electrical connection is typically supplied by solder bumps 14, which also function to maintain device 10 in its physical location on the board.

Referring now to Figure 2, capacitor device 10 is configured in the illustrated embodiment as an integrated array having a plurality of individual capacitors. In particular, device 10 has three individual capacitors 16a, 16b and 16c. One plate of each capacitor is electrically connected to an associated terminal 18a, 18b, and 18c of a first polarity. A second plate of each capacitor is electrically connected to a common ground terminal 20. The equivalent circuit formed by the illustrated arrangement is depicted schematically in Figure 3.

In this case, capacitors 16a, 16b and 16c are formed as thin film capacitors having a pair of opposed capacitor plates separated by a predetermined dielectric. Presently preferred embodiments utilize a high-K dielectric to achieve

a relatively large capacitance value in a small package. For example, it will often be desirable to utilize a dielectric material exhibiting a dielectric constant of approximately 100 or more.

5 A dielectric constant of greater than approximately 500 will often be preferred, with a dielectric constant of approximately 1100 being used in some exemplary embodiments.

Certain lead-based dielectrics, such as
10 $\text{Pb}(\text{Zr},\text{Ti})\text{O}_3$ (referred to as PZT), are suitable for this purpose. The PZT may be doped with Nb, thereby yielding a PNZT material. Various aspects of PZT dielectrics are discussed in U.S. Patent No. 5,625,529 to Lee, incorporated herein by reference.

15 The upper capacitor plate 22a, 22b and 22c of each opposed pair is formed by a respective conductive pattern formed above the dielectric. The lower capacitor plate of each opposed pair is formed by a conductive layer 24 located under the
20 dielectric. Specifically, the portion of conductive layer 24 underlying each of the upper capacitor plates 22a, 22b and 22c forms the respective lower capacitor plate.

It can be seen that terminals 18a, 18b and 18c
25 are formed as integral extensions of respective upper capacitor plates 22a, 22b and 22c.

Conductive layer 24, on the other hand, integrally extends to ground terminal 20. This arrangement provides a structure in which the terminals are
30 widely spaced near the corners of device 10. Such spacing may reduce the incidence of short circuits

that may occur when device 10 is mounted to circuit board 12. In addition, the capacitors themselves are located adjacent to, instead of coincident with, the terminal structures. This reduces stress during device mounting that could otherwise damage a thin dielectric.

Despite the fact that device 10 will often have multiple capacitors of relatively large capacitance, the dimensions of device 10 will often be quite small. For example, it would not be unusual for the length L of device 10 to measure less than about 55 mil. In one exemplary embodiment, each side of device 10 may measure only about 40 mil.

The various layers in device 10 can be most easily explained with reference to Figures 4 through 6. Lower conductive layer 24 is located on the top surface of a suitable substrate 24, such as silicon, glass or Al_2O_3 . Particularly where a PZT dielectric is utilized, conductive layer 24 may be constructed having a metallic layer 28 of a highly conductive metal and an oxide layer 30 of a material adapted to collect oxygen vacancies in the dielectric. One suitable oxide material that may be utilized for this purpose is lanthanum strontium cobalt oxide (LSCO).

Dielectric layer 32 is located above lower conductive layer 24, at least in regions where upper capacitor plates 22a, 22b and 22c will be applied. As noted above, terminals 18a, 18b and 18c are formed as integral extensions of the upper

capacitor plates. A conductive layer 34, formed in the same manner as the upper capacitor plates and their associated terminals, may be optionally located on lower conductive layer 24 at ground terminal 20.

The various layers located on substrate 26 may be protected by a suitable encapsulate. In presently preferred embodiments, the encapsulate may comprise a primary passivation layer 36 of SiN or the like. A secondary passivation layer 38 of a suitable polymer material may also be provided. One such polymer material that may be utilized for this purpose is benzocyclobutene (BCB). The use of BCB as a polymer coating to a primary passivation layer is discussed in A.J.G. Strandjord et al., "Photosensitive Benzocyclobutene for Stress-Buffer and Passivation Applications (One Mask Manufacturing Process)", 1997 Electronic Components and Technology Conference, incorporated herein by reference. As shown, the encapsulate is patterned to expose the various terminals of device 10.

Figures 7A through 7E illustrate various steps employed in the manufacture of device 10. Referring first to Figure 7A, substrate 26 is illustrated prior to the application of any layers. It will be appreciated that the length and width of device 10 will generally be defined by the size of substrate 26. Next, as shown in Figure 7B, lower conductive layer 24 is applied to the top surface of substrate 26. In exemplary embodiments, lower conductive layer 24 may be a layer of platinum

metallization that has been patterned according to conventional processing techniques.

Figure 7C illustrates dielectric layer 32 applied to cover a selected portion of lower conductive layer 24. As described above, dielectric layer 32 is preferably a lead-based dielectric having a relatively high dielectric constant. According to preferred methodology, the dielectric is applied by a sol-gel coating process and subsequently patterned as desired.

A sol-gel process that applies relatively thick coating cycles is particularly preferred to achieve a given layer thickness with a fewer coats. For example, a 1,3-propanediol-based PZT solution synthesis may be utilized to apply PZT films having a thickness of 0.4-0.5 μ m per spin casting cycle. As such, only two coats may be necessary to achieve desired thickness levels of about 0.8-1.0 μ m. This is in comparison with many conventional sol-gel techniques which may only achieve a thickness of about 0.1 μ m with each coating cycle. A more detailed description of a sol-gel coating process that may be utilized herein is given in Liu et al., "Thick Layer Deposition of Lead Perovskites Using Diol-Based Chemical Solution Approach," Integrated Ferroelectrics, 1997, Vol. 18, pp. 263-274, incorporated herein by reference.

Referring now to Figure 7D, a patterned second conductive layer provides terminals 18a, 18b and 18c as well as upper capacitor plates 22a, 22b and 22c. As described above, a conductive layer 34 may

also be optionally provided in direct contact with lower conductive layer 24. A Cr/Ni plus Ag, Pd layer applied by typical processing techniques, such as by sputtering, is suitable for this second
5 conductive layer.

The various layers formed on substrate 26 are then encapsulated as shown in Figure 7E. The encapsulate material is patterned, such as by etching, to expose the terminal structures.

10 The use of a dielectric having a high dielectric constant in devices of the present invention allows a large capacitance to be achieved in a small plate area (X times Y). In fact, exemplary embodiments of the invention may exhibit
15 a capacitance of about 14 nanofarad/mil² or more. As an example, each capacitor of device 10 may have a plate area of about 175 mil² or less. In one exemplary embodiment, the plate area (X times Y) of each capacitor may be only about 100 mil² while
20 having a capacitance value of 560 picofarads or more.

Figures 8A through 8D illustrate the manufacture of an alternative three-capacitor array according to the present invention. For the sake
25 of simplicity, the steps involved in producing this device will not be described in detail. Steps or elements analogous to similar steps or elements in device 10 are represented by a reference number augmented by one-hundred.

30 The manufacture of a further alternative is illustrated in Figures 9A through 9D. Similarly,

steps or elements analogous to those of device 10 are represented by a reference number augmented by two-hundred. In this embodiment, any of the four terminals can be used as a common terminal for the other three. This is schematically illustrated in Figure 10.

It can be seen that the present invention provides integrated capacitor arrays having the simultaneous advantages of being very small while providing relatively large capacitance values at each capacitor. The preferred embodiments described above utilize integrated circuit fabrication techniques to integrate ferroelectric materials in a surface mountable electronic device. One of skill in the art will appreciate that variations and modifications may be made without departing from the invention. In addition, aspects of the various embodiments may be interchanged both in whole or in part. Furthermore, those of ordinary skill in the art will appreciate that the foregoing description is by way of example only, and is not intended to be limitative of the invention so further described in such appended claims.

WHAT IS CLAIMED IS:

1. A miniature capacitor device for inverted mounting to a predetermined surface, said device comprising:

a substrate;

5 a first conductive layer disposed on said substrate, said first conductive layer defining at least one first capacitor plate and a first terminal structure adjacent thereto;

10 a dielectric layer disposed on said first capacitor plate; and

a second conductive layer defining at least one second capacitor plate and a second terminal structure adjacent thereto, said second capacitor plate being disposed on said dielectric layer in
15 opposition to said first capacitor plate.

2. A miniature capacitor device as set forth in claim 1, further comprising an encapsulate material disposed over said layers on said substrate, said encapsulate material defined to
5 expose said first and second terminal structures.

3. A miniature capacitor device as set forth in claim 2, wherein said dielectric material has a dielectric constant of at least 100.

4. A miniature capacitor device as set forth in claim 3, wherein said dielectric material comprises a lead-based dielectric material.

5. A miniature capacitor device as set forth in claim 4, wherein said lead-based dielectric material comprises a PZT dielectric material.

6. A miniature capacitor device as set forth



in claim 3, wherein said dielectric layer has a thickness of no greater than approximately 1.0 μm .

7. A miniature capacitor device as set forth in claim 1, wherein said first conductive layer comprises at least three first capacitor plates and said second conductive layer comprises at least
5 three second capacitor plates respectively opposed thereto.

8. A miniature capacitor device as set forth in claim 7, wherein second conductive layer further defines a respective second terminal structure disposed adjacent to each of said second capacitor
5 plates.

9. A miniature capacitor device as set forth in claim 8, further comprising an encapsulate material disposed over said layers of said substrate, said encapsulate material defined to
5 expose said first and second terminal structures.

10. A miniature capacitor device as set forth in claim 1, wherein said substrate is selected from a group consisting of silicon, glass or Al_2O_3 .

11. A miniature capacitor array having a plurality of capacitor devices in a single package, said device comprising:

- a substrate;
- 5 a first conductive layer disposed on said substrate, said first conductive layer defining a plurality of first capacitor plates;
- a dielectric layer disposed on said plurality of first capacitor plates; and
- 10 a second conductive layer defining a plurality



of second capacitor plates disposed on said dielectric layer in opposition to respective of said first capacitor plates, said second conductive layer further defining respective terminal structures adjacent to each of said second capacitor plates.

12. A miniature capacitor array as set forth in claim 11, further comprising an encapsulate material disposed over said layers on said substrate, said encapsulate material defined to expose said terminal structures.

13. A miniature capacitor array as set forth in claim 11, wherein said first conductive layer comprises at least three first capacitor plates and said second conductive layer comprises at least three second capacitor plates respectively opposed thereto.

14. A miniature capacitor array as set forth in claim 13, wherein said top surface of said substrate has an area of no greater than approximately 175 square mils.

15. A miniature capacitor array as set forth in claim 14, wherein each of said plurality of capacitor devices is located between a respective pair of said terminal structures.

16. A miniature capacitor array as set forth in claim 14, wherein each of said capacitor devices has a capacitance of at least approximately 560 pf.

17. A miniature capacitor array as set forth in claim 11, wherein said first conductive layer is a continuous conductive layer in which said



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plurality of capacitor plates comprise integral portions thereof.

18. A miniature capacitor array as set forth in claim 17, wherein said first conductive layer defines a common terminal structure as a further integral portion thereof.

19. A miniature capacitor array as set forth in claim 11, wherein said dielectric material comprises a lead-based dielectric material having a dielectric constant of at least about 500.

20. A miniature capacitor array as set forth in claim 19, wherein said lead-based dielectric material comprises a PZT dielectric material.

21. A miniature capacitor device as set forth in claim 19, wherein said dielectric layer has a thickness of no greater than approximately $1.0\ \mu\text{m}$.

22. An electronic device comprising at least one thin film capacitor arranged on a substrate, said capacitor having a capacitance of at least approximately 14 nanofarads/mil².

23. An electronic device as set forth in claim 22, wherein said thin film capacitor is located between terminals configured for connection of said electronic device to external circuitry.

24. An electronic device as set forth in claim 22, wherein said capacitor has a dielectric layer having a thickness of no greater than approximately $1.0\ \mu\text{m}$.

25. An electronic device as set forth in claim 24, wherein said dielectric layer has a thickness of approximately 0.8 to 1.0 microns.



26. An electronic device as set forth in claim 24, wherein said dielectric layer comprises a PZT dielectric material.

27. An electronic device as set forth in claim 26, wherein said PZT material is applied by a sol-gel process.

28. A method of manufacturing a thin film capacitor array, said method comprising steps of:

- (a) providing a generally planar substrate;
- (b) applying a first conductive layer to said substrate, said first conductive layer formed so as to define a plurality of first capacitor plates;
- (c) applying a dielectric layer to cover said first capacitor plates of said first conductive layer;
- (d) applying a second conductive layer defining a plurality of second capacitor plates opposed to respective of said first capacitor plates.

29. A method as set forth in claim 28, further comprising the step of:

- (e) applying an encapsulate over said layers on said substrate.

30. A method as set forth in claim 28, wherein said second conductive layer is applied in step (d) so as to further define a plurality of terminal structures defined adjacent to respective of said second capacitor plates.

31. A method as set forth in claim 28, wherein said dielectric layer is applied in step (c) by a sol-gel process.



32. A method as set forth in claim 31, wherein said dielectric layer is a lead-based dielectric.

33. A method as set forth in claim 32, wherein said dielectric layer is a PZT dielectric.

34. A method as set forth in claim 31, wherein said dielectric layer is built-up from multiple sol-gel coats.

35. A method as set forth in claim 34, wherein said coats each have a thickness of greater than approximately 0.4 mils.

36. A method as set forth in claim 28, wherein said substrate is selected from a group consisting of silicon, glass and Al_2O_3 .

