CLAIMS

What is claimed is:

1. A method of forming a three dimensional memory array, comprising:

forming a stack comprising a set of conductive layers, wherein each conductive layer of the set is separated from an adjacent conductive layer of the set by a thermally insulating region, the thermally insulating region having a thermal resistance greater than that of the adjacent conductive layer;

forming a set of insulating layers within each thermally insulating region, wherein the set of insulating layers comprises at least two layers that comprise electrically insulating material;

forming a via through the stack, wherein at least a portion of the via passes through each conductive layer of the set of conductive layers;

forming a recess in at least one conductive layer of the set of conductive layers, wherein the recess is adjacent the via; and

forming a memory cell within the recess.

2. The method of claim **1**, wherein forming the set of insulating layers within each thermally insulating region comprises:

forming a first electrically insulating layer that comprises a first material; and

forming a second electrically insulating layer positioned on top of the first electrically insulating layer, wherein the second electrically insulating layer comprises a second material that is different from the first material.

3. The method of claim **1**, wherein forming the set of insulating layers within each thermally insulating region comprises:

forming a first electrically insulating layer according to a first set of formation parameters; and

forming a second electrically insulating layer according to a second set of formation parameters that is different from the first set of formation parameters, wherein the first electrically insulating layer and the second electrically insulating layer comprise a different material.

4. The method of claim **1**, wherein forming the set of insulating layers within each thermally insulating region comprises:

forming a first electrically insulating layer that comprises a first material;

forming a second layer positioned on top of the first electrically insulating layer, wherein the second layer comprises a second material different from the first material; and

forming a third layer positioned on top of the second layer, wherein the first and third layer comprise a same material.

5. The method of claim **4**, wherein the second material comprises at least one of a metal, a metal alloy, carbon, or a compound comprising silicon and nitrogen.

6. The method of claim **1**, wherein forming the stack, the set of insulating layers, and the memory cell comprises:

depositing material using one of chemical vapor deposition, metal-organic chemical vapor deposition, physical vapor deposition, or atomic layer deposition.

7. The method of claim **1**, further comprising:

forming a first conductive element on a surface of the via, wherein the first conductive element is coupled to the memory cell;

forming an intervening component on a surface of the first conductive element in the via, wherein the intervening component is coupled to the first conductive element; and

forming a second conductive element, wherein the second conductive element fills a remainder of the via and is coupled to the intervening component.

8. The method of claim **1**, further comprising:

forming an intervening material on the memory cell, wherein both the intervening material and the memory cell are formed within the recess;

forming an intervening component on a surface of the via, wherein the intervening component is coupled to the intervening material and the intervening material separates the intervening component and the memory cell; and

forming a conductive element, wherein the conductive element fills a remainder of the via and is coupled to the intervening component.

9. The method of claim **1**, further comprising:

forming a conductive element in the via, wherein the conductive element fills an entirety of the via and is coupled to the memory cell; and

forming an end component at an end of the conductive element and coupled to the conductive element, wherein the end component comprises one of a diode, a bipolar junction device, an ovonic threshold selector, a field effect transistor, or a chalcogenide material.

10. A three-dimensional memory array, comprising:

a first layer comprising a first memory cell coupled to a first electrode;

a second layer comprising a second memory cell coupled to a second electrode;

a third layer comprising a stack of at least two sublayers, the third layer positioned between the first and second layers, wherein the first, second, and third layers are each substantially parallel to one another; and

a third electrode coupled to the first and second memory cells, wherein the third electrode is substantially perpendicular to the first, second, and third layers.

11. The three-dimensional memory array of claim 10, wherein the stack of at least two sublayers comprise electrical and thermal insulators.

12. The three-dimensional memory array of claim 10, wherein the stack of at least two sublayers comprise an oxide material.

13. The three-dimensional memory array of claim 10, wherein the stack of at least two sublayers comprises materials with a different composition or stoichiometry from each other.

14. The three-dimensional memory array of claim 10, wherein the third layer further comprises:

a third sublayer positioned between the first and second sublayers.

15. The three-dimensional memory array of claim 14, wherein the third sublayer is a thermal conductor.

16. The three-dimensional memory array of claim 14, wherein the third sublayer comprises at least one of a metal, carbon, or a compound comprising silicon and nitrogen.

17. The three-dimensional memory array of claim 10, wherein the first electrode, the second electrode, and the third electrode each comprise at least one of tungsten, tungsten nitride, aluminum, titanium, titanium nitride, silicon, doped polycrystalline silicon, or carbon, or any combination thereof.

18. The three-dimensional memory array of claim 10, further comprising:

a selection component coupled to the third electrode; and

a conductive line coupled to the selection component, wherein the selection component separates the conductive line from the third electrode.

19. The three-dimensional memory array of claim 18, wherein the selection component comprises a diode, a bipolar junction device, an ovonic threshold selector, a field effect transistor, or a chalcogenide material.

20. The three-dimensional memory array of claim 10, wherein the first memory cell and the second memory cell each comprise a chalcogenide material.

21. The three-dimensional memory array of claim 10, wherein the first memory cell and the second memory cell each comprise a material with a programmable resistivity.

22. The three-dimensional memory array of claim 10, wherein the first and second memory cells are coaxial with the third electrode.

23. A three-dimensional memory array, comprising:

a first layer that comprises a first memory cell and a first electrode, wherein the first memory cell comprises a chalcogenide material and is coupled to the first electrode;

a second layer that comprises a second memory cell and a second electrode, wherein the second memory cell comprises the chalcogenide material and is coupled to the second electrode, and wherein the second layer is substantially parallel to the first layer;

a plurality of insulating layers positioned between the first layer and the second layer, wherein the plurality of insulating layers are substantially parallel to the first and second layers, and wherein a first insulating layer and a second insulating layer of the plurality each comprise an electrical insulator;

a third electrode positioned substantially perpendicular to the first and second layers, wherein the third electrode is adjacent to the first and second memory cells; and

a selection component coupled to the third electrode.

24. The three-dimensional memory array of claim 23, wherein the chalcogenide material comprises a phase change material.

25. The three-dimensional memory array of claim 23, wherein the plurality of insulating layers comprises three or more insulating layers.