contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing.

Semiconductor die 50~~6~~8 is mounted to conductive traces 512 formed on substrate 514 using bump material 516 formed on contact pads 518, using any of the embodiments from FIGs. 13a-13g, 14a-14d, 15a-15d, 16a-16c, and 17a-17b. Contact pads 518 and conductive traces 512 can correspond to the signal pads, power pads, or ground pads in the die pad layout of FIGs. 5-11. Semiconductor die 50~~8~~6 is electrically connected to contact pads 520 formed on substrate 514 using bond wires 522. The opposite end of bond wire 522 is bonded to contact pads 524 on semiconductor die 506.

Masking layer 526 is formed over substrate 514 and opened beyond the footprint of semiconductor die 506. While masking layer 526 does not confine bump material 516 to conductive traces 512 during reflow, the open mask can operate as a dam to prevent encapsulant 528 from migrating to contact pads 520 or bond wires 522 during MUF. Encapsulant 528 is deposited between semiconductor die 508 and substrate 514, similar to FIGs. 18a-18c. Masking layer 526 blocks MUF encapsulant 528 from reaching contact pads 520 and bond wires 522, which could cause a defect. Masking layer 526 allows a larger semiconductor die to be placed on a given substrate without risk of encapsulant 528 bleeding onto contact pads 520.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a semiconductor die including ~~having~~ a die pad layout comprising ~~with~~ signal pads located in no more than two peripheral rows ~~primarily~~ in a perimeter region of the semiconductor die, and power pads and ground pads located primarily in an inboard region of the semiconductor die from the signal pads;

forming a plurality of bumps over the signal pads, power pads, and ground pads of the semiconductor die;

providing a substrate;

forming a plurality of conductive traces ~~with~~ including interconnect sites disposed over the substrate, the bumps over the signal pads, power pads, and ground pads of the semiconductor die being wider than the interconnect sites of the conductive traces;

mounting the semiconductor die to the substrate with the bumps over the signal pads, power pads, and ground pads of the semiconductor die being bonded~~;~~

~~bonding the bumps~~ to the interconnect sites over the substrate so that the bumps cover a top surface and side surfaces of the interconnect sites; and

depositing an encapsulant around the bumps between the semiconductor die and substrate.

2. The method of claim 1, wherein the bumps include a fusible portion and non-fusible portion.

3. The method of claim 1, further including arranging the signal pads in ~~in a peripheral row or in~~ a peripheral array generally parallel to an edge of the semiconductor die.

4. The method of claim 1, further including arranging the signal pads in adjacent rows in a staggered arrangement or orthogonal arrangement.

5. The method of claim 1, wherein fewer than 10% of the power pads and ground pads are located within the perimeter region and fewer than 10% of the signal pads are located within the inboard region.

6. The method of claim 1, further including forming a masking layer over an area of the substrate away from the interconnect sites.

7. A method of making a semiconductor device, comprising:

providing a semiconductor die;

providing a substrate;

forming a plurality of conductive traces ~~with~~ including interconnect sites over the substrate arranged in a layout ~~with~~ comprising signal sites located in no more than two peripheral rows near a perimeter of the substrate, and power sites and ground sites located inboard from the signal sites over the substrate; and

forming an interconnect structure between the semiconductor die and substrate so that the interconnect structures cover a top surface and side surfaces of the signal sites, power sites, and ground sites over the substrate ~~interconnect sites~~.

8. The method of claim 7, further including depositing an encapsulant between the semiconductor die and substrate.

9. The method of claim 7, wherein the interconnect structure includes a fusible portion and non-fusible portion.

10. The method of claim 7, further including arranging the signal sites in ~~a peripheral row or in~~ a peripheral array generally parallel to an edge of the substrate.

11. The method of claim 7, further including arranging the signal sites in adjacent rows in a staggered arrangement or orthogonal arrangement.

12. The method of claim 7, further including arranging the power and ground sites in an array near a center of the substrate.

13. The method of claim 7, wherein a central region of the semiconductor die has no pads.

14. A method of making a semiconductor device, comprising:

providing a semiconductor die;

providing a substrate;

forming a plurality of conductive traces ~~with~~ including interconnect sites on the conductive traces and disposed over the substrate arranged in a layout ~~with~~ comprising signal sites located primarily in a perimeter region of the substrate, and power sites and ground sites located primarily in an inboard region of the substrate from the signal ~~pads~~ sites;

bonding the semiconductor die to the interconnect sites with bumps wider than the interconnect sites on the conductive traces; and

depositing an encapsulant between the semiconductor die and substrate.

15. The method of claim 14, further including forming an interconnect structure over the semiconductor die, the

interconnect structure including a fusible portion and non-fusible portion.

16. The method of claim 14, wherein fewer than 10% of the power sites and ground sites are located within the perimeter region.

17. The method of claim 14, wherein fewer than 10% of the signal sites are located within the inboard region.

18. The method of claim 14, further including arranging the signal sites in a peripheral row or in a peripheral array generally parallel to an edge of the substrate.

19. The method of claim 14, further including arranging the power sites and ground sites in an array near a center of the substrate.

20. The method of claim 14, further including arranging the signal sites in adjacent rows in a staggered arrangement or orthogonal arrangement.

21. A semiconductor device, comprising:

a semiconductor die ~~having~~ including a die pad layout ~~with~~comprising signal pads located primarily in a perimeter region of the semiconductor die, and power pads and ground pads located primarily in an inboard region of the semiconductor die from the signal pads;

a substrate;

a plurality of conductive traces ~~with~~ including interconnect sites formed over the substrate~~,~~; ~~wherein~~ interconnects comprising a width greater than a width of the

interconnect sites are bonded to the semiconductor die ~~is bonded to the~~ and interconnect sites; and

an encapsulant deposited between the semiconductor die and substrate.

22. The semiconductor device of claim 21, ~~further including an interconnect structure formed over the semiconductor die, the interconnect structure including~~ wherein the interconnects include a fusible portion and non-fusible portion.

23. The semiconductor device of claim 21, wherein fewer than 10% of the power pads and ground pads are located within the perimeter region.

24~~6~~. ~~The semiconductor device of claim 21, wherein fewer than 10% of the signal pads are located within the inboard region.~~ A semiconductor device, comprising:

a semiconductor die including a die pad layout comprising signal pads located primarily in a perimeter region of the semiconductor die, and power pads and ground pads located primarily in an inboard region of the semiconductor die from the signal pads;

a substrate;

a plurality of conductive traces including interconnect sites formed over the substrate;

bumps bonded to the semiconductor die and to a top surface and side surfaces of the interconnect sites; and

an encapsulant deposited between the semiconductor die and substrate.

2~~5~~4. The semiconductor device of claim 21, wherein the signal pads are arranged in adjacent rows in a staggered arrangement or orthogonal arrangement.

25. The semiconductor device of claim 21, wherein the signal pads are arranged in no more than two rows.

27. The semiconductor device of claim 26, wherein the bumps include a fusible portion and non-fusible portion.

28. The semiconductor device of claim 26, wherein fewer than 10% of the power pads and ground pads are located within the perimeter region.

29. The semiconductor device of claim 26, wherein the signal pads are arranged in adjacent rows in a staggered arrangement or orthogonal arrangement.

30. The semiconductor device of claim 26, wherein the signal pads are arranged in a peripheral row or in a peripheral array generally parallel to an edge of the substrate.

31. The semiconductor device of claim 26, wherein the power pads and ground pads are arranged in an array near a center of the substrate.