

APPARATUS AND METHOD FOR INSPECTING AND RE-CONDITIONING LEADS OF IC CHIPS

FIELD OF THE INVENTION

This invention relates to apparatus and a system for inspecting the leads of encapsulated IC chips, sorting out those that fail the quality criteria and re-conditioning their leads.

BACKGROUND OF THE INVENTION

Integrated circuits have achieved tremendous technological advancements in recent years. The small feature sizes and multiple circuit layers achieved today enable ultra large-scale integration (ULSI). More and more circuit modules are also integrated into a single chip. These IC chips are therefore getting more external lead connections. These leads also tend to be finer and more closely spaced.

Besides, these IC chips are increasing in economic value despite the decreasing costs of production.

With the continual push towards automation in the manufacturing industries, the quality requirements of IC chips are becoming more stringent. This is contrasted by the fact that finer and more closely spaced leads are more susceptible to damage during handling, which is aggravated by the use of high-speed, fully automated machines. The bigger surface areas and decreasing relative thicknesses of the chips also lead to warpage and distortion of the leads in terms of parallelism and planarity once a chip is encapsulated and removed from its mould. As the chips are relatively more expensive, it is more economical to inspect and re-condition the leads of those chips that have passed the functional tests but have not met the external quality requirements.

The push towards automation is not sufficient. The yield and throughput of the machines are becoming important factors, especially in the increasingly competitive manufacturing

environment.

As the economic value of IC chips is high, automation with minimal or no human intervention or handling is desired. This will ensure fewer operator errors, for example, that IC chips of different lots are not mis-identified.

SUMMARY OF THE INVENTION

With this invention, the primary objective of the example embodiments is to provide a fully integrated inspection process and system for IC chips and means for re-conditioning the leads.

Another objective is to increase the throughput of the machine.

According to a first aspect of the present invention, there is provided apparatus for inspecting and reconditioning the leads of IC chips comprising:

lead inspecting means for inspecting IC chips for defective leads;

lead reconditioning means for reconditioning leads determined to be reworkable by said lead inspecting means; and

transfer means for transferring chips with leads reconditioned by said lead reconditioning means to said lead inspecting means for reinspection; and for selectively presenting IC chips to said lead reconditioning means without first passing through said lead inspecting means.

Preferably the apparatus may further comprise sorter means to remove chips that fail reinspection.

The apparatus may also further comprise

a buffer station for a buffer of chips that have previously passed quality acceptance; and

a lead reject station;

wherein said sorter means is operable to remove chips that fail reinspection, to said lead reject station and to replace them with chips from said buffer station.

In one mode the apparatus may be operable to accept a tray of chips for reworking and to recondition them without first inspecting them and reinspecting them after reconditioning.

To operate in this mode there may preferably be:

- a scanning line for tray of chips to be inspected;
- a reconditioning line for receiving trays from the scanning line for reconditioning of reworkable chips; and
- a rework line for the input of trays of reworkable chips for reconditioning without prior scanning.

The apparatus may usefully be operable such that the contents of one tray of chips is scanned, while the defective contents of a previously scanned tray of chips are reconditioned. The apparatus may then be further operable such that a tray where all reworkable chips have been reconditioned is reinspected, while the reworkable contents of a previously scanned tray of chips are reconditioned.

For increased usefulness the apparatus may further comprise

- marking inspection means for inspecting chip markings;
 - removal means for removing chips that fail the chip marking inspection; and
 - reconditioning of the leads of reworkable chips and re-scanning, while a second tray containing chips for reconditioning of the leads is in concurrent process,
- whereby the chips from the first and second tray are differentiated.

According to a second aspect of the present invention, there is provided a method of inspecting and reconditioning the leads of IC chips, comprising the steps of:

- inspecting IC chips for defective leads;
 - re-conditioning the leads of chips determined to be reworkable in said inspecting step,
- and
- transferring chips with the leads reconditioned in said reconditioning step to said lead inspecting step for reinspection; and
 - selectively presenting IC chips for reconditioning without first passing through said lead inspecting step.

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The example embodiments provide an apparatus and system for inspecting and re-conditioning the leads of IC chips. The leads of the chips are scanned to determine their conditions by

comparing the images with that of a standard reference; those which do not match the reference image would have the leads re-conditioned and re-scanned, before being sorted for acceptance or rejection.

In concurrent processing, another tray with IC chips having reworkable leads may be input for reworking, just for reconditioning. The chips from the two trays are differentiated and returned to their respective trays, so as to preserve their lot identifications.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be further described by way of non-limitative examples with reference to the accompanying drawings, in which:-

Fig. 1 shows a schematic layout of a system for inspecting and reconditioning the leads of IC chips according to the embodiment of the invention.

DESCRIPTION OF THE EMBODIMENTS OF THE INVENTION

Referring to Fig. 1, the system of inspecting IC chips and the process of reconditioning the leads involve various stations and steps in a checking and reconditioning machine 1.

IC chips, typically held in a tray 10, are loaded into the machine 1 at an input station 20. The trays 10 have individual identifiers that allow them to be identified at different points along the route they travel in machine 1.

From the input station 20, the tray 10 is then conveyed to a pick-up position of an inspection station 30. A pick-and-place means 32 transfers two IC chip at a time from tray 10 to the inspection station 30. Inspection is done two at a time. However, only one chip is placed on the inspection station 30 when encountering an odd column of tray.

The inspection station 30 works in a standard way. The leads of the IC chips are scanned and an image captured. This is then compared to a reference image to determine the

conditions of the leads. The parameters of the leads of the IC chip, such as lead coplanarity, skew, pitch, length, foot angle and so on, are then stored in memory together with an identifier of the chip, usually its position in the tray 10. After being scanned, the IC chips are returned to their original positions in the trays.

Once all the chips have been scanned and returned to a tray 10, the tray is conveyed to the pick-up position of a unit rotation station 40. There unit rotation pick-and-place means 42 picks up two units at a time, rotates and returns them to the tray until all the chips have been rotated in their orientation. Once this has been done, the tray is conveyed to the tray transfer station 50.

From the input station 20 to the transfer station 50, the tray travels in a straight line in a first direction on an input conveying line. At the tray transfer station 50, a tray is transferred from position 52 to the start of an output conveying line at position 54. These positions 52, 54 also serve as buffer positions for the transfer of trays. There may also be intermediate positions, if necessary. From position 54 the trays travel in a straight line in an opposite direction along the output conveying line.

From position 54, a tray is conveyed to a mark inspection station 60. The markings of every chip are inspected by means of a camera. The conditions of the markings, such as clarity, orientation, mark identification and so on are also required to be satisfactory. Thus the results of the inspection are stored in memory together with the positions of the respective chips in the tray.

The tray is then indexed forward to rework position 56. At rework position 56, a rework pick-and-place means 130 retrieves from the tray 10 those chips with reworkable leads, one at a time, for realignment at a rework station 142 (based on the results from the inspection station 30). After reworking, the chips are returned back to their positions in tray 10 at rework position 56. Once all the chips with reworkable leads in a tray have been reworked, the tray 10 is then indexed to rescan position 58.

The chips for reworking are picked up based on the results of the inspection at the

inspection station 30, using the memorised tray identification and the chip positions within the tray 10. After being picked up, the chips are rotated 180° vertically and moved to a standby position. From there they are taken by a rework transfer arm 140 for reworking.

The rework station 142 operates in a known manner, bending unaligned leads in any three dimensions, to ensure correct and acceptable alignment.

At rescan position 58, reworked chips are removed again from the tray 10, by a sorter pick and place means 70 and taken back for rescanning at the inspection station 30. Those that pass reinspection are returned to their positions in tray 10. Those that fail are taken to a lead reject tray at lead reject station 90, which is replaced as and when it fills up.

Additionally, at rescan position 58, any chips that failed the mark inspection at mark inspection station 60 are removed, also by the sorter pick and place means 70 and loaded into a separate mark reject tray at mark reject station 100. This too is removed and replaced as and when it fills up.

A buffer tray containing chips that have passed both the quality and functional tests is provided at buffer station 110. After removing all the defective chips (ie, lead reject and mark reject), the sorter pick and place means 70 replaces them all with good chips from buffer station 110. In this way, the output tray, after passing through rescan position 58, would be fully filled. Finally the tray passes to an output station 80, with a full complement of chips for further use or processing.

The above process is a concurrent scan and rework process. There is a continuous throughput with transfer from one station to the next, relying not only on completion of working at the current station but also on the next station being vacant. As mentioned above, positions 52 and 54 act as buffers. There may be additional buffers elsewhere to avoid bottlenecks, especially if there is a particularly bad batch.

It should be noted that the above machine can be used to conduct just scanning alone – this would miss out the reworking steps, with all reject chips being removed at rescan position

58. It can also be used just as a reworking machine, by missing out the scanning, rescanning and sorting steps or missing out only the scanning but using rescanning and sorting. To make the latter possibility easier, the present invention includes a dedicated rework process line and a rework mode.

In the rework mode, a tray with only reworkable chips is placed into a rework input station 120. The tray is indexed to a position 122 and a rework rotary pick-and-place means 130 retrieves each chip for reworking in the same way as described above. After re-aligning of its leads each chip is returned to the tray. This cycle is repeated until all the leads of the reworkable chips have been corrected for their alignment. Once completed, the tray is indexed forward and accumulated at the output station 124 of the rework process line. From there it may be taken out, for instance to be placed in the input station 20 for concurrent scanning and reworking as described above.

In another concurrent mode processing, a tray 10' with chips is placed into input station 20 while another tray 10" with chips having reworkable leads is placed into the rework input station 120. In this mode the controller memorises the identities of the chips picked up at positions 56 and 122 during processing. To preserve the lot identification of the chips, the chips from each tray must be returned to the same tray after processing. Of course, the chips in buffer station 110 must be from the same lot as those loaded into station 20. However, the reworked chips at station 120 may be from a different lot. In this way, the utility of the scan station 30 and rework station 142 is further maximised, with neither being idle for long. If necessary a separate buffer of acceptable chips from the batch on the rework line may also be present.

Mark scanning and identifying is present in the preferred embodiment. However, it is not essential and the sorter may just remove and replace those that fail lead rescanning.

In the above description, the use of linear conveying means for the tray containing the IC chips are exemplified. However, the method of transferring the tray is not a limitation on this inventive concept. The use of a robot with rotary end effector may replace the transferring means for the tray, both linear and rotary.

While only one exemplary apparatus and several exemplary modes of the present invention has been described and illustrated, it is to be understood that many changes, modifications and variations could be made to the present invention without departing from the scope of the invention. For instance, the number of rework station 142 may be more than one so as to improve the throughput of this process. The limits of the invention will now be spelled out in the claims, with reference to above disclosure.

CLAIMS

1. Apparatus for inspecting and reconditioning the leads of IC chips comprising:
lead inspecting means for inspecting IC chips for defective leads;
lead reconditioning means for reconditioning leads determined to be reworkable by said lead inspecting means; and
transfer means for transferring chips with leads reconditioned by said lead reconditioning means to said lead inspecting means for reinspection; and for selectively presenting IC chips to said lead reconditioning means without first passing through said lead inspecting means.
2. Apparatus according to claim 1, further comprising sorter means to remove chips that fail reinspection.
3. Apparatus according to claim 2, further comprising
a buffer station for a buffer of chips that have previously passed quality acceptance; and
a lead reject station;
wherein said sorter means is operable to remove chips that fail reinspection, to said lead reject station and to replace them with chips from said buffer station.
4. Apparatus according to any one of the preceding claims, further comprising:
a scanning line for tray of chips to be inspected;
a reconditioning line for receiving trays from the scanning line for reconditioning of reworkable chips; and
a rework line for the input of trays of reworkable chips for reconditioning without prior scanning.
5. Apparatus according to any one of the preceding claims, operable such that the contents of one tray of chips is scanned, while the reworkable contents of a previously scanned tray of chips are reconditioned.

6. Apparatus according to claim 5, further operable such that a tray where all reworkable chips have been reconditioned is reinspected, while the reworkable contents of a previously scanned tray of chips are reconditioned.
7. Apparatus according to any one of the preceding claims, further comprising:
 - marking inspection means for inspecting chip markings;
 - removal means for removing chips that fail the chip marking inspection; and
 - reconditioning of the leads of reworkable chips and re-scanning, while a second tray containing chips for reconditioning of the leads is in concurrent process, whereby the chips from the first and second tray are differentiated.
8. A method of inspecting and reconditioning the leads of IC chips comprising:
 - inspecting IC chips for defective leads;
 - reconditioning the leads of chips determined to be reworkable in said inspecting step; and
 - transferring chips with the leads reconditioned in said reconditioning step to said lead inspecting step for reinspection; and
 - selectively presenting IC chips for reconditioning without first passing through said lead inspecting step.